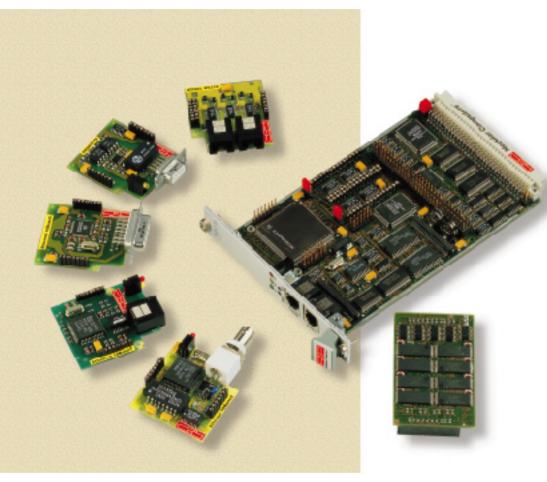


# VSBC-32

## 32-Bit Single-Board Computer



#### **32-Bit Computation Performance**

- QUad-channel Integrated
   Communications Controller
- Up to six serial interfaces
- Serial interfaces accessible by front-panel and CXC
- Flexible front-panel options for network and serial I/O
- CXC interface
- Up to 64 MByte DRAM & 4 MByte FLASH
- Implemented background debugging
- ► Low power consumption
- Extended operating temperature range capability
- Extensive software support
- CE conformance



A VMEbus single-board computer incorporating the 32-bit MC68(EN)360 high-performance QUad-channel Integrated Communications Controller (QUICC).





## **Ordering Information**

## VSBC-32



Product	Description	Order No.
VSBC-32-BASE	VMEbus single-board computer comprising MC68360 @ 25MHz, 256 kByte dual-ported SRAM (with Goldcap for	12479
	back-up), up to 6 serial interfaces without Ethernet support (two available on the front panel as RS232 (RJ45)	
	and an additional four divided between the CXC and SI-interfaces), CXC interface, PEPbug	
VSBC-32E-BASE	Same as order no. 12479 but with MC68EN360 @ 33MHz providing Ethernet support	12480
VSBC-32E-BASE	Same as order no. 12480 but with 1 MByte dual-ported SRAM	12499
DM600	Memory Piggyback with 4 MByte DRAM and 1 MByte FLASH memory for VSBC-32	11852
DM600	Memory Piggyback with 4 MByte DRAM and 4 MByte FLASH memory for VSBC-32	11853
DM601	Memory Piggyback with 16 MByte DRAM and 1 MByte FLASH memory for VSBC-32	11854
DM601	Memory Piggyback with 16 MByte DRAM and 4 MByte FLASH memory for VSBC-32	11855
DM602	Memory Piggyback with 1 MByte DRAM and 1 MByte FLASH memory for the VSBC-32	12765
DM603	Memory Piggyback with 32 MByte DRAM and 1 MByte FLASH memory for the VSBC-32	16329
DM603	Memory Piggyback with 32 MByte DRAM and 4 MByte FLASH memory for the VSBC-32	16330
DM604	Memory Piggyback with 8 MByte DRAM and 1 MByte FLASH memory for the VSBC-32	15911
DM604	Memory Piggyback with 8 MByte DRAM and 4 MByte FLASH memory for the VSBC-32	15912
DM605	Memory Piggyback with 64 MByte DRAM and 1 MByte FLASH memory for the VSBC-32	16369
DM605	Memory Piggyback with 64 MByte DRAM and 4 MByte FLASH memory for the VSBC-32	16368
SI-10B2	10Base2 Thin Ethernet interface piggyback with RG58 coax. connector	9925
SI-10B5	10Base5 Ethernet (AUI) interface piggyback with 15-pin D-Sub connector	9924
SI-10BT	10BaseT Twisted pair Ethernet interface piggyback with RJ45 connector	9926
SI-DUMMY	Front panel without extra interface(s)	12351
SI-PB232	Serial interface piggyback for 2x RS232 connections (Modem interface) with 2x RJ45 connectors	11850
SI-PB232-ISO	Serial interface piggyback for 1x optoisolated RS232 connection with 1x RJ45 connector	11851
SI-PB485-ISO	Optoisolated RS485 interface piggyback for 2-wire half-duplex connection with 9-Pin D-Sub connector	9927
CABLE-VM42	3 metre RS232 Serial Interface cable with RJ12 to 9-Pin D-Sub (female)	12383

Important: The VSBC-32 must be ordered with a memory module (DM60x) and a front-panel with integrated SI - piggyback module.

For OEM quantities, other FLASH memory configurations are available on request. A VSBC-32 with a 6U format is easily created by ordering the relevant SI-piggyback with a 6U format option. Please contact the nearest PEP sales office for more information.

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## **CXC** Overview

## VSBC-32

First introduced in 1990, PEP's Controller eXtension Connector (CXC) concept enables a mezzanine I/O extension according to the guidelines laid-down in the CXC specification.

PEP has named these mezzanine plugin units 'Controller eXtension Modules' (CXMs). These 96-pin CXMs are designed to operate with CXC-based host CPU modules which includes the VSBC-32.

Designed primarily to operate in harsh industrial environments, this versatile modularity provides not only a cost-effective engineering solution but also allows customers a near exhaustive selection of system configurations through a portfolio of over 30 CXMs providing analog, digital and other I/O extensions such as SCSI and fieldbus connection (High-speed PROFIBUS, CAN, LON and Interbus-S.) Hence, a feature of the VSBC-32 is that the 'raw' serial signals from the 'QUICC' SCC2, SCC3 and SCC4 channels, being internally wired to the CXC interface, may be used by dedicated signal translation modules.

Network interfacing is provided if required by ordering the relevant front-panel which comes complete with the appropriate SI-piggyback and serial port connectors. Naturally, to cater for those customers who merely wish to take advantage of the communication power and CXC capability that the VSBC-32 offers, blank front-panels without the networking options have been devised.

## **Real-Time Software Support**

## VSBC-32

With several real-time operating systems available, each targeting specific markets, PEP is able to support the most popular brands suitable for the majority of applications due to the open nature of the QUICC and its implementation on the VSBC-32.

#### **VxWorks**

Wind River's VxWorks distributed real-time operating system includes integrated networking facilities and a complete software development environment for Windows and UNIX hosts such as high-end PC and SUN Workstations.

Major features of VxWorks include a fast, multitasking kernel with preemptive scheduling and fast interrupt response, extensive intertask communications and synchronisation facilities, efficient UNIX-compatible memory manage-ment, multiprocessor facilities, a shell for user interface, symbolic and source level debugging capabilities, performance monitoring and an I/O file system.

#### **OS-9**

OS-9 is a flexible, modular real-time operating system for 680x0-based applications featuring a scalable architecture built around a powerful standalone microkernel, with ROMable extensions that can be dynamically loaded and linked to the system while it is up and running. OS-9 is available in different configurations, designed to provide the compact size and I/O support required. Embedded OS-9 is designed for FLASH or PROM-based applications; Disk-based OS-9 adds support for floppy, RAM disk, SCSI hard disk and tape units; Extended OS-9 adds TCP/

IP networking and NFS support. The *Ultra C* ANSI compiler represents advanced compiler technology for 680x0 microprocessors and is a complete implementation in accordance with the ANSI X3.159-1989 and POSIX standards. *FasTrak* provides graphical tools on UNIX-based workstations or Windows-based PCs.

#### **pSOSystem**

Integrated Systems' pSOSystem software provides a full featured runtime and development environment for embedded systems. The complete cross development environment enables developers to use UNIX workstations or PC compatible host systems running C and C++ language compilers, source language and target-level debuggers, a pSOS+ application simulator and visual debugging and profiling tools.

#### VRTX32

Spectra represents the first application of a client-server architecture to real-time and embedded software development. Its advanced open software backplane offers unparalleled productivity, convenience and flexibility in host-target connection.

## **Product Overview**

## VSBC-32

PEP's VSBC-32 combines high computational performance and low power consumption with excellent communication ability afforded by the Motorola 'QUICC' communication controller.

The 'QUICC' is a 32-bit high-performance communication controller which combines powerful peripheral functions with system integration and an on-chip 32-bit core. The core is essentially a 68020 processor operating at 25 MHz or 33 MHz without cache and achieves a computational performance that is approximately three times that of a 68302 running at 16 MHz. It has a communication performance that is approximately six times that of the 68302!

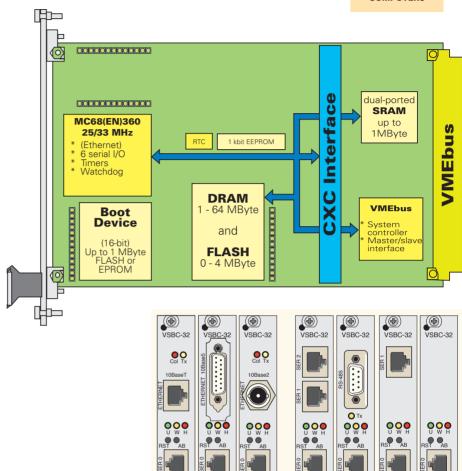
In addition, the 'QUICC' offers background debugging via the on-chip "Background Debug-Mode" which allows direct communication with the CPU core and VME DMA memory accesses are also controlled by the integrated on-chip memory controller.

When used together with PEP's CXC interface, the VSBC-32 is ideally suited for communication applications with up to 6 serial interfaces including LAN, WAN or fieldbuses (PROFIBUS, CAN, LON.)

The use of standard interfaces (VME and CXC) allows combination and customization using currently available off-the-shelf products.

The PEP VSBC-32 comprises a base module (with a choice of controller speed, Ethernet support and SRAM blocks), memory piggyback and SI-interface module. The complete package provides support for several popular real-time operating systems including: VxWorks, OS-9, VRTX, pSOS<sup>+</sup>, and others on request.





## I/O Extension

The illustrated front-panels show the possible connections of the SCC1 communications channel for Ethernet, RS232, RS485 or blank. These have been developed to adapt the usable multi-protocol serial channels of the MC68(EN)360 to the physical interfaces:

- ▶ Ethernet 10Base5
- ▶ Ethernet 10Base2
- ► Ethernet 10BaseT
- ► RS485 Optoisolated
- ▶ 2xRS232 Modem compatible
- ► 1xRS232 Optoisolated

An additional CXC module (CXM-SIO3) routes 2 or 3 of the available but unused serial interfaces to its front-panel allowing different physical connections (RS232, RS485, RS422).

This versatile modularity provides not only a cost-effective engineering solution but also allows customers a near exhaustive selection of system configurations through VME and CXC modules which provide analog, digital and other I/O extensions such as SCSI and fieldbus connections (PROFIBUS, CAN, LON and others on request).

## **Specifications**

## VSBC-32

#### **CPUs (Communication Controller)**

MC68360 @ 25 MHz MC68EN360 @ 33 MHz

#### Memory

1/4/8/16/32/64 MByte (32-bit access) DRAM<sup>†</sup>
1/4 MByte (32-bit access) FLASH<sup>†</sup>
256 kByte or 1 MByte (16-bit access) ROM or FLASH
256 kByte or 1 MByte dual-ported SRAM with data
retention via Goldcap
2 kbit serial EEPROM for applications

#### **Real-Time Clock**

V3021 with year, month, week, day, hour, min., sec.

#### Tick

Built-in on MC68(EN)360 providing a programmable periodic interrupt

### Timer

4x16, 2x32-bit resolution built-in timers on the MC68(EN)360

#### Time-Out

On-board BERR\* time-out fixed at 8µs with software enable/disable

#### Watchdog

Enabled by software with front-panel LED; generates RESET

#### Clocks

CPU clock: 25 MHz, 33 MHz
Communication clock: 24 MHz
VME/CXC clock: 16 MHz

All serial port baud-rate clocks may be configured individually by software

#### Interrupts

VMEbus IRQ1\* - IRQ7\* interrupts, enable/disable; SYSFAIL\* and ACFAIL\* handlers

#### **System Controller**

Single-level (BR3\*), FAIR, RWD (Release When Done); Automatic First-Slot Detection

VME and DP SRAM Read-Modify-Write cycle support

### Address Modifier

A24 Access Code : HEX 39/3A/3D/3E A16 Access Code : HEX 29/2D User Defined : HEX 10-17/18-1F

†Available on DM60x Memory Piggyback

#### Slave Functions

Dual-ported SRAM for VME; up to 16 software selectable VME base addresses VME Mailbox IRQ

#### CXC Interface

DIN 41612 (C), 96-pin, 3 NMSI ports, DMA

#### **VMEbus Interface**

DIN 41612 (C), 96-pin P1 connector A24/A16:D16/D8 master and slave

#### DMA

Two independent channels with 32-bit internal/external transfers

#### Networking

All Ethernet interfaces conform to IEEE 802-3 and are available on SI-xx piggybacks (only with 68EN360)

#### Serial-Interfaces

From MC68(EN)360 (ports SMC1 and SMC2) with standard RS232 configuration

### Power Consumption #

Typ. 3W for MC68360 @ 25 MHz Typ. 3.5W for MC68EN360 @ 33 MHz

#### Temperature

0°C to +70°C (standard) -40°C to +85°C (extended) -55°C to +85°C (storage)

#### Humidity

0 to 95% non-condensing

### **Weight / Dimensions**

260g (with 10BaseT and memory piggybacks) 100mm x 160mm 3U format; Single-slot (4HP)

### **Front-Panel Functions**

3 LEDs: red: Halt

yellow: Watchdog enabled green: General purpose user

2 Switches: AB: Abort function (NMI)

RST: Reset

Other LEDs showing Ethernet or RS485 activity are present depending on the version ordered

depending on the version ordered

# (with 4 MByte DRAM, 256 kByte SRAM and 1 MByte FLASH memory)

## **Features**

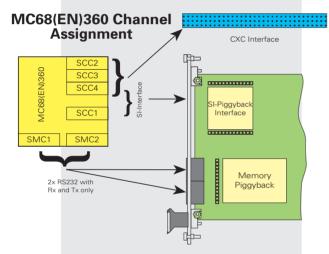
## VSBC-32

#### 68(EN)360

A 25/33 MHz full 32-bit CPU (CPU32+ core) with I/O and system controller providing all the necessary interfaces, timers and clocks etc. in addition to the DRAM memory controller.

#### Serial Channels

Six are provided by the QUICC - Two SMC channels are ported to the front panel and the remaining four SCC channels may be optionally configured as shown.



Each VSBC-32 comes complete with 2 RS232 serial interfaces provided by the SMC1 and SMC2 channels of the QUICC controller ported to the lower half of the front panel. The SCC1 channel of the QUICC provides the interface to one of the available SI-x piggybacks. All other channels (SCC2, SCC3 and SCC4) of the QUICC are ported to the CXC interface except for the SI-PB232 piggyback which has additional control provided by the SCC4 channel.

### **CXC-Interface**

The 96-pin interface allows other I/O possibilities to be realized by utilising PEP's plugin cards with digital, analog, serial and SCSI interfaces. Fieldbus controllers complete the interface range.

#### **Ethernet Interface**

Three different SI piggybacks equipped with all the associated control logic are available for the 'EN' version providing 10Base2, 10Base5 or 10BaseT interfaces.

#### **RS232 Serial Interfaces**

2 SI-piggybacks provide MODEM compatible RS232 communication.

#### **RS485 Fieldbus Interfaces**

This SI-piggyback provides is a fully optoisolated RS485 interface piggyback with a 9-pin D-Sub connector.

#### **DMA Channels**

2 independent channels are provided by the QUICC chip for use by applications requiring DMA transfer between VMEbus, CXC-modules, DRAM, FLASH memory and dual-ported SRAM.

#### DRAM/FLASH

This memory, complete with a 32 bit-wide access bus is placed on a piggyback with addressing capability for up to two memory banks of 64 MByte each. The on-board programmable FLASH memory allows the user to produce low-cost upgrades by over-writing existing stored data and may also be configured as a boot device.

#### SRAM

This is a dual-ported battery-backed (Goldcap) memory area with a 16 bit- wide access bus. Users of the VMEbus and CPU both have access to this memory.

#### **EEPROM**

A 2 kbit EEPROM is provided on-board; 1 kbit has been pre-programmed with PEP production data leaving the remaining available space for user application code.

#### Boot ROM/FLASH

2 DIL sockets supporting up to 1 MByte of 16-bit ROM/FLASH memory are available for use as main memory or as a boot device if the FLASH appearing on the DM60x piggyback is not required.