Modular Computers®

CPCI Backplane Manual

PRODUCT DOCUMENTATION

PD05

CP3-BP8-M-RIO

Reference ID: 24229 PD05

Revision: 01

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The product described in this manual is in compliance with all applied CE standards.

Revision History

Manual/Product Title:	CPCI Backplane Manual: Product Documentation: CP3-BP8-M-RIO
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Rev. Index	Brief Description of Changes	Date of Issue
01	Initial Issue	Mar. 01, 2002

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

1. Introduction

The specific product description provided with this product documentation is part of the PEP's CPCI Backplane manual. For further information, in particular regarding general details as well as safety and warranty statements, refer to the CPCI Backplane Manual, ID 24229.

2. CP3-BP8-M-RIO DIN Type M RIO Backplane

The main features of the 3U, 8-slot, DIN type M backplane CP3-BP8-M-RIO, which is designed for rear I/O applications, are described in the following table:

Table 1: Distinctive Features of Backplane CP3-BP8-M-RIO

Feature	Specification
Form Factor	3U
Size	197.12*128.7 mm
Number of Slots	8
Bus Resolution	32 bits: slots 1 to 8
Bus Frequency	33MHz: slots 1 to 8
Rear I/O Connectivity	P2 on slots 1 to 8
Hot-Swap Capability	Yes
Power Supply Connector	DIN type M
Redundant Power Supply	—
Flexible Grounding Option	Yes
Fan Connector	Yes
MSD Connector	Yes
Power LED Connector	Yes
PS-ON Connector	Yes
Reset Function Connector	Yes

3. Board Layout

Figure 1: CP3-BP8-M-RIO Board Layout (Front)

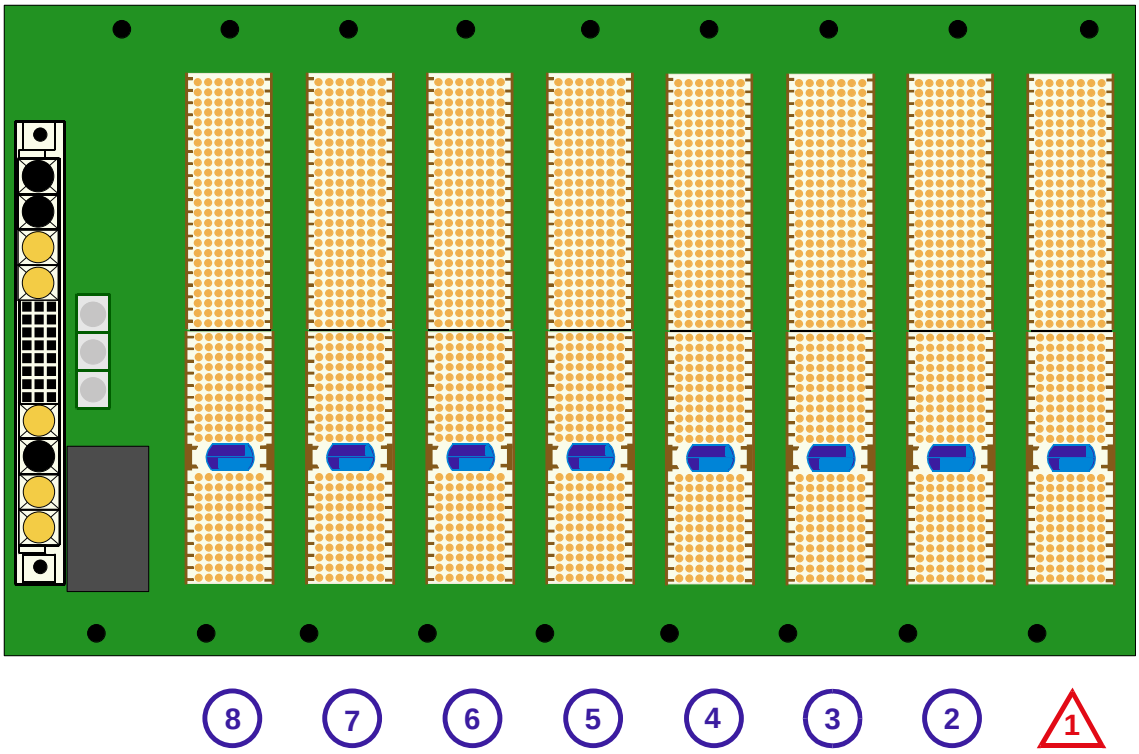
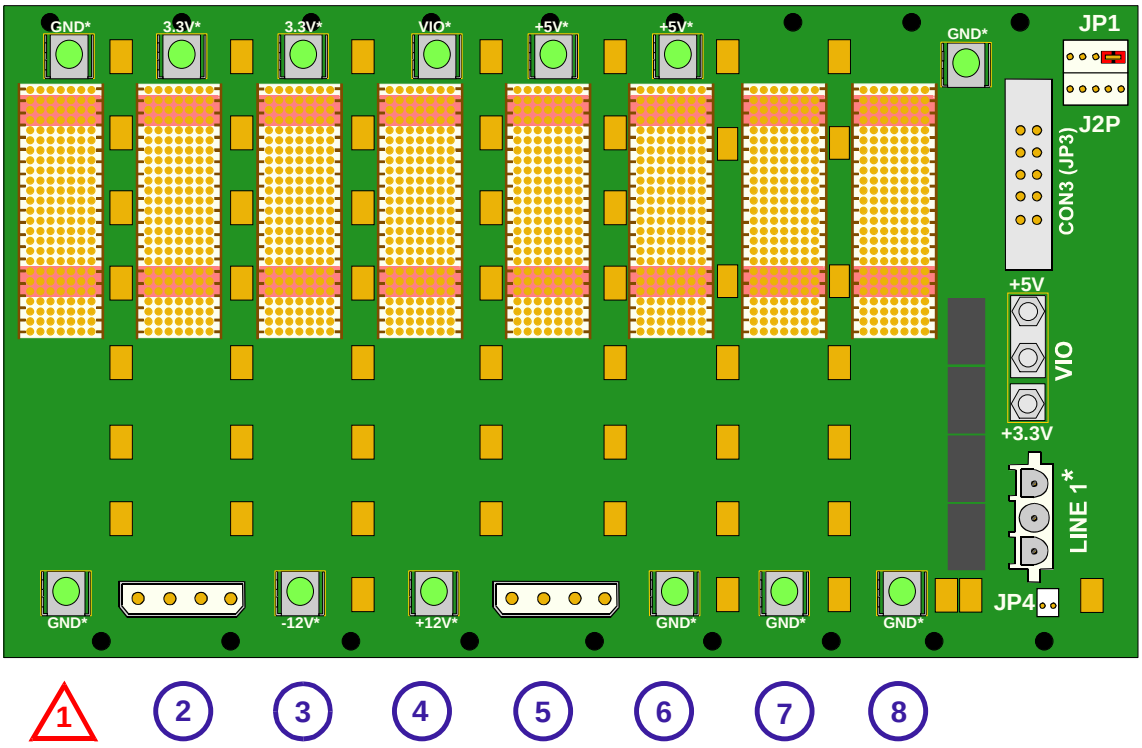


Figure 2: CP3-BP8-M-RIO Board Layout (Reverse)



Components marked with an asterisk (*) are optionally available.

4. Signalling Environment

4.1 V(I/O) Setting

The backplane provides a block of three high-current terminals (designated as V(I/O)) for connecting V(I/O) to either the +5V or +3.3V power supply. V(I/O) must be connected either to the +5V or the +3.3V input power. It is the responsibility of the system integrator to ensure that the required signalling voltage is implemented and that the backplane P1 connector coding corresponds to the implemented signalling voltage.

Warning!

Using both 3.3V and 5V boards within the same system may result in damage to your equipment. Please note that the presence of only one 5V board determines a 5V signalling environment. The default setting is 5V.

4.2 P1 Connector Coding for V(I/O)

The CompactPCI Specification foresees coding of the P1 connector to correspond to the signalling environment of the PCI bus. For this reason, only boards with universal or the corresponding coding can be physically inserted into the backplane. PEP's factory default setting for V(I/O) is +5V and male, 1567 code, brilliant blue coding keys are used.

Warning!

Using boards with an inadequate signalling voltage may result in damage to your equipment. Therefore, when changing the signalling environment from 5V to 3.3V or vice versa, it is mandatory that proper coding keys are used (refer to chapter 3 of the CPCI Backplane Manual, ID 24229, for details).

5. Interfaces

5.1 Line Connector

The power supply to the backplane is connected by means of the 3-pole Mate-N-Lok connector marked ”LINE1” on the reverse side of the backplane.

Figure 3: Orientation and Pinouts of CP3-BP8-M-RIO Connector LINE1

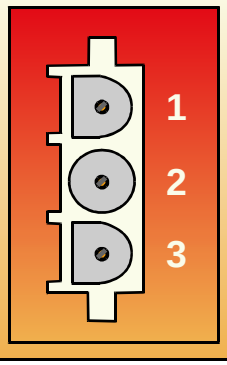


Table 2: Pinouts of CP3-BP8-M-RIO Connector LINE1

Pin	Function
1	N or -DC
2	L or +DC
3	PE

5.2 Power Supply Connector

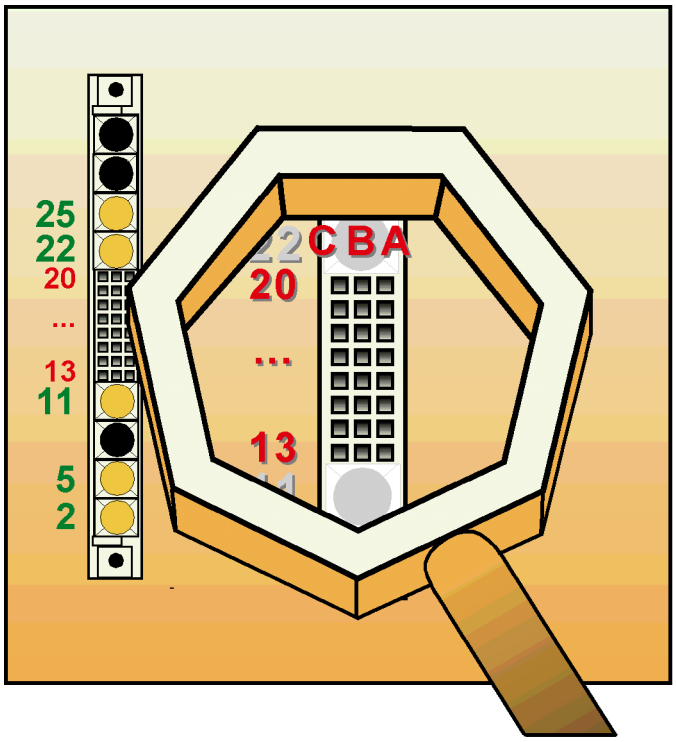


Figure 4: Orientation and Pinouts of CP3-BP8-M-RIO DIN type M Power Supply Connector

The input voltages to the power supply unit and the V1 ... V4 output voltages from the power supply unit to the backplane are connected via a 32-position, DIN type M, female power supply connector.

Warning!

System integrators must ensure that only power supplies which comply with the pinout as provided in Table 3 are used with this connector!

Pins B2, B5, B28, and B31 do not comply with the CompactPCI Power Interface Specification.

Table 3: DIN Type M Connector Pinout

Pin	Function	Pin	Function	Pin	Function
		B.2	L or +DC		
		B.5	N or -DC		
		B.8	No Pin Loaded		
		B.11	PE		
C.13	EN#	B.13	+3.3V	A.13	Spare
C.14	DEG#	B.14	+3.3V	A.14	INH#
C.15	FAL#	B.15	+3.3V	A.15	ISH
C.16	+3.3V	B.16	+3.3V	A.16	5V Sense -
C.17	+3.3V	B.17	+3.3V	A.17	5V Sense +
C.18	+3.3V	B.18	+3.3V	A.18	+3.3V
C.19	+12V	B.19	+12V	A.19	+12V
C.20	-12V	B.20	-12V	A.20	-12V
		B.22	+5V		
		B.25	GND		
		B.28	No Pin Loaded		
		B.31	No Pin Loaded		
L = line, N = neutral, PE = protective earth;					

5.3 Fan Connector

The backplane is equipped with the lockable Molex male connector JP4 for the connection of fans to the 12V power supply of the bus.

Figure 5: Orientation and Pinouts of CP3-BP8-M-RIO Connector JP4

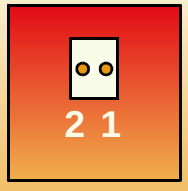


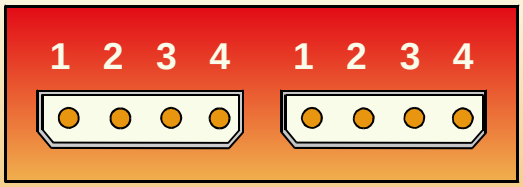
Table 4: Pinouts of CP3-BP8-M-RIO Connector JP4

Pin	Function
1	GND
2	+12V

5.4 MSD Connectors

Two 4-pole Molex male connectors are equipped on the backplane for the connection of mass storage devices (drives) to the +5V/+12V power supply of the bus.

Figure 6: Orientation and Pinouts of CP3-BP8-M-RIO MSD Connectors



Legend:

These connectors are available optionally.

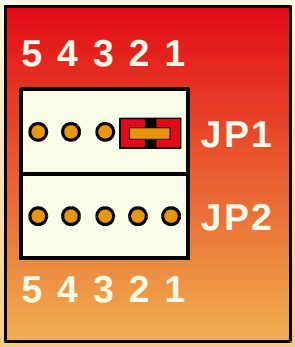
Table 5: Pinouts of CP3-BP8-M-RIO MSD Connector

Pin	Function
1	+12V
2	GND
3	GND
4	+5V

5.5 Auxiliary Signal Connectors

The connection of the auxiliary signals is accomplished by means of the two 5-pole Molex male connectors JP1 and JP2 as well as the 10-pole LPV male connector JP3. The LPV connector JP3 provides the same signals as JP1 and JP2 taken together.

Figure 7: Orientation and Pinouts of CP3-BP8-M-RIO Connectors JP1 and JP2



View from reverse side

Table 6: Pinouts of CP3-BP8-M-RIO Connectors JP1 and JP2

Pin		Function
JP1	1	EN#
	2	GND
	3	INH#
	4	GND
	5	N/C
JP2	1	GND
	2	+5V
	3	FAL#
	4	DEG#
	5	PRST#

Figure 8: Orientation and Pinouts of CP3-BP8-M-RIO Connector JP3

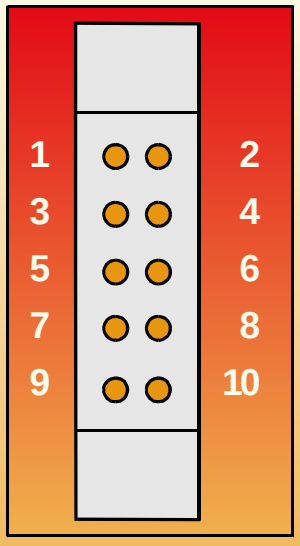


Table 7: Pinouts of CP3-BP8-M-RIO Connector JP3

Pin	Function
1	GND
2	EN#
3	GND
4	INH#
5	DEG#
6	FAL#
7	GND
8	PRST#
9	GND
10	+5V

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