Modular Computers®

CPCI Backplane Manual

PRODUCT DOCUMENTATION

PD12

CP6-BP8-P47-STD-SL

Reference ID: 24229 PD12

Revision: 01

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The product described in this manual is in compliance with all applied CE standards.

Revision History

Manual/Product Title:	CPCI Backplane Manual: Product Documentation: CP6-BP8-P47-STD-SL	
Reference ID:	24229 PD12	
Rev. Index	Brief Description of Changes	Date of Issue
01	Initial Issue	Mar. 01, 2002

Imprint

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

1. Introduction

The specific product description provided with this product documentation is part of the PEP's CPCI Backplane manual. For further information, in particular regarding general details as well as safety and warranty statements, refer to the CPCI Backplane Manual, ID 24229.

2. CP6-BP8-P47-STD-SL Positronic Type Backplane

The main features of the 6U, 8-slot, Positronic type system slot left backplane CP6-BP8-P47-STD-SL are described in the following table:

Table 1: Distinctive Features of Backplane CP6-BP8-P47-STD-SL

Feature	Specification
Form Factor	6U
Size	202.2*262.05 mm
Number of Slots	8 (System slot is on the left side of this backplane)
Bus Resolution	64 bits
Bus Frequency	33MHz
Rear I/O Connectivity	P3 to P5 on all slots
Hot-Swap Capability	Yes
Power Supply Connectors	Positronic PCIH47, 47-contact (Power supply connectors are on the right side of this backplane.)
Redundant Power Supply	Yes
System Management	Yes
Flexible Grounding Option	Yes
Fan Connector	Yes
MSD Connector	Yes
Power LED	Yes
PS-ON Connector	Yes
Reset Function Connector	Yes

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3. Board Layout

Figure 1: CP6-BP8-P47-STD-SL Board Layout (Front)

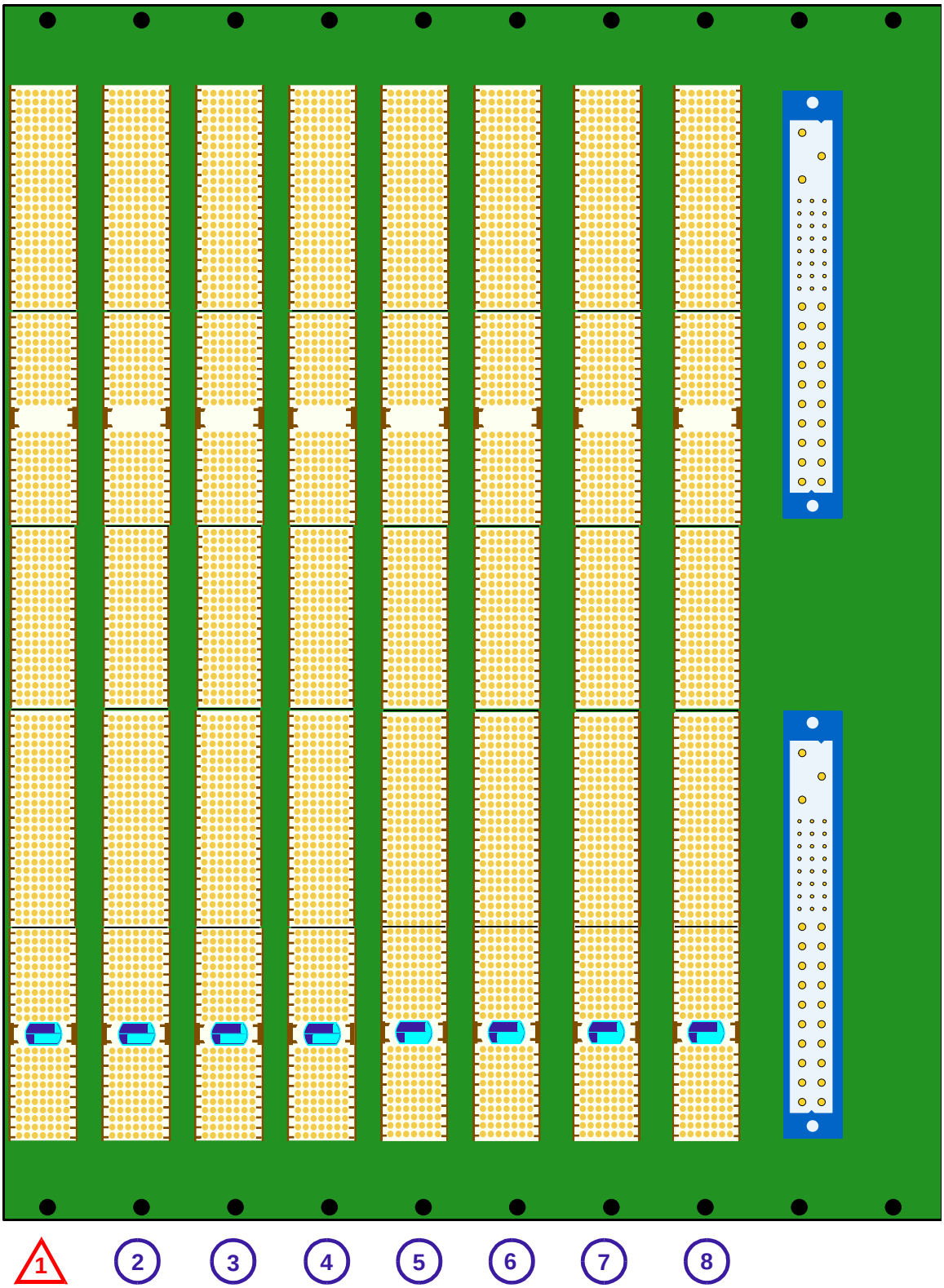

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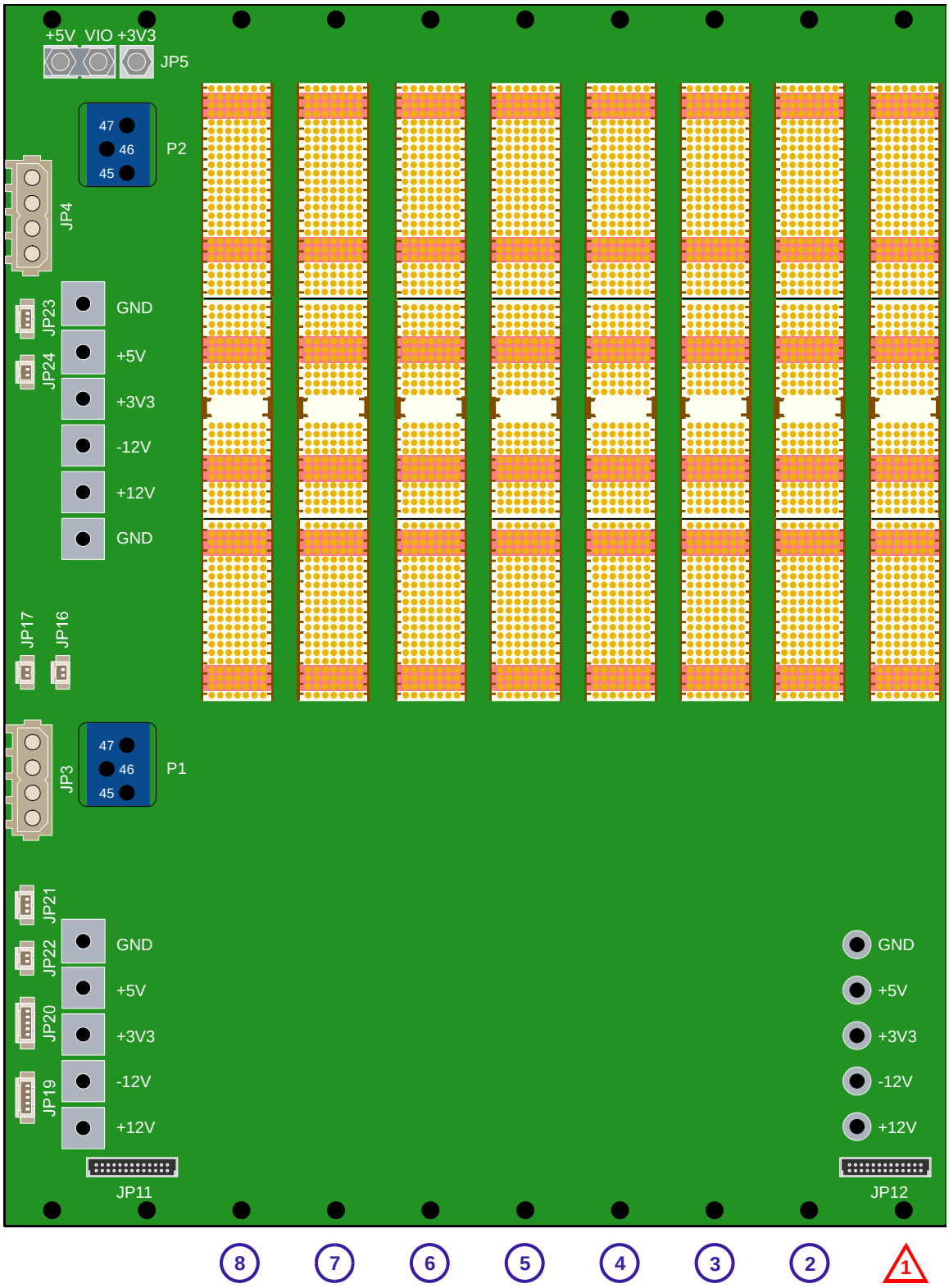
Figure 2: CP6-BP8-P47-STD-SL Board Layout (Reverse)



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4. Signalling Environment

4.1 V(I/O) Setting

There is one block of three high-current terminals (designated as V(I/O)) for connecting V(I/O) to either the +5V or +3.3V power supply. V(I/O) must be connected either to the +5V or the +3.3V input power. It is the responsibility of the system integrator to ensure that the required signalling voltage is implemented and that the backplane P1 connector coding corresponds to the implemented signalling voltage.

Warning!

Using both 3.3V and 5V boards within the same backplane segment may result in damage to your equipment. Please note that the presence of only one 5V board determines a 5V signalling environment. The default setting is 5V.

4.2 P1 Connector Coding for V(I/O)

The CompactPCI Specification foresees coding of the P1 connector to correspond to the signalling environment of the PCI bus. For this reason, only boards with universal or the corresponding coding can be physically inserted into the backplane. PEP's factory default setting for V(I/O) is +5V and male, 1567 code, brilliant blue coding keys are used.

Warning!

Using boards with an inadequate signalling voltage may result in damage to your equipment. Therefore, when changing the signalling environment from 5V to 3.3V or vice versa, it is mandatory that proper coding keys are used (refer to chapter 3 of the CPCI Backplane Manual, ID 24229, for details).

5. Interfaces

5.1 Power

This backplane is designed to accommodate several different schemes for power input. Pluggable 3U and 6U power supplies can be used as well as non-pluggable power supplies. In addition it is possible to extend the backplane's power busses for adding additional power supplies. Appropriate provisions have been made on both the left side as well as the right side of the backplane for power bus extension

5.1.1 Terminal Type Power Input

Both bolt type terminals and Faston/M4 type terminals can be provided for inputting DC power to this backplane. These terminals are primarily designed for extending the DC power busses, but they can also be used with non-pluggable power supplies for providing primary DC power input. Refer to Figure 2 for terminal locations.

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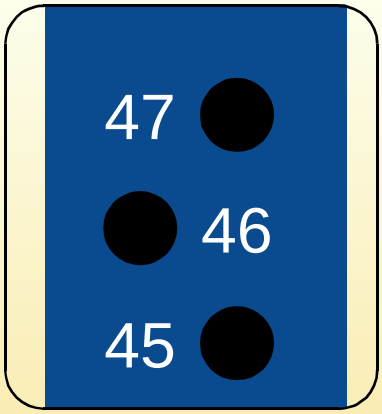
5.1.2 Pluggable Power Supply and Line Input

The V1 ... V4 output voltages from the power supply unit to the backplane are connected via a 47-contact, female, Positronic type power supply connector.

The main power supply input power is connected directly to pins 45, 46, and 47 of the power supply connector. The is accomplished by means of a single, closed barrel pass-through contact for each pin via the reverse side of the backplane.

Figure 3: Orientation and Pinouts of CP6-BP8-P47-STD-SL Positronic 47-pin Connector



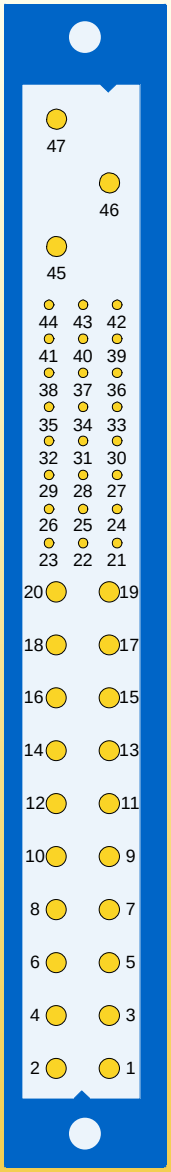


Table 2: Pinouts of CP3-BP8-P47-RIO 47-pin Connector

Pin	Function
45	PE or GND
46	N or +DC
47	L or -DC

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Table 3: Positronic 47-Pin Connector Pinout

PIN	SIGNAL NAME	DESCRIPTION	PIN	SIGNAL NAME	DESCRIPTION
1 - 4	V1	V1 OUTPUT (+5V)	32	V2ADJ	V2 ADJUST
5 - 12	RTN	V1 and V2 RETURN	33	V2 SENSE	V2 REMOTE SENSE
13 - 18	V2	V2 OUTPUT (+3.3V)	34	S RTN	SENSE RETURN
19	RTN	V3 RETURN	35	V1 SHARE	V1 CURRENT SHARE
20	V3	V3 OUTPUT (+12V)	36	V3 SENSE	V3 REMOTE SENSE
21	V4	V4 OUTPUT (-12V)	37	IMPB_SCL	IMPB SYS CLOCK
22	RTN	SIGNAL RETURN	38	DEG#	DEGRADE SIGNAL
23	RESERVED	RESERVED	39	INH#	INHIBIT
24	RTN	V4 RETURN	40	IMPB_SDA	IMPB SYS DATA
25	GA0	GA BIT 0	41	V2 SHARE	V2 CURRENT SHARE
26	RESERVED	RESERVED	42	FAL#	FAIL SIGNAL
27	EN#	ENABLE	43	IMPB_PWR	IMPB POWER
28	GA1	GA BIT 1	44	V3 SHARE	V3 CURRENT SHARE
29	NC	NOT CONNECTED	45	CGND	CHASSIS GROUND
30	V1SENSE	V1 REMOTE SENSE	46	ACN / +DC IN	AC INPUT NEUTRAL / +DC INPUT
31	GA2	GA BIT 2	47	ACL / -DC IN	AC INPUT LINE / +DC INPUT

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5.2 Fan Connectors

The backplane is equipped with four connectors for supplying power for fan(s) and for connecting a fan speed control device. JP21/23 (FAN1/2), are 3-contact male connectors which supply +12V for fan operation as well as the possibility to connect to a speed control device for regulating air flow within the system sub-rack. JP22/24 (NTC1/2), are 2-contact male connectors which provide a separate connection for a speed control device and are designed to be used in conjunction with JP21/23.

For fans that have their own speed control or where no control is required, pins 1 and 2 of JP21/23 can be used. For external speed control of fans, pins 2 and 3 of JP21/23 and pins 1 and 2 of JP22/24 are used. Pin 3 of JP21/23 and pin 2 of JP22/24 are connected internally on the board side to each other.

External air flow regulation can be accomplished using a negative thermal coefficient (NTC) device connected to JP22/24

Figure 4: Orientation and Pinouts of CP6-BP8-P47-STD-SL Connectors JP21/23 and JP22/24

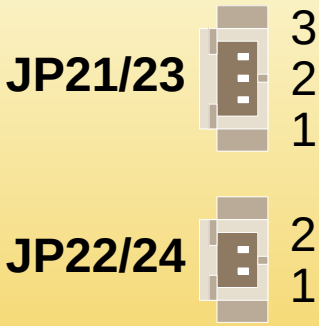

Table 4: Pinout of CP6-BP8-P47-STD-SL JP21/23 Connector

Pin	Function
1	GND
2	+12V
3	NTC1/2

Table 5: Pinout of CP6-BP8-P47-STD-SL JP22/24 Connector

Pin	Function
1	GND
2	NTC1/2

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5.3 Auxiliary Connectors and Signals

There are two, two-contact, male auxiliary connectors, JP16 and JP17, available on this backplane.

JP16 and JP17 make the signal lines, PRST and INH# respectively, available for external switches to either invoke a system reset or to switch the power supply on or off.

Figure 5: Orientation and Pinouts of CP6-BP8-P47-STD-SL Connectors JP16 and JP17

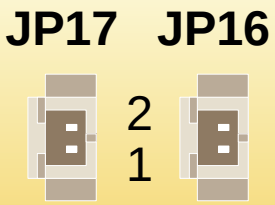

Table 6: Pinouts of CP6-BP8-P47-STD-SL Connectors JP16 and JP17

Pin		Function
JP16	1	GND
	2	PRST
JP17	1	GND
	2	INH#

5.4 System Management Connectors JP19 and JP20

Two five-contact male system management bus (IPMB0/1) connectors, JP19/20, are provided for external interfacing to this bus.

Figure 6: Orientation and Pinout of the CP6-BP8-P47-STD-SL IMPB0/1 Connectors JP19/20

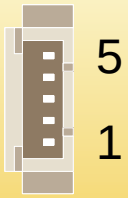

Table 7: Pinout of CP6-BP8-P47-STD-SL IMPB0/1 Connectors JP19/20

Pin	Function
1	IMPB0_SCL / IMPB1_SCL
2	GND
3	IMPB0_SDA / IMPB1_SDA
4	IMPB_PWR / V
5	SMB_Alert *

** JP20 only*

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5.5 System Monitor and Control Connectors JP11 and JP12

This backplane is provided with two connectors for system monitor and control signal interfacing to external devices. Both are 26-contact, male, double pin-row connectors, and have the same signal pinout configuration. The system management bus (IPMB0), the power supply monitor and control signals, and push button reset (PRST#) signal are all implemented on these connectors.

Figure 7: Orientation and Pinout of the CP6-BP8-P47-STD-SL SMC Connectors JP11 and JP12

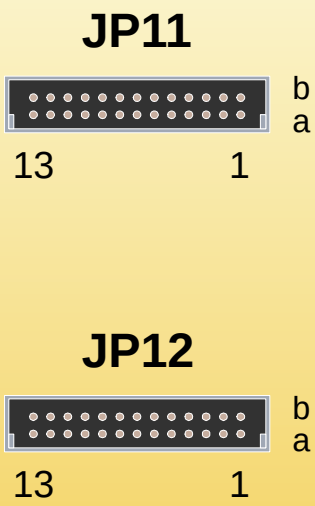

Table 8: Pinout of CP6-BP8-P47-STD-SL SMC Connectors JP11 and JP12

Pin	Function	
	Pin Row A	Pin Row B
1	IMPB0_SCL	GND
2	IMPB0_SDA	IMPB0_PWR
3	N/C	GND
4	N/C	GND
5	N/C	GND
6	INH#	GND
7	FAL#	DEG#
8	PRST#	GND
9	GND	V1 SENSE (+5V)
10	V2 SENSE (+3.3V)	SENSE RTN
11	V3 SENSE (+12V)	GND
12	V1 SHARE (+5V)	V2 SHARE (+3.3V)
13	V3 SHARE (+12V)	GND

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5.6 MSD Connectors

Two 4-pole Molex female connectors, JP3 and JP4, are equipped on the backplane for the connection of mass storage devices (drives) to the +5V/+12V power supply of the bus.

Figure 8: Orientation and Pinouts of CP6-BP8-P47-STD-SL Connectors JP3 and JP4

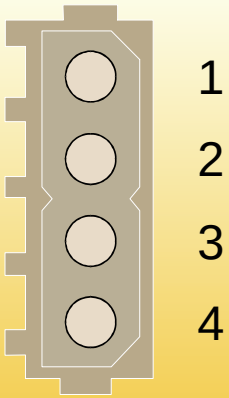

Table 9: Pinouts of CP6-BP8-P47-STD-SL Connectors JP3 and JP4

Pin	Function
1	+12V
2	GND
3	GND
4	+5V

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