

CPCI Backplane Manual

PRODUCT DOCUMENTATION

PD15 CP3-BP2-PB-RIO

Reference ID: 24229 PD15

Revision: 01

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The product described in this manual is in compliance with all applied CE standards.



Revision History

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Rev. Index	Brief Description of Changes	Date of Issue
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Imprint

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH.**



1. CPCI Backplane Introduction

The specific product description provided with this product documentation is part of the PEP's CPCI Backplane manual. For further information, in particular regarding general details as well as safety and warranty statements, refer to the CPCI Backplane Manual, ID 24229.

2. CP3-BP2-PB-RIO Power Bar Backplane

The main features of the 3U, 2-slot, power bar backplane CP3-BP2-PB-RIO, which is designed for rear I/O applications, are described in the following table:

Table 1: Distinctive Features of Backplane CP3-BP2-PB-RIO

Feature	Specification
Form Factor	3U
Size	202.2*128.7 mm
Number of Slots	2
Bus Resolution	32 bits: slots 1 and 2
Bus Frequency	33 or 66 MHz: slots 1 and 2
Rear I/O Connectivity	P2 on slots 1 and 2
Hot-Swap Capability	Yes
Power Supply Connector	5 power bar terminals, M3 lugs
Redundant Power Supply	Supported
Flexible Grounding Option	Yes
Fan Connector	-
MSD Connector	-
PS-ON Connector	-
Reset Function Connector	-
IPMB Extension Connector	-
System MON-CTRL Connector	Yes

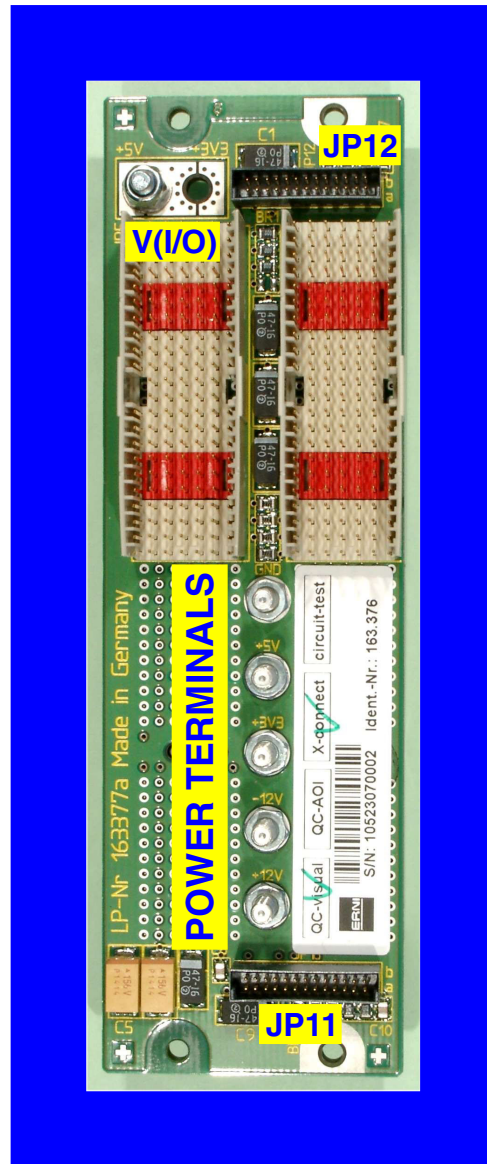
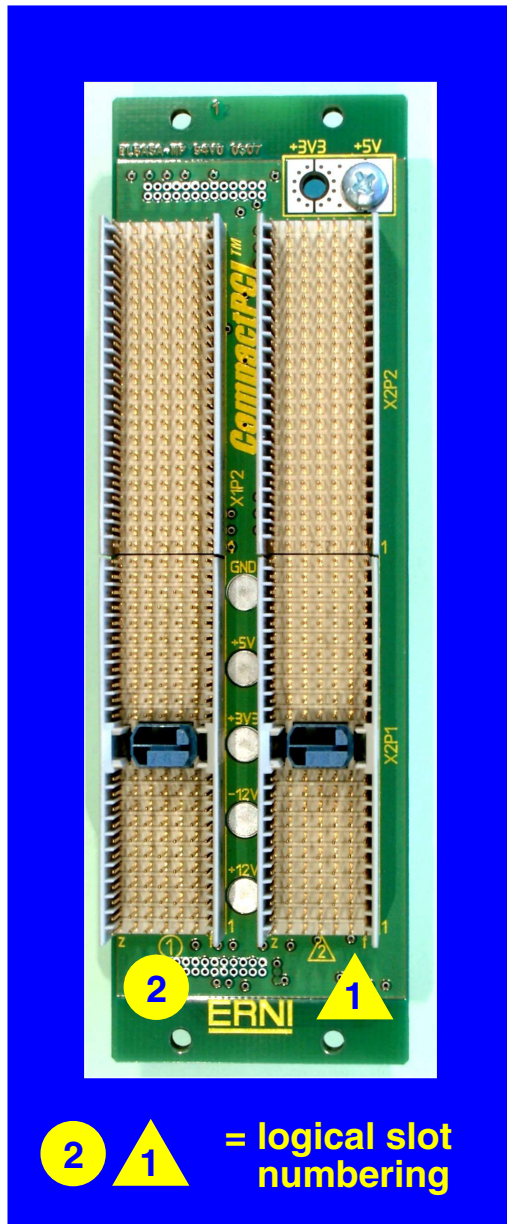


3. Board Layout

The following figures illustrate the layout of the board components of the CP3-BP2-PB-RIO-backplane.

Figure 1: CP3-BP2-PB-RIO Board Layout (Front)

Figure 2: CP3-BP2-PB-RIO Board Layout (Reverse)



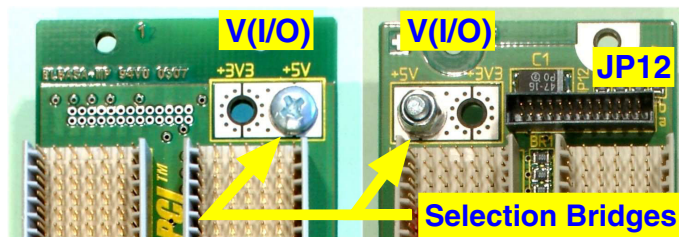


4. Signalling Environment

4.1 V(I/O) Setting

The backplane provides high-current selection capability (designated as V(I/O)) for connecting V(I/O) to either the +5V or +3.3V power supply. V(I/O) must be connected either to the +5V or the +3.3V input power. Selection is accomplished by installation of an M3 bolt in either one or the other of the two holes provided for this purpose. The following figure illustrates how a selection of +5V V(I/O) is achieved.

Figure 3: Selection of +5V V(I/O)



It is the responsibility of the system integrator to ensure that the required signalling voltage is implemented and that the backplane P1 connector coding corresponds to the implemented signalling voltage.



Warning!

Using both 3.3V and 5V boards within the same system may result in damage to your equipment. Please note that the presence of only one 5V board determines a 5V signalling environment. The default setting is 5V.

4.2 P1 Connector Coding for V(I/O)

The CompactPCI Specification foresees coding of the P1 connector to correspond to the signalling environment of the PCI bus. For this reason, only boards with universal or the corresponding coding can be physically inserted into the backplane. The factory default setting for V(I/O) is +5V and male, 1567 code, brilliant blue coding keys are used.



Warning!

Using boards with an inadequate signalling voltage may result in damage to your equipment. Therefore, when changing the signalling environment from 5V to 3.3V or vice versa, it is mandatory that proper coding keys are used (refer to chapter 3 of the CPCI Backplane Manual, ID 24229, for details).



5. Interfaces

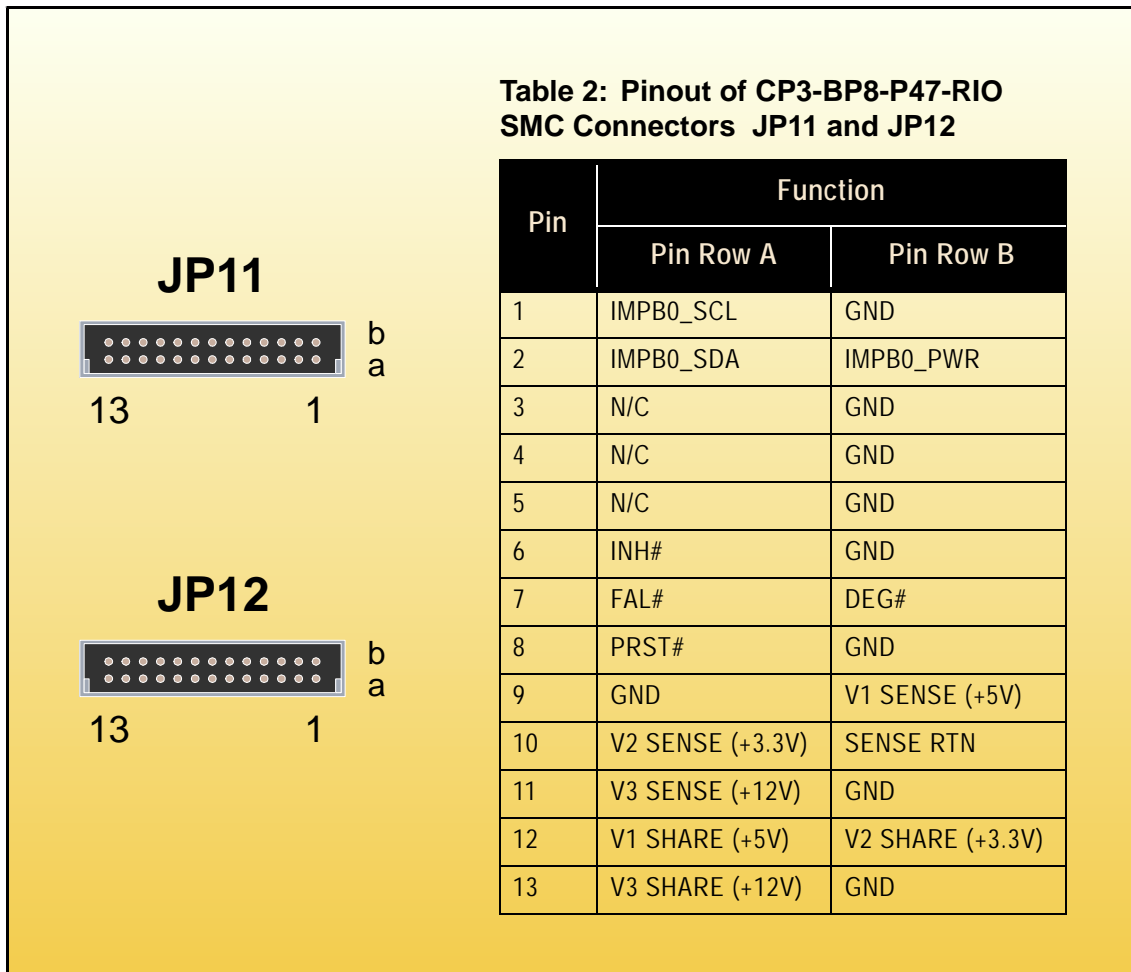
5.1 Power Supply Input

The V1 ... V4 output voltages from the power supply unit to the backplane are connected via power bar elements to the respective supply terminals of the power distribution backplane and the CP3-BP2-PB-RIO backplane. The power bars themselves are specifically designed to fit the backplane raster and allow additional backplanes to be integrated into a customized designed system to satisfy almost any application requirements.

5.2 System Monitor and Control Connectors JP11 and JP12

This backplane is provided with two connectors for system monitor and control signal interfacing to external devices. Both are 26-contact, male, double pin-row connectors, and have the same signal pinout configuration. The system management bus (IPMB0), the power supply monitor and control signals, and push button reset (PRST#) signal are all implemented on these connectors.

Figure 4: Orientation and Pinout of the CP3-BP2-PB-RIO SMC Connectors JP11 and JP12



**Note...**

The signal pinout assignment is a function of the power supply actually utilized with this backplane. Refer to the corresponding power supply documentation for the applicable signal pinout.

6. Optional System Configurations

6.1 Power Supply Options

The design of this backplane allows for several different power supply options:

1. The default configuration of a single compatible pluggable power supply.
2. Addition of compatible pluggable power supplies installed either to the left or right of the backplane.

Option 1 is the standard configuration which requires the integration of a single CP-ADAP-P47-PB (3U or 6U) power bar adapter.

Option 2 can be achieved through the use of power bar adapter boards which can be mounted either to the left or right of the backplane. These boards which accommodate pluggable power supplies are connected to the backplane terminals through the use of power bars. In addition, the system monitor and control signals can be extended via JP11 or JP12 to the power supply adapter boards using appropriate cabling. This configuration allows for additional power supplies to be added which satisfy system requirements such as redundancy, power sharing, or simply increasing available power.

6.2 System Addon Options

The CP3-BP2-PB-RIO backplane is designed to allow the installation of backplane(s) to the left or right of it in a sub-rack and at the same time maintaining the slot raster. This feature makes it possible to add (an) additional backplane(s) using appropriate hardware for accommodating multiple system configurations in one sub-rack.



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