Modular Computers®

CPCI Backplane Manual

PRODUCT DOCUMENTATION

PD18

CP6-BP4-PB-RIO

Reference ID: 24229 PD18

Revision: 01

Issued: August 29, 2003

The product described in this manual is in compliance with all applied CE standards.

Revision History

Manual/Product Title:	CPCI Backplane Manual: Product Documentation: CP6-BP4-PB-RIO
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Rev. Index	Brief Description of Changes	Date of Issue
01	Initial Issue	Aug. 29, 2003

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DISCLAIMER:

PEP Modular Computers GmbH rejects any liability for the correctness and completeness of this manual as well as its suitability for any particular purpose.

This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

1. Introduction

The specific product description provided with this product documentation is part of the PEP's CPCI Backplane manual. For further information, in particular regarding general details as well as safety and warranty statements, refer to the CPCI Backplane Manual, ID 24229.

2. CP6-BP4-PB-RIO Power Bar Backplane

The main features of the 6U, 4-slot, power bar backplane CP6-BP4-PB-RIO are described in the following table:

Table 1: Distinctive Features of Backplane CP6-BP4-PB-RIO

Feature	Specification
Form Factor	6U
Size	95.5*262.05 mm
Number of Slots	4
Bus Resolution	64 bits
Bus Frequency	33 or 66MHz
Rear I/O Connectivity	P3 to P5 on all slots
Hot-Swap Capability	Yes
Power Supply Connector	11 power bar terminals, M3 lugs
Redundant Power Supply	–
System Management	Optional
Flexible Grounding Option	Yes
Fan Connector	Optional
MSD Connector	Optional
Power LED	–
PS-ON Connector	Yes
System MON-CTRL Connector	Yes

3. Board Layout

Figure 1: CP6-BP4-PB-RIO Board Layout (Front)

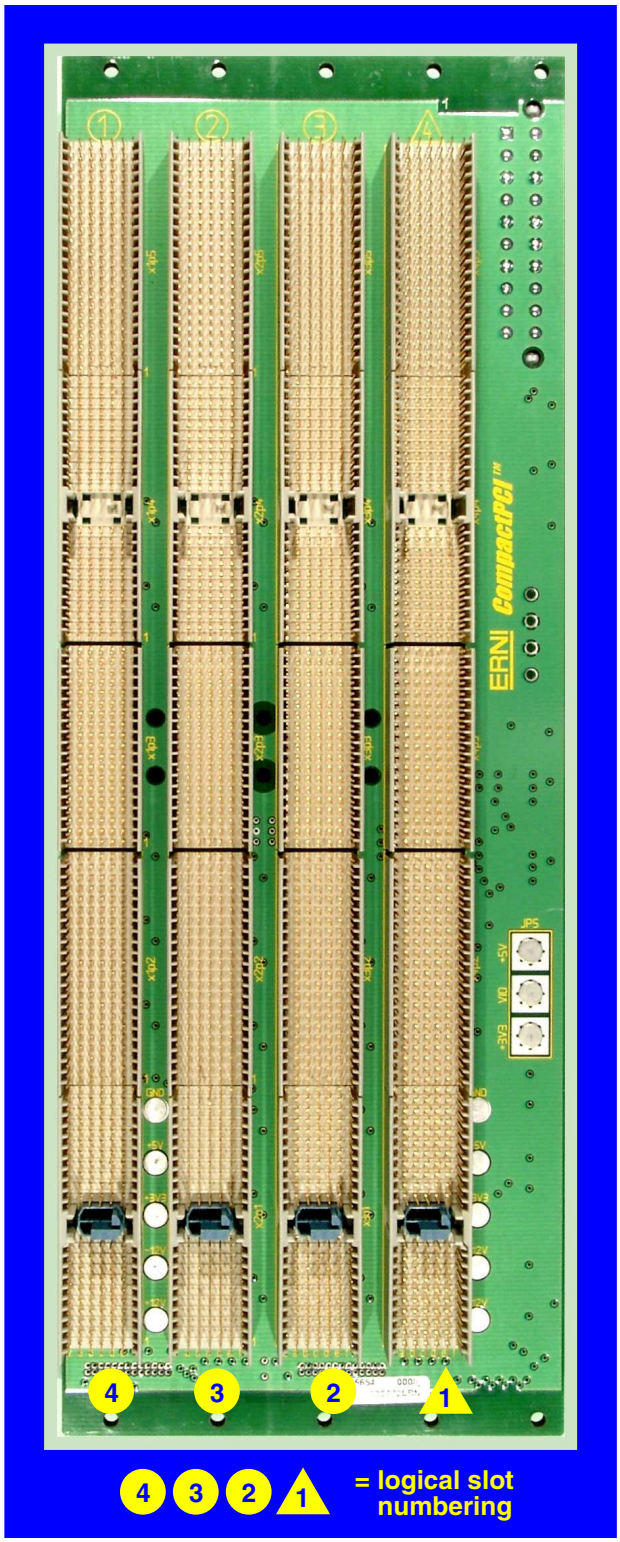
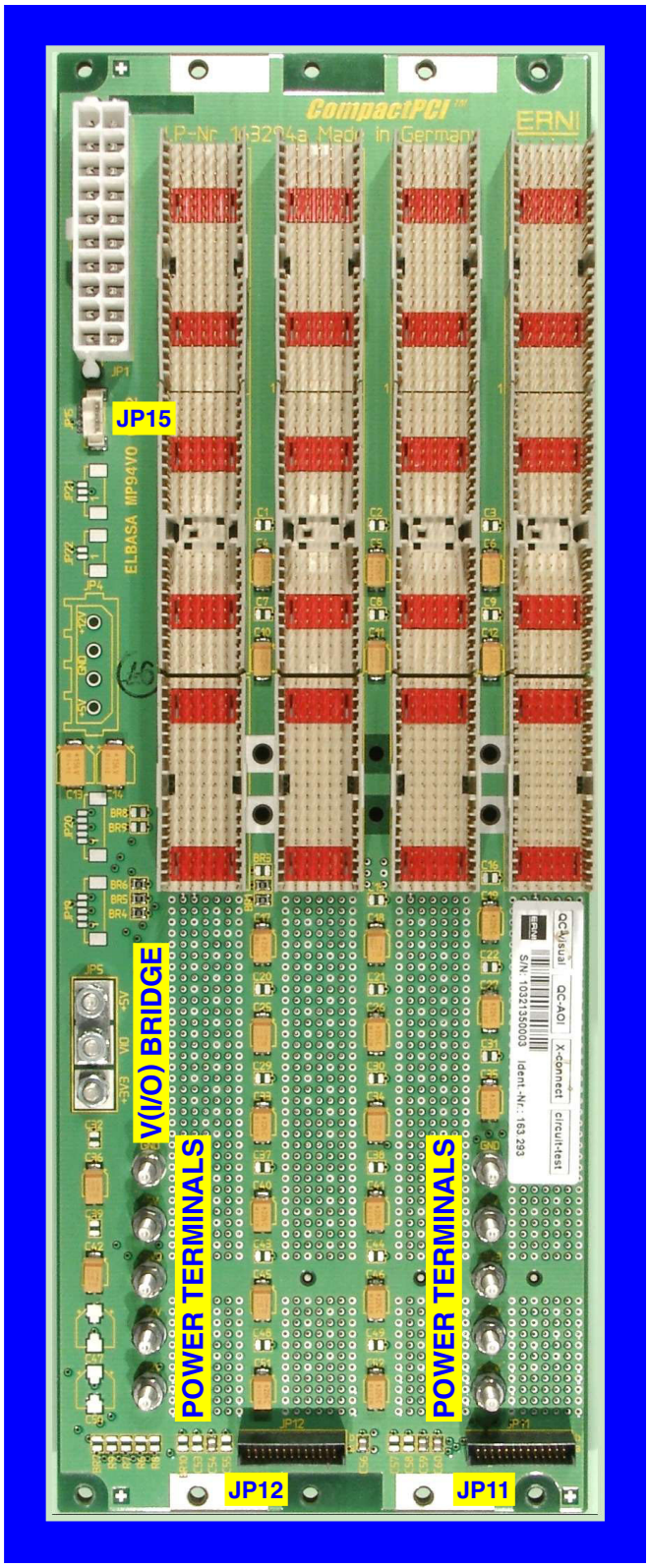


Figure 2: CP6-BP4-PB-RIO Board Layout (Reverse)



4. Signalling Environment

4.1 V(I/O) Setting

There is one block of three high-current terminals (designated as V(I/O)) for connecting V(I/O) to either the +5V or +3.3V power supply. V(I/O) must be connected either to the +5V or the +3.3V input power. It is the responsibility of the system integrator to ensure that the required signalling voltage is implemented and that the backplane P1 connector coding corresponds to the implemented signalling voltage.

Warning!

Using both 3.3V and 5V boards within the same backplane segment may result in damage to your equipment. Please note that the presence of only one 5V board determines a 5V signalling environment. The default setting is 5V.

4.2 P1 Connector Coding for V(I/O)

The CompactPCI Specification foresees coding of the P1 connector to correspond to the signalling environment of the PCI bus. For this reason, only boards with universal or the corresponding coding can be physically inserted into the backplane. PEP's factory default setting for V(I/O) is +5V and male, 1567 code, brilliant blue coding keys are used.

Warning!

Using boards with an inadequate signalling voltage may result in damage to your equipment. Therefore, when changing the signalling environment from 5V to 3.3V or vice versa, it is mandatory that proper coding keys are used (refer to chapter 3 of the CPCI Backplane Manual, ID 24229, for details).

5. Interfaces

5.1 Power

Bolt type terminals are provided for inputting DC power to this backplane. These terminals are primarily designed for extending the DC power busses, but they can also be used with non-pluggable power supplies for providing primary DC power input. Refer to Figure 2 for terminal locations.

5.2 Fan Connectors

The backplane can be optionally equipped with two connectors for supplying power for fans and for connecting a fan speed control device. JP21 (FAN1), is a 3-contact male connector which supplys +12V for fan operation as well as the possibility to connect to a speed control device for regulating air flow within the system sub-rack. JP22 (NTC1), is a 2-contact male connector which provides a separate connection for a speed control device and is designed to be used in conjunction with JP21.

For fans that have their own speed control or where no control is required, pins 1 and 2 of JP21 can be used. For external speed control of fans, pins 2 and 3 of JP21 and pins 1 and 2 of JP22 are used. Pin 3 of JP21 and pin 2 of JP22 are connected internally on the board side to each other.

External air flow regulation can be accomplished using a negative thermal coefficient (NTC) device connected to JP22.

Figure 3: Orientation and Pinouts of Connectors JP21 and JP22

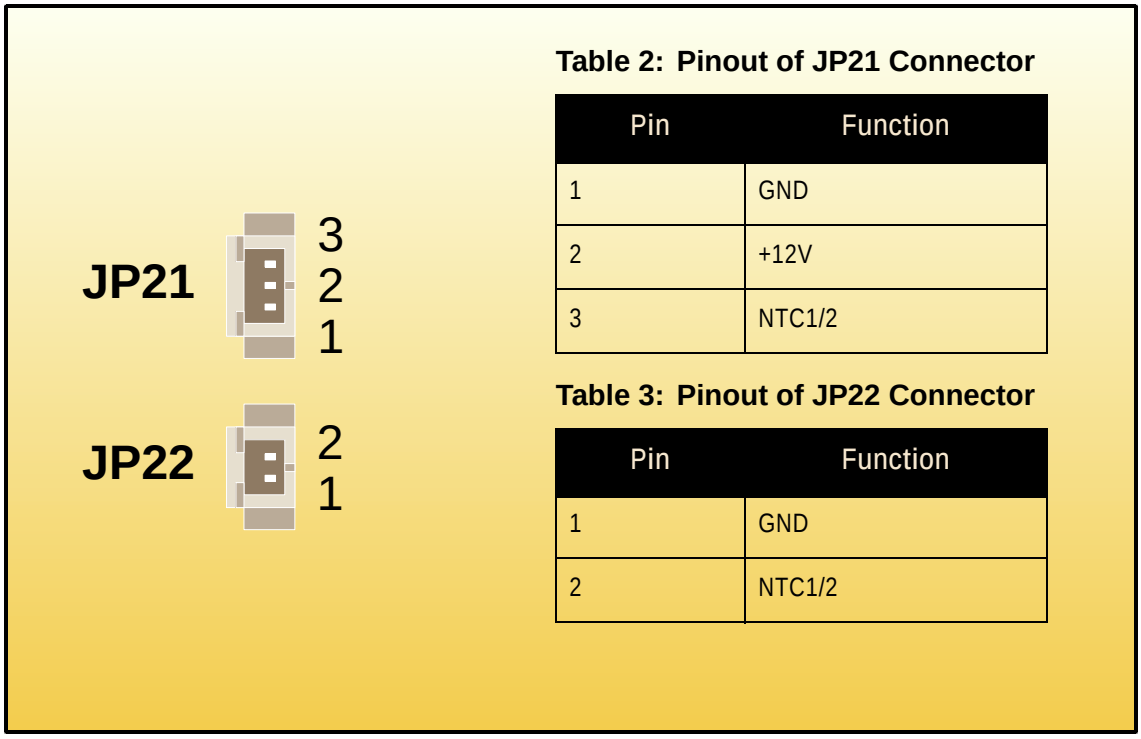


Table 2: Pinout of JP21 Connector

Pin	Function
1	GND
2	+12V
3	NTC1/2

Table 3: Pinout of JP22 Connector

Pin	Function
1	GND
2	NTC1/2

5.3 System Management Connectors JP19 and JP20

Two five-contact male system management bus (IPMB0/1) connectors, JP19/20, can be optionally provided for external interfacing to this bus.

Figure 4: Orientation and Pinout of the IMPB0/1 Connectors JP19/20

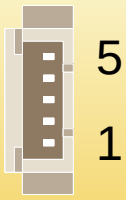


Table 4: Pinout of IMPB0/1 Connectors JP19/20

Pin	Function
1	IMPB0_SCL / IMPB1_SCL
2	GND
3	IMPB0_SDA / IMPB1_SDA
4	IMPB_PWR / V
5	SMB_Alert *

** JP20 only*

5.4 MSD Connector

One 4-pole Molex male connector, JP4, can be optionally equipped on the backplane for the connection of mass storage devices (drives) to the +5V/+12V power supply of the bus.

Figure 5: Orientation and Pinout of Connector JP4

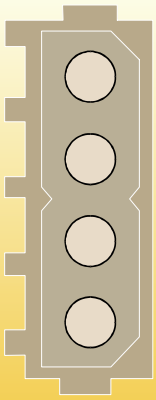


Table 5: Pinout of Connector JP4

Pin	Function
1	+12V
2	GND
3	GND
4	+5V

5.5 System Monitor and Control Connectors JP11 and JP12

This backplane is provided with two connectors for system monitor and control signal interfacing to external devices. Both are 26-contact, male, double pin-row connectors, and have the same signal pinout configuration. The system management bus (IPMB0), the power supply monitor and control signals, and push button reset (PRST#) signal are all implemented on these connectors.

Figure 6: Orientation and Pinout of the SMC Connectors JP11 and JP12

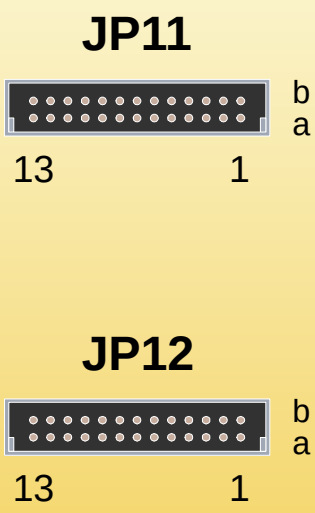


Table 6: Pinout of SMC Connectors JP11 and JP12

Pin	Function	
	Pin Row A	Pin Row B
1	IMPB0_SCL	GND
2	IMPB0_SDA	IMPB0_PWR
3	N/C	GND
4	N/C	GND
5	N/C	GND
6	INH#	GND
7	FAL#	DEG#
8	PRST#	GND
9	GND	V1 SENSE (+5V)
10	V2 SENSE (+3.3V)	SENSE RTN
11	V3 SENSE (+12V)	GND
12	V1 SHARE (+5V)	V2 SHARE (+3.3V)
13	V3 SHARE (+12V)	GND

Note...

The signal pinout assignment is a function of the power supply actually utilized with this backplane. Refer to the corresponding power supply documentation for the applicable signal pinout.

5.6 Auxiliary Signal Connector JP15

One five-contact male auxiliary signal connector, JP15, can be optionally provided for external interfacing.

Figure 7: Orientation and Pinout of Connector JP15

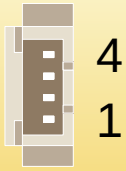


Table 7: Pinout of Connector JP15

Pin	Function
1	GND
2	P5VStby
3	PRST#
4	PSON

6. Optional System Configurations

6.1 Power Supply Options

The design of this backplane allows for several different power supply options:

1. The default configuration of a single compatible pluggable power supply.
2. Addition of compatible pluggable power supplies installed either to the left or right of the backplane.

Option 1 is the standard configuration which requires the integration of a single CP-ADAP-P47-PB (3U or 6U) power bar adapter.

Option 2 can be achieved through the use of power bar adapter boards which can be mounted either to the left or right of the backplane. These boards which accommodate pluggable power supplies are connected to the backplane terminals through the use of power bars. In addition, the system monitor and control signals can be extended via JP11 or JP12 to the power supply adapter boards using appropriate cabling. This configuration allows for additional power supplies to be added which satisfy system requirements such as redundancy, power sharing, or simply increasing available power.

6.2 System Addon Options

The CP6-BP4-PB-RIO backplane is designed to allow the installation of backplane(s) to the left or right of it in a sub-rack and at the same time maintaining the slot raster. This feature makes it possible to add (an) additional backplane(s) using appropriate hardware for accommodating multiple system configurations in one sub-rack.

