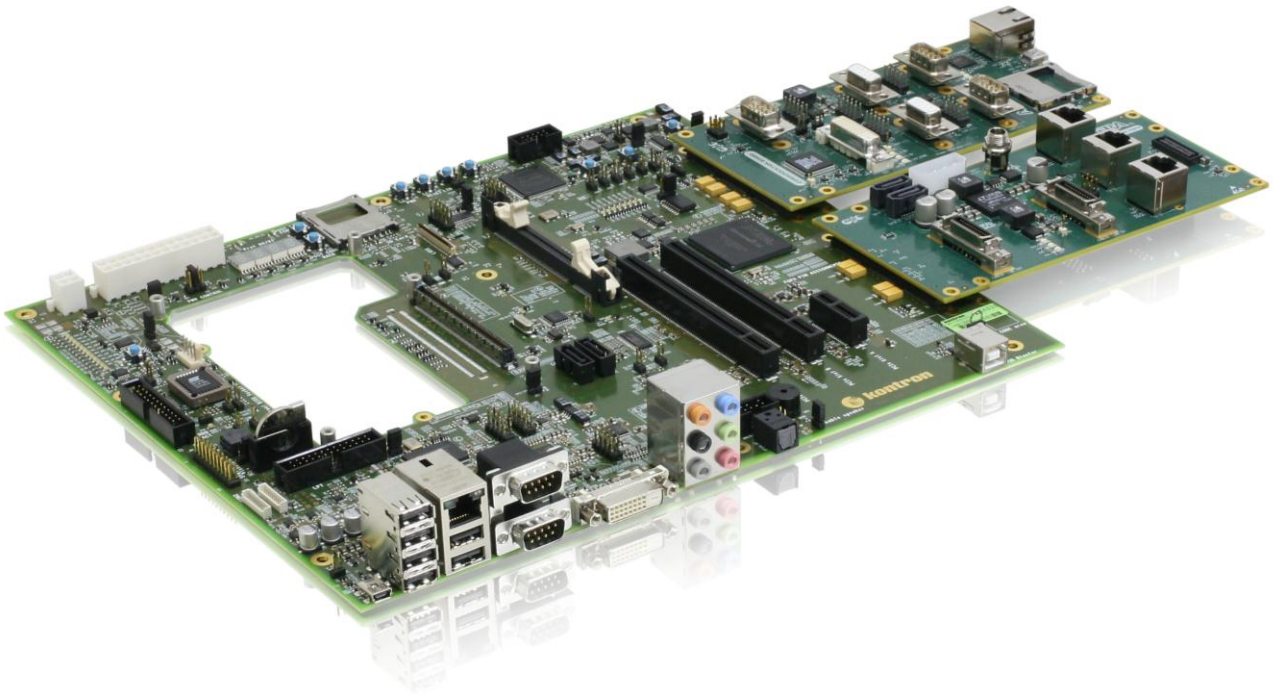
» Kontron User's Guide «



COM Express® FPGA Evaluation Board

Document Revision 1.0

If it's embedded, it's Kontron.

» Table of Contents «

1 User Information 1

1.1 About This Document 1

1.2 Copyright Notice 1

1.3 Trademarks 1

1.4 Standards 1

1.5 Warranty 2

1.6 Technical Support 2

2 Introduction 3

3 Specification 4

3.1 Functional Specification 4

3.2 Block Diagram 6

3.3 Mechanical Specification 7

3.4 Electrical Specification 9

3.5 Environmental Specification 10

3.6 MTBF 10

4 Connector Layout 11

4.1 Rear Panel 11

4.2 Connector Locations 12

4.3 Component overview 13

5 Quick start 16

6 Connectors and Features 17

6.1 Power supply 17

6.1.1 ATX connector 17

6.1.2 PS_ON override & S5 Eco 18

6.1.3 Reset and Power button 19

6.1.4 LID and Sleep 20
6.2 COM Express® connector 21
6.3 FPGA 22
6.3.1 IO Bank 6, 7 and 8 voltage selection 22
6.3.2 Programming 22
6.3.3 Transceivers sharing 23
6.3.4 HSMC interface 24
6.3.5 DDR2 interface 28
6.3.6 FPGA GPIO and LEDs 31
6.3.7 FPGA clock sources 32
6.3.8 FPGA reset 32
6.4 Status LED 33
6.5 Serial ATA 34
6.6 SD-Card / Module GPIO 35
6.7 High Definition Audio 36
6.8 Ethernet 38
6.9 USB 39
6.10 Kontron Feature connector 40
6.11 DVI-D 42
6.12 LVDS 43
6.13 External BIOS 45
6.14 Serial Interface 46
6.15 Status & Debug Connector 47
6.16 CPLD & POST-Code Display 48
6.17 Winbond 83627 Super-I/O 50
6.17.1 RS232 51
6.17.2 LPT 52
6.17.3 FAN 53
6.17.4 SIO Debug connectors 54
6.18 FRU-PROM (I2C EEPROM) 55
7 Battery Information 56
8 Module Single Supply and Wide Range 58

9 Compatibility Matrix.....59

10 Power Distribution.....60

11 Security Advice.....61

12 Document Revision History.....62

1 User Information

1.1 About This Document

This document provides information about products from Kontron Europe GmbH and/or its subsidiaries. No warranty of suitability, purpose, or fitness is implied. While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied “as-is” and is subject to change without notice.

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1.2 Copyright Notice

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- Intel is a registered trademark of Intel Corp.
- Altera is a registered trademark of Altera Corp.
- Cyclone is a registered trademark of Altera Corp.
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1.4 Standards

Kontron Europe GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Europe GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Europe GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Europe GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Europe GmbH that are caused by a faulty Kontron Europe GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Europe GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Please consult our Web site at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section http://emdcustomersection.kontron.com for the latest BIOS downloads, Product Change Notifications and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Introduction

The COM Express® COM.0 Rev. 2.0 COM Express® FPGA Evaluation carrier board is designed to allow embedded application developers to get up and running quickly on the COM Express® modular platform, giving them a head start on the total system design. Simply select a Type 1, Type 10 or Type 2 COM Express® CPU module, then Plug & Go. The Kontron COM Express® FPGA Evaluation Board is an evaluation backplane for COM Express® Computer-on-Modules following the PICMG COM.0 specification Rev 2.0 with pin-out Type 1, Type 10 or Type 2.

Ordering Information

Article	Part-No.	Description
COM Express® FPGA Evaluation Board	38111-0000-00-0	COM Express® FPGA Evaluation Board COM.0 Rev2.0 Type 1, Type 10 or Type 2

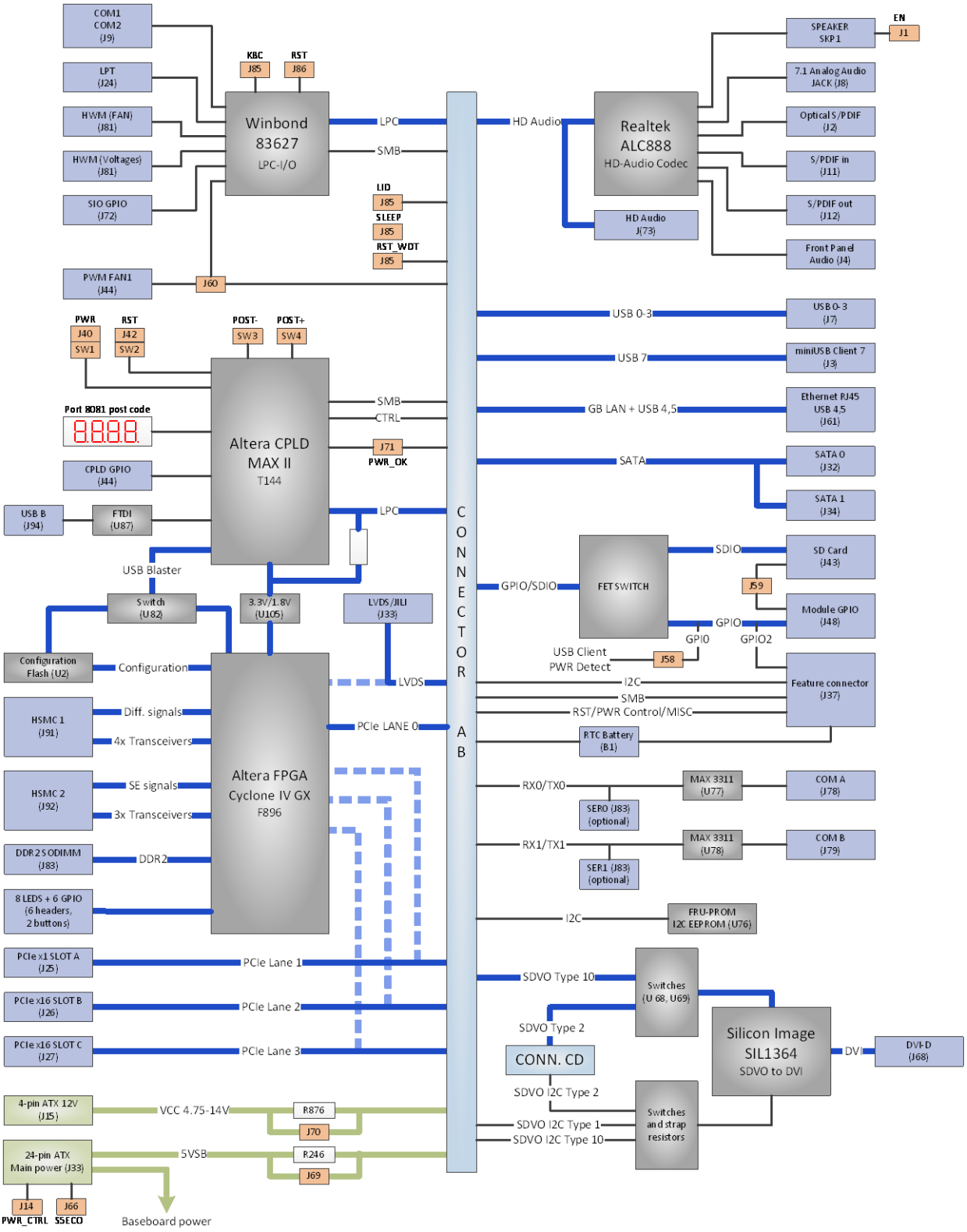
3 Specification

3.1 Functional Specification

- COM Express® COM.0 Rev 2.0 baseboard compatible to Type 10, Type 1 or Type 2 pin-out based modules
- ATX EPS (20pin + 4pin) power connector
- Cyclone IV GX FPGA, F896 package, connected to the module via PCIe lane 0
- 1x HSMC connector – differential pinout + 4 transceivers
- 1x HSMC connector – single-ended pinout + 3 transceivers
- DDR2 (x64) connected to FPGA via SODIMM straight connector
- FPGA GPIOs and LEDs
- 2x PCIexpress x16 (electricaly x1), 1x PCIe x1
- 2 x SATA
- LVDS (40pin JILI FFC40 connector)
- LVDS connected to FPGA (strap option)
- LPC bus connected to FPGA (strap option)
- 1 x DVI-D (SIL1364 SDVOtoDVI)
- 1x Ethernet RJ45
- 6 x USB 2.0/1.1 + 1 x USB Client
- LPC Firmware Hub and SPI Flash support for external BIOS
- Kontron feature connector
- Front panel connectors (HDD Act., Reset and Power Switch)
- Status LED
- SD-Card Socket
- GPIO pin header for module GPIO and Winbond LPC-I/O GPIO
- 4 digit Port 80/81 POST code display with POST code control
- LID and SLEEP support
- Power Control functions (Power Button override, module single supply, power consumption measurements)
- Realtek ALC888 HDAudio Codec
  - 7.1 Analog Audio Jack
  - Optical S/PDIF output
  - Digital S/PDIF input/output
  - Front Panel HD Audio connector
- Winbond 83627HFJ LPC-I/O
  - LPT pin-header
  - COM1/COM2 DSUB9 rear panel connector

- PWM FAN and Hardware Monitor connectors (FAN/Voltage)

3.2 Block Diagram

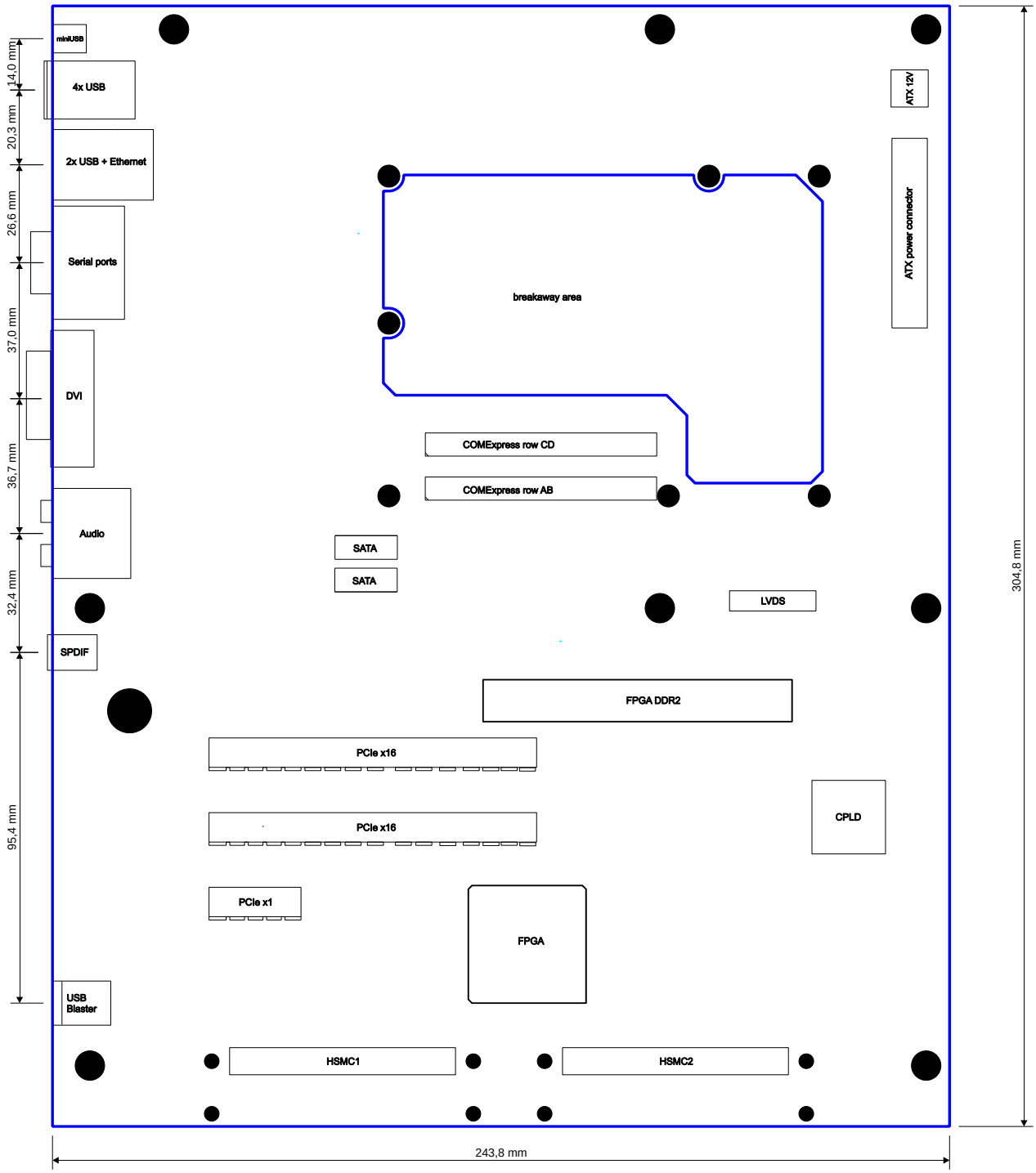


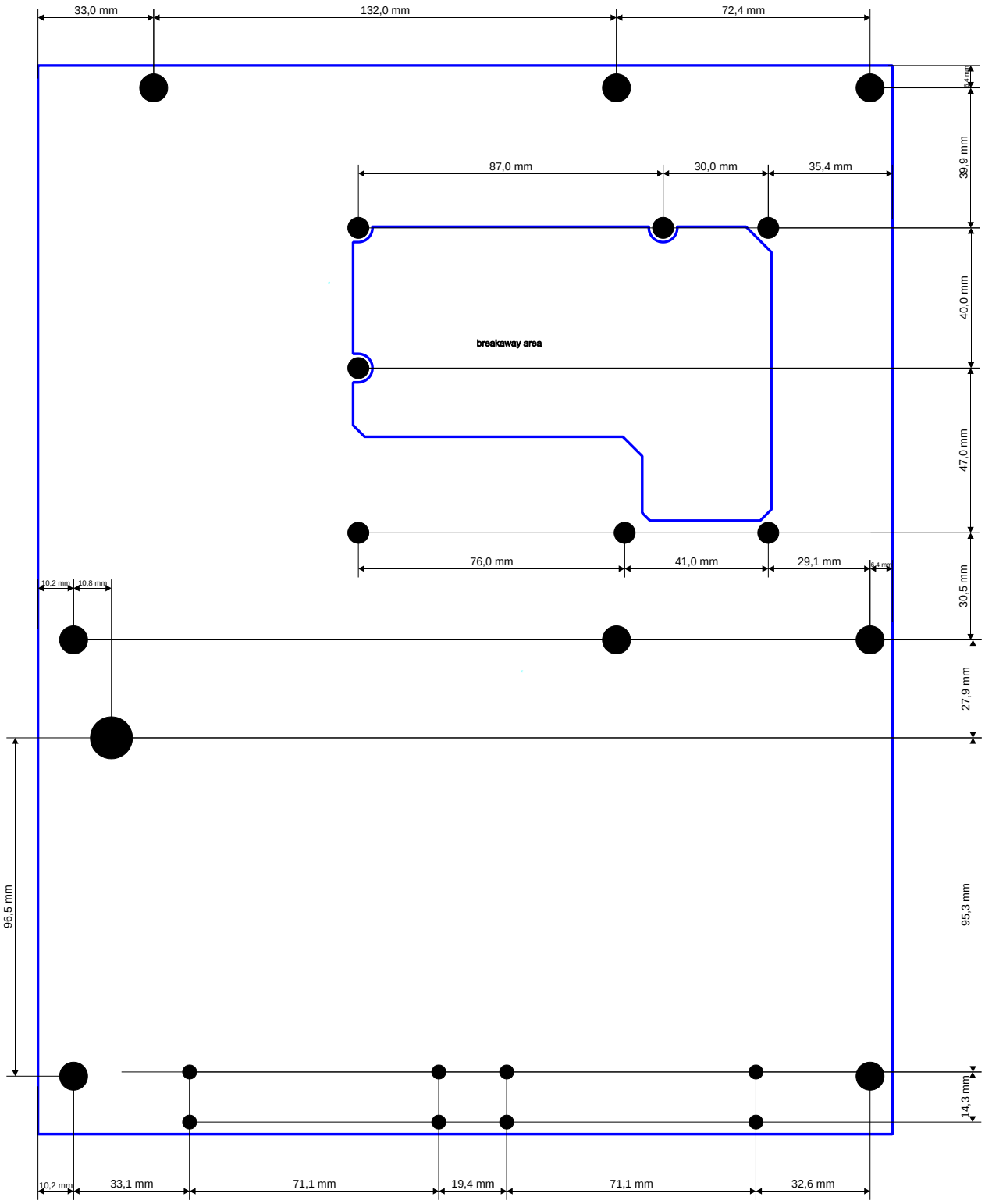
3.3 Mechanical Specification

» Size: 243.8mm x 304.8mm

» max height on top: 34.7mm (Connector J8)

» PCB thickness: 1.4mm ±10%




33,0 mm
132,0 mm
72,4 mm
87,0 mm
30,0 mm
35,4 mm
breakaway area
76,0 mm
41,0 mm
29,1 mm
10,2 mm
10,8 mm
39,9 mm
40,0 mm
47,0 mm
30,5 mm
27,9 mm
96,5 mm
95,3 mm
14,3 mm
10,2 mm
33,1 mm
71,1 mm
19,4 mm
71,1 mm
32,6 mm

3.4 Electrical Specification

Supply Voltage

- » ATX Main Power 24pin
- » ATX_12V P4 connector (wide range input depends on module specification)

Power Supply Rise time

- » The input voltages shall rise from ≤10% of nominal to within the regulation ranges within 0.1ms to 20ms.
- » There must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of its final set-point following the ATX specification

Supply Voltage Ripple

- » Maximum 100 mV peak to peak 0-20MHz

3.5 Environmental Specification

Ambient temperature

» Operating: 0 to +60 °C

» Non-operating: -30 to +85 °C

Humidity

» Operating: 10% to 90% (non condensing)

» Non operating: 5% to 95% (non condensing)

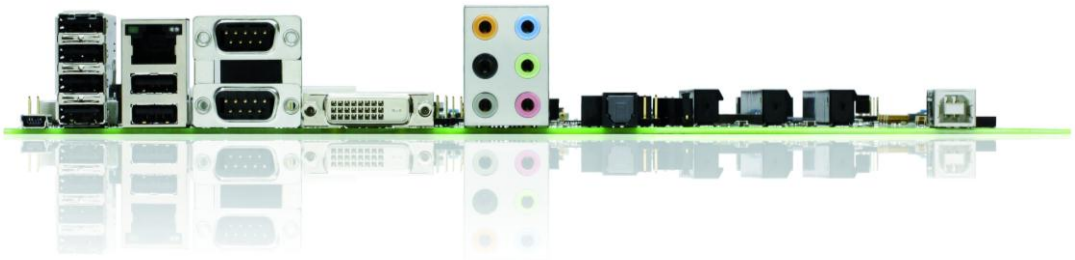
3.6 MTBF

The following MTBF (Mean Time Between Failures) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50% stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

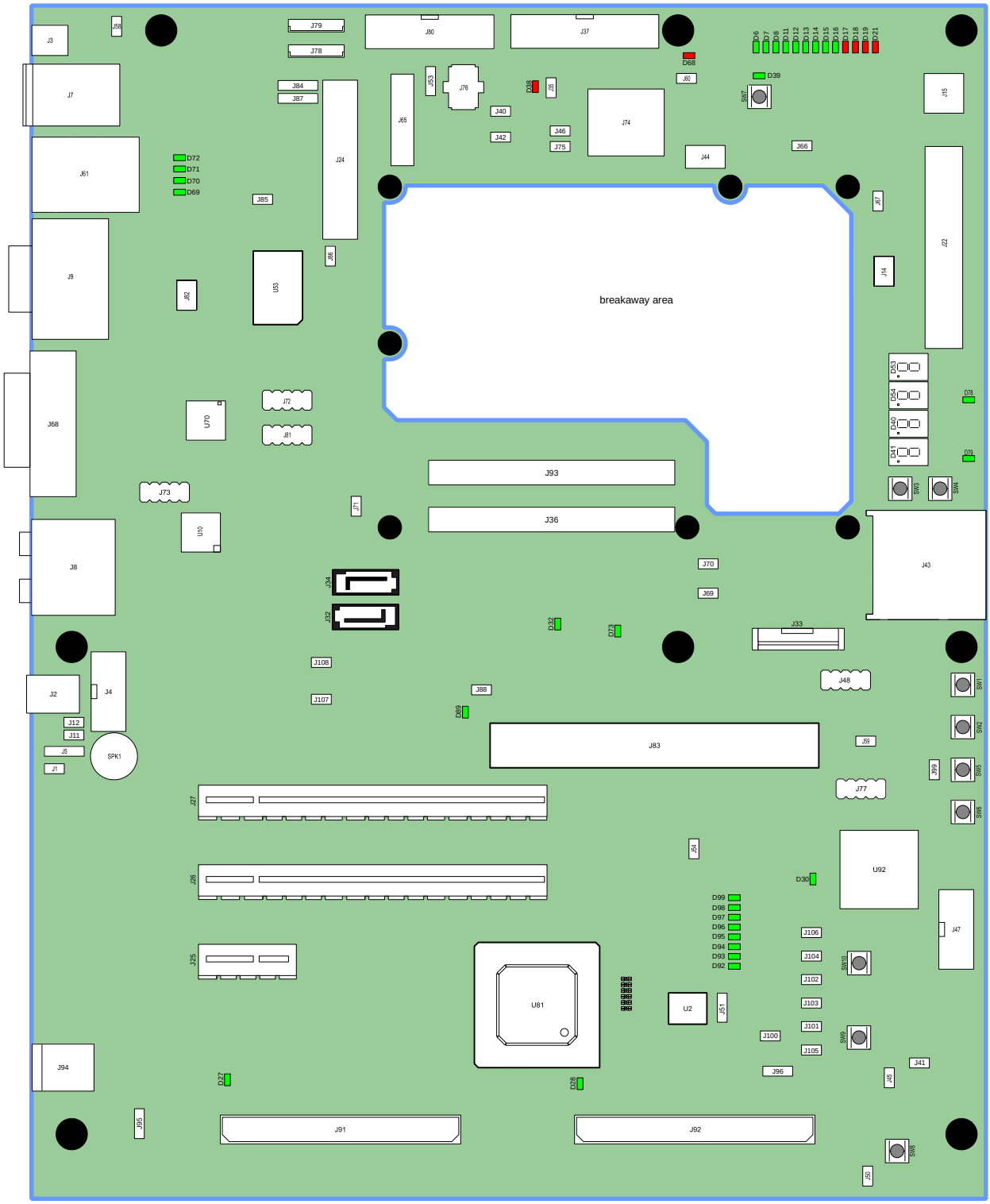
» System MTBF: **tbd** hours

4 Connector Layout

4.1 Rear Panel



4.2 Connector Locations



4.3 Component overview

Connector	Short Description
D6	Status LED: VCC 3.3V
D7	Status LED: VCC 5V
D8	Status LED: VCC 5V SBY
D11	Status LED: VCC 12V Module
D12	Status LED: VCC 12V
D13	Status LED: VCC 3.3V SBY
D14	Status LED: VCC FPGA I/O
D15	Status LED: VCC FPGA INT
D16	Status LED: SUS_STAT#
D17	Status LED: SUS_S3#
D18	Status LED: SUS_S4#
D19	Status LED: SUS_S5#
D21	Status LED: THRMTRIP
D27	HSMC1 present LED
D28	HSMC2 present LED
D32	USB Blaster status LED
D38	Status LED: HDD activity
D39	Status LED: WDT latched
D40/41	PORT80 POST code display
D53/54	PORT81 POST code display
D68	Status LED: WDT active
D69	Status LED: GBLAN Activity
D70	Status LED: GBLAN Link
D71	Status LED: GBLAN Link 100
D72	Status LED: GBLAN Link 1000
D73	Status LED: Type10 detection
D78	Status LED: VCC 1.8V
D79	Status LED: VCC 3.3V for Silicon Image SIL1364
D89	Status LED: VCC 1.8V for DDR2 and FPGA IO
D92	FPGA LED1 – pin AK3
D93	FPGA LED2 – pin AK6
D94	FPGA LED3 – pin AK7
D95	FPGA LED4 – pin AK8
D96	FPGA LED5 – pin AK9
D97	FPGA LED6 – pin AJ9
D98	FPGA LED7 – pin AK10
D99	FPGA LED8 – pin AJ12
J1	Enable/Disable onboard speaker
J2	Optical S/PDIF out
J3	USB Client connector
J4	Front Panel HDAudio connector
J5	HD Audio GPIO / Digital Microphone
J7	USB #0-3
J8	7.1 Analog Audio Jack

J9	SIO COM1/COM2
J11	S/PDIF input
J12	S/PDIF output
J14	ATX_PS_ON Override
J15	ATX_12V 4pin P4 Power Connector
J22	ATX 24pin Main Power Connector
J24	LPT
J25	PCIexpress Slot A (x1, electrically x1)
J26	PCIexpress Slot B (x16, electrically x1)
J27	PCIexpress Slot C (x16, electrically x1)
J32	SATA0
J33	LVDS FFC40
J34	SATA1
J35	HDD Activity
J36	COM Express® AB connector for Type1/Type10 Computer-on-Modules
J37	Kontron Feature Connector
J40	Power Button Front Panel connector
J41	FPGA IO Bank voltage select
J42	ResetButton Front Panel connector
J43	SD-Card socket
J44	PWM FAN1 (SIO or Module)
J45	Automatic OS start
J46	Enable external BIOS0 from LPC FWH
J47	CPLD JTAG
J48	Module GPIO
J50	Onboard USB Blaster target select
J51	Cyclone IV GX slow/fast programming
J53	RTC Supply Voltage source select
J58	Enable/Disable USB Client Power Detect to GPIO
J59	SDCard/GPIO selection
J60	Enable SIO PWM FAN/Module PWM FAN to FAN1 connector
J61	USB #4 / USB #5 and Ethernet RJ45
J65	RTC Battery
J66	Disable/Enable S5ECO
J67	Enable/Disable 5V Standby to module
J68	DVI-D (SDVO2DVI)
J69	Module 5VSB measurement point
J70	Module VCC measurement point
J71	Enable/Disable CPLD PWR_OK
J72	SIO GPIO
J73	HDAudio Connector for external codecs
J74	LPC FirmwareHub for external BIOS
J75	Enable external BIOS1 from SPI Flash
J76	SPI Flash for external BIOS
J77	CPLD GPIO
J78	RS232 COMA from module (RX/TX only)
J79	RS232 COMB from module (RX/TX only)
J80	Status/Debug pin-header
J81	SIO HWM: FAN
J82	SIO HWM: Voltages

J83	DDR2 SODIMM connector
J84	SER1 from module (RX/TX only)
J85	Enable/Disable SIO KBC
J86	Enable/Disable Winbond LPC-I/O
J87	SER0 from module (RX/TX only)
J91	HSMC 1 – differential pinout
J92	HSMC 2 – single-ended pinout
J93	COM Express® CD connector for Type2 Computer-on-Modules
J94	USB Blaster connector
J101	FPGA GPIO9 – pin AJ25
J102	FPGA GPIO10 – pin AG27
J103	FPGA GPIO11 – pin AG26
J104	FPGA GPIO12 – pin AH28
J105	FPGA GPIO13 – pin AK27
J106	FPGA GPIO14 – pin AH29
SPK1	Speaker
SW1	Power button
SW2	Reset button
SW3	POST Code back
SW4	POST Code foward
SW5	LID
SW6	SLEEP
SW7	Reset WDT Latch
SW8	Start OS button
SW9	FPGA GPIO13 button
SW10	FPGA GPIO14 button
U53	Winbond Super IO
U2	FPGA configuration flash
U81	Cyclone IV GX
U87	FTDI
U92	MAX II

5 Quick start

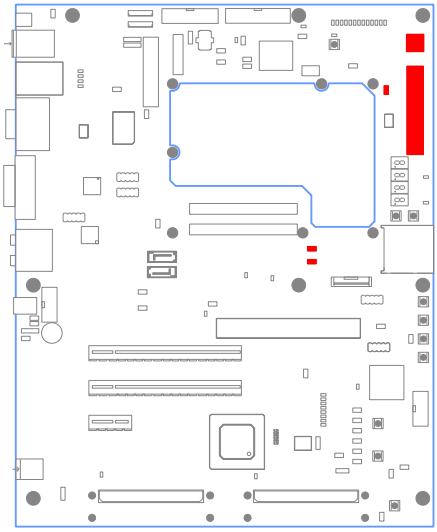
- Connect ETXe module
- Connect SATA hard drive
- Connect ATX power supply
- Connect HSMC card if desired
- Connect DVI-D or LVDS display
- Press PWR (SW1) button for power up the board
- Configure FPGA or configuration flash
- Press START_OS (SW8) to boot to operating system

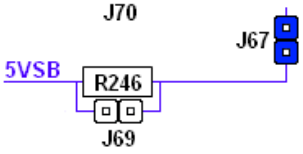
6 Connectors and Features

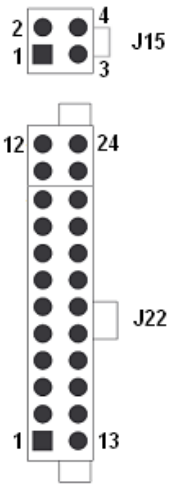
6.1 Power supply

6.1.1 ATX connector

The COM Express® FPGA Evaluation Baseboard power supply follows the ATX 2.x specification and the baseboard should be supplied by connecting an ATX PSU with 24pin ATX and 4pin ATX_12V supply cable in correct orientation. The 4pin ATX_12V connector mainly supplies power to the module over 0R resistor R876 and allows powering the module directly in specified wide range power input. The module additionally is supplied with 5V standby voltage over 0R resistor R246. Standby voltage can easily be disconnected by opening jumper J67 to drive the module in single supply mode. Use connector J70 and J69 for current measurements.







Pin	ATX Main Power	Pin	ATX Main Power
1 (Orange)	+3.3V	13 (Orange/Brown)	+3.3V / +3.3V sense
2 (Orange)	+3.3V	14 (Blue)	-12V
3 (Black)	GND	15 (Black)	GND
4 (Red)	+5V	16 (Green)	Power on
5 (Black)	GND	17 (Black)	GND
6 (Red)	+5V	18 (Black)	GND
7 (Black)	GND	19 (Black)	GND
8 (Grey)	PWR_OK	20	No connection
9 (Purple)	+5VSB	21 (Red)	+5V
10 (Yellow)	+12V	22 (Red)	+5V
11 (Yellow)	+12V	23 (Red)	+5V
12 (Orange)	+3.3V	24 (Black)	GND

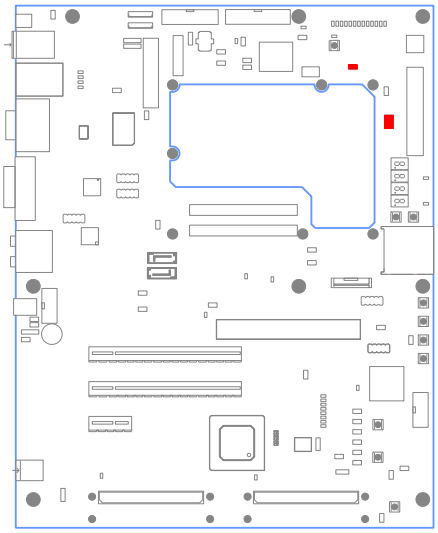
Pin	ATX_12V	Pin	ATX_12V
1 (Black)	GND	3 (Yellow)	Module VCC (12V nominal)
2 (Black)	GND	4 (Yellow)	Module VCC (12V nominal)

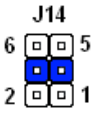
6.1.2 PS_ON override & S5 Eco

With PS_ON override jumper J14 it is possible to switch off the ATX power supply manually. Jumper J66 should be opened to test module S5Eco or single supply mode.

In S5Eco mode all baseboard components (including status LED) are disconnected from standby voltages in S5 state. 5VSB supply to the module can be disconnected separately with jumper J67.

Note:	If S5Eco mode is enabled only power button SW1 is supported to power-on the system.

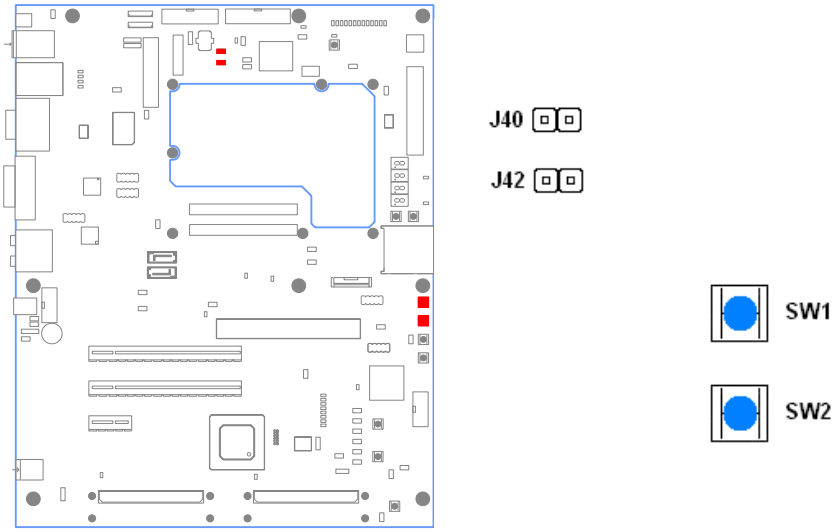




J14 Jumper position	Function
1-2	Power Supply OFF
3-4 (default)	Power Supply controlled by PS_ON signal
5-6	Power Supply always ON

6.1.3 Reset and Power button

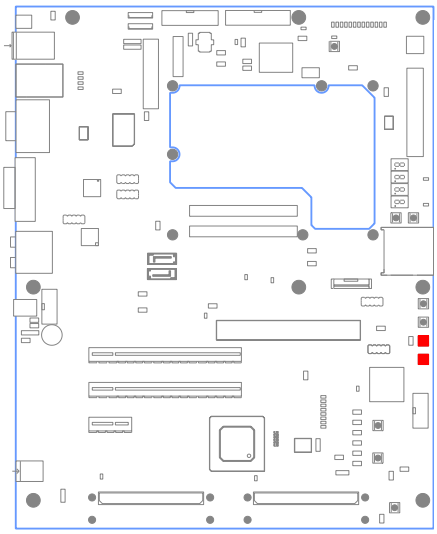
The COM Express® FPGA Evaluation Board provides an onboard Reset Button (SW2) and Power Button (SW1). To connect a front panel button from your chassis use J40 (Power) or J42 (Reset).



Connector	Function
J40	Power Button
SW1	
J42	Reset Button
SW2	

6.1.4 LID and Sleep

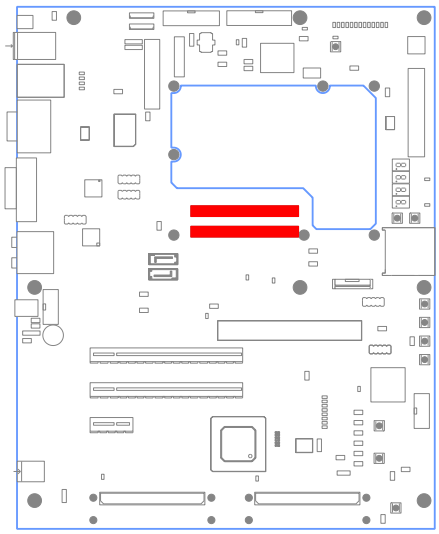
The specification update for PICMG COM.0 modules to revision 2.0 implements new signals for LID and Sleep. The low active signals can be simulated by switch 5 and 6 similar to notebook functionality of closing the lid or pressing the sleep button.



Connector	Function
SW5	LID
SW6	Sleep

6.2 COM Express® connector

The COM Express® FPGA Evaluation Board is an evaluation backplane for Type 1, Type 10 or Type 2 based Computer-on-Modules. Both types 1 and 10 are module pin-outs based on one connectors with 2 rows (Row A and B) with 220 pins overall. Type 2 module has additional connector with two rows (Row C and D). In case Type 1 or Type 10 modules are used with this baseboard, the adapter is necessary to avoid mechanical conflicts of the module and second COM Express® connector (Rows C and D). Please refer to your module documentation for detailed pin-out descriptions.



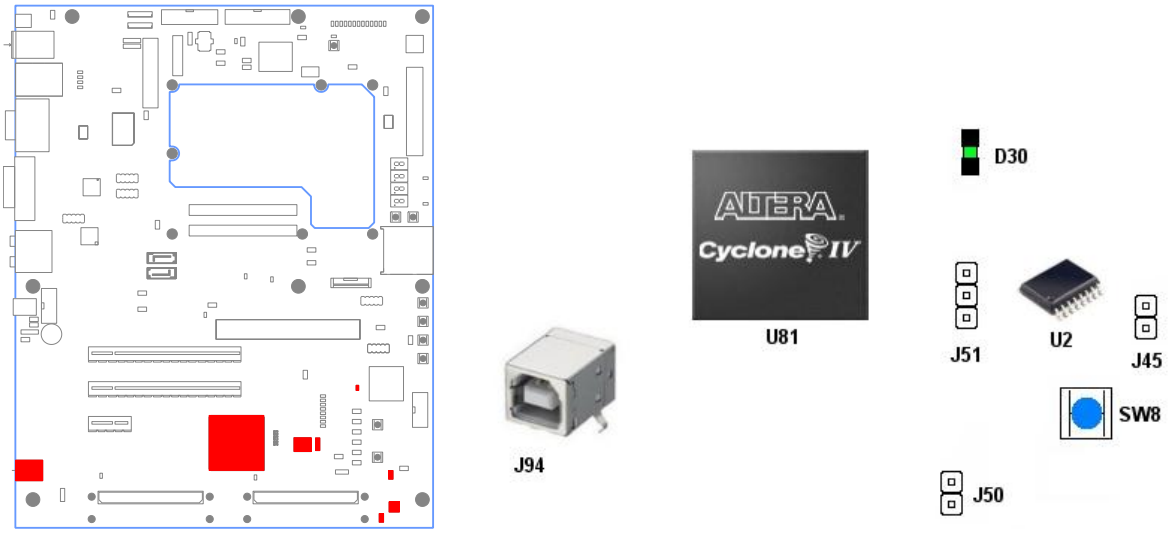
6.3 FPGA

6.3.1 IO Bank 6, 7 and 8 voltage selection

Voltage for IO Banks 6, 7 and 8 can be 2.5V or 3.3V. Voltage is selected with J41. By default J41 is open and 2.5V IO Bank voltage is set. If jumper is placed in J41, then voltage for IO Bank 6, 7 and 8 is set to 3.3V.

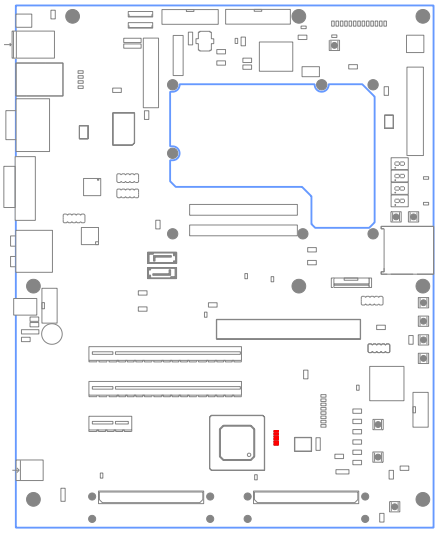
6.3.2 Programming

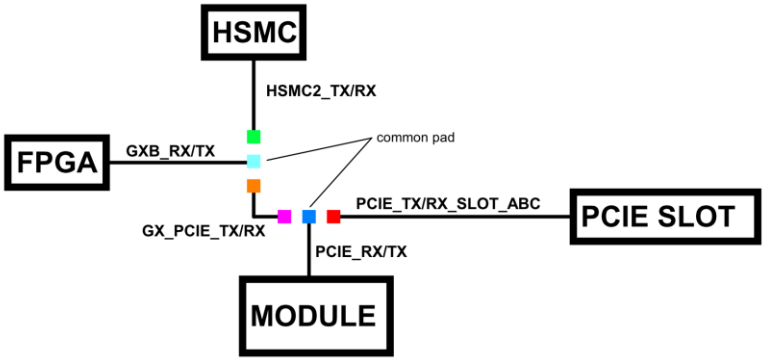
Both FPGA and its configuration flash can be programmed with onboard USB Blaster. The connection with Quartus software is done via J94 (USB B type connector). The programming target is selected with J50. Insert jumper for configuration flash programming, leave J50 open for FPGA programming. D30 indicates that FPGA is configured. FPGA programming speed is selected with J51. After you are done with programming, you can press SW8 to boot to operating system. Install jumper to J45 for automatic boot.



6.3.3 Transceivers sharing

By default, FPGA is connected to the module with PCIe lane 0. With resistors and capacitors you can also lead additional PCIe lanes 1, 2 and 3 into FPGA.

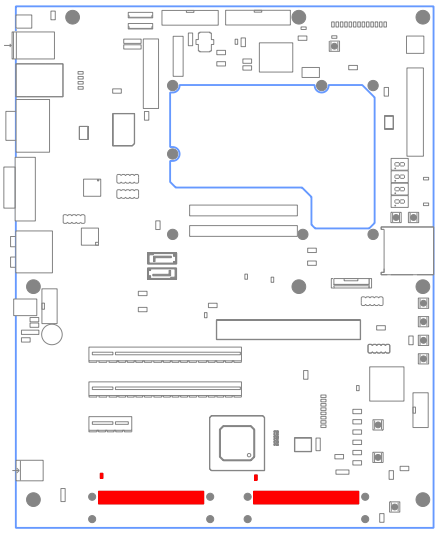


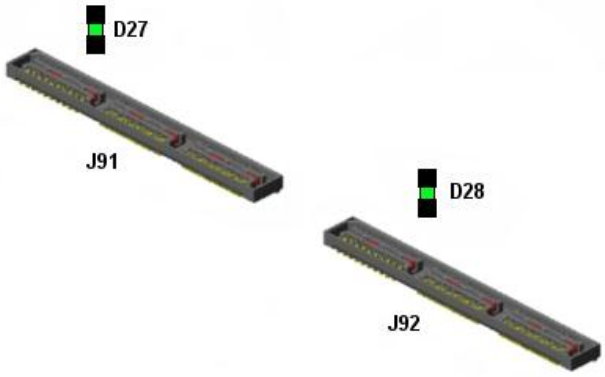


PCIe from module	FPGA pin	FPGA xcvr	I/O standard	Note
PCIE_TX0+	AC2	GXB_RX0+	1.5-V PCML	
PCIE_TX0-	AC1	GXB_RX0-		
PCIE_RX0+	AB4	GXB_TX0+	1.5-V PCML	
PCIE_RX0-	AB3	GXB_TX0-		
PCIE_TX1+	AA2	GXB_RX1+	1.5-V PCML	by default to HSMC2_GRX0
PCIE_TX1-	AA1	GXB_RX1-		
PCIE_RX1+	Y4	GXB_TX1+	1.5-V PCML	by default to HSMC2_GTX0
PCIE_RX1-	Y3	GXB_TX1-		
PCIE_TX2+	W2	GXB_RX2+	1.5-V PCML	by default to HSMC2_GRX1
PCIE_TX2-	W1	GXB_RX2-		
PCIE_RX2+	V4	GXB_TX2+	1.5-V PCML	by default to HSMC2_GTX1
PCIE_RX2-	V3	GXB_TX2-		
PCIE_TX3+	U2	GXB_RX3+	1.5-V PCML	by default to HSMC2_GRX2
PCIE_TX3-	U1	GXB_RX3-		
PCIE_RX3+	T4	GXB_TX3+	1.5-V PCML	by default to HSMC2_GTX2
PCIE_RX3-	T3	GXB_TX3-		

6.3.4 HSMC interface

FPGA banks 6,7 and 8 are connected to two HSMC connectors. HSMC 1 (J91) connector has differential pinout in respect to HSMC specification. D27 indicates presence of HSMC card in connector J91. Following table shows possible combinations of J91 bank usage. HSMC 2 connector has single-ended pinout. D28 indicates presence of HSMC card in connecter J92.





J91 Bank 2	J91 Bank 3
Differential	Single-ended
Differential	Differential
Single-ended	Single-ended
Single-ended	Differential

J91 HSMC connector pinout

FPGA PIN	SIGNAL NAME	HSMC PIN	HSMC SIGNAL NAME	HSMC SIGNAL NAME	HSMC PIN	SIGNAL NAME	FPGA PIN
-	NC	1	XCVR_TXp7	XCVR_TXp7	2	NC	-
-	NC	3	XCVR_TXn7	XCVR_TXn7	4	NC	-
-	NC	5	XCVR_TXp6	XCVR_TXp6	6	NC	-
-	NC	7	XCVR_TXn6	XCVR_TXn6	8	NC	-
-	NC	9	XCVR_TXp5	XCVR_TXp5	10	NC	-
-	NC	11	XCVR_TXn5	XCVR_TXn5	12	NC	-
-	NC	13	XCVR_TXp4	XCVR_TXp4	14	NC	-
-	NC	15	XCVR_TXn4	XCVR_TXn4	16	NC	-
PIN_H4	HSMC1_GTX3+	17	XCVR_TXp3	XCVR_TXp3	18	HSMC1_GRX3+	PIN_J2
PIN_H3	HSMC1_GTX3-	19	XCVR_TXn3	XCVR_TXn3	20	HSMC1_GRX3-	PIN_J1
PIN_K4	HSMC1_GTX2+	21	XCVR_TXp2	XCVR_TXp2	22	HSMC1_GRX2+	PIN_L2
PIN_K3	HSMC1_GTX2-	23	XCVR_TXn2	XCVR_TXn2	24	HSMC1_GRX2-	PIN_L1

J91 HSMC connector pinout

FPGA PIN	SIGNAL NAME	HSMC PIN	HSMC SIGNAL NAME	HSMC SIGNAL NAME	HSMC PIN	SIGNAL NAME	FPGA PIN
PIN_M4	HSMC1_GTX1+	25	XCVR_TXp1	XCVR_TXp1	26	HSMC1_GRX1+	PIN_N2
PIN_M3	HSMC1_GTX1-	27	XCVR_TXn1	XCVR_TXn1	28	HSMC1_GRX1-	PIN_N1
PIN_P4	HSMC1_GTX0+	29	XCVR_TXp0	XCVR_TXp0	30	HSMC1_GRX0+	PIN_R2
PIN_P3	HSMC1_GTX0-	31	XCVR_TXn0	XCVR_TXn0	32	HSMC1_GRX0-	PIN_R1
PIN_F20	HSMC1_SDA	33	SDA	SCL	34	HSMC1_SCL	PIN_F21
-	JTAG_TCK	35	JTAG_TCK	JTAG_TMS	36	JTAG_TMS	-
-	JTAG_HSMC2_TDI_R	37	JTAG_TDO	JTAG_TDI	38	JTAG_HSMC1_TDI_R	-
PIN_A19	HSMC1_CLKOUT0	39	CLKOUT0	CLKIN0	40	HSMC1_CLKIN0	PIN_A20
PIN_B22	HSMC1_D0	41	D0	D1	42	HSMC1_D1	PIN_C22
PIN_A21	HSMC1_D2	43	D2	D3	44	HSMC1_D3	PIN_B21
		45	3.3 V	12 V	46		
PIN_F26	HSMC1_TX0+	47	LVDS_TXp0	LVDS_RXp0	48	HSMC1_RX0+	PIN_K25
PIN_F27	HSMC1_TX0-	49	LVDS_TXn0	LVDS_RXn0	50	HSMC1_RX0-	PIN_J26
		51	3.3 V	12 V	52		
PIN_G26	HSMC1_TX1+	53	LVDS_TXp1	LVDS_RXp1	54	HSMC1_RX1+	PIN_K21
PIN_G27	HSMC1_TX1-	55	LVDS_TXn1	LVDS_RXn1	56	HSMC1_RX1-	PIN_K22
		57	3.3 V	12 V	58		
PIN_E27	HSMC1_TX2+	59	LVDS_TXp2	LVDS_RXp2	60	HSMC1_RX2+	PIN_J25
PIN_E28	HSMC1_TX2-	61	LVDS_TXn2	LVDS_RXn2	62	HSMC1_RX2-	PIN_H25
		63	3.3 V	12 V	64		
PIN_F28	HSMC1_TX3+	65	LVDS_TXp3	LVDS_RXp3	66	HSMC1_RX3+	PIN_G23
PIN_F29	HSMC1_TX3-	67	LVDS_TXn3	LVDS_RXn3	68	HSMC1_RX3-	PIN_F23
		69	3.3 V	12 V	70		
PIN_J27	HSMC1_TX4+	71	LVDS_TXp4	LVDS_RXp4	72	HSMC1_RX4+	PIN_B30
PIN_H27	HSMC1_TX4-	73	LVDS_TXn4	LVDS_RXn4	74	HSMC1_RX4-	PIN_A29
		75	3.3 V	12 V	76		
PIN_C29	HSMC1_TX5+	77	LVDS_TXp5	LVDS_RXp5	78	HSMC1_RX5+	PIN_H24
PIN_C30	HSMC1_TX5-	79	LVDS_TXn5	LVDS_RXn5	80	HSMC1_RX5-	PIN_G24
		81	3.3 V	12 V	82		
PIN_D29	HSMC1_TX6+	83	LVDS_TXp6	LVDS_RXp6	84	HSMC1_RX6+	PIN_D28
PIN_D30	HSMC1_TX6-	85	LVDS_TXn6	LVDS_RXn6	86	HSMC1_RX6-	PIN_C28
		87	3.3 V	12 V	88		
PIN_K26	HSMC1_TX7+	89	LVDS_TXp7	LVDS_RXp7	90	HSMC1_RX7+	PIN_J28
PIN_K27	HSMC1_TX7-	91	LVDS_TXn7	LVDS_RXn7	92	HSMC1_RX7-	PIN_H28
		93	3.3 V	12 V	94		
PIN_B25	HSMC1_CLKOUT1+	95	CLKOUT1p	CLKIN1p	96	HSMC1_CLKIN1+	PIN_B15
PIN_A24	HSMC1_CLKOUT1-	97	CLKOUT1n	CLKIN1n	98	HSMC1_CLKIN1-	PIN_A15
		99	3.3 V	12 V	100		
PIN_L27	HSMC1_TX8+	101	LVDS_TXp8	LVDS_RXp8	102	HSMC1_RX8+	PIN_J29
PIN_L28	HSMC1_TX8-	103	LVDS_TXn8	LVDS_RXn8	104	HSMC1_RX8-	PIN_J30
		105	3.3 V	12 V	106		
PIN_H30	HSMC1_TX9+	107	LVDS_TXp9	LVDS_RXp9	108	HSMC1_RX9+	PIN_N24
PIN_G30	HSMC1_TX9-	109	LVDS_TXn9	LVDS_RXn9	110	HSMC1_RX9-	PIN_M25
		111	3.3 V	12 V	112		
PIN_K28	HSMC1_TX10+	113	LVDS_TXp10	LVDS_RXp10	114	HSMC1_RX10+	PIN_M27
PIN_K29	HSMC1_TX10-	115	LVDS_TXn10	LVDS_RXn10	116	HSMC1_RX10-	PIN_M28
		117	3.3 V	12 V	118		

J91 HSMC connector pinout							
FPGA PIN	SIGNAL NAME	HSMC PIN	HSMC SIGNAL NAME	HSMC SIGNAL NAME	HSMC PIN	SIGNAL NAME	FPGA PIN
PIN_N29	HSMC1_TX11+	119	LVDS_TXp11	LVDS_RXp11	120	HSMC1_RX11+	PIN_N25
PIN_N30	HSMC1_TX11-	121	LVDS_TXn11	LVDS_RXn11	122	HSMC1_RX11-	PIN_M26
		123	3.3 V	12 V	124		
PIN_L30	HSMC1_TX12+	125	LVDS_TXp12	LVDS_RXp12	126	HSMC1_RX12+	PIN_R27
PIN_K30	HSMC1_TX12-	127	LVDS_TXn12	LVDS_RXn12	128	HSMC1_RX12-	PIN_R28
		129	3.3 V	12 V	130		
PIN_M29	HSMC1_TX13+	131	LVDS_TXp13	LVDS_RXp13	132	HSMC1_RX13+	PIN_P27
PIN_M30	HSMC1_TX13-	133	LVDS_TXn13	LVDS_RXn13	134	HSMC1_RX13-	PIN_P28
		135	3.3 V	12 V	136		
PIN_N27	HSMC1_TX14+	137	LVDS_TXp14	LVDS_RXp14	138	HSMC1_RX14+	PIN_M21
PIN_N28	HSMC1_TX14-	139	LVDS_TXn14	LVDS_RXn14	140	HSMC1_RX14-	PIN_M22
		141	3.3 V	12 V	142		
PIN_R30	HSMC1_TX15+	143	LVDS_TXp15	LVDS_RXp15	144	HSMC1_RX15+	PIN_R24
PIN_P30	HSMC1_TX15-	145	LVDS_TXn15	LVDS_RXn15	146	HSMC1_RX15-	PIN_P25
		147	3.3 V	12 V	148		
PIN_R25	HSMC1_TX16+	149	LVDS_TXp16	LVDS_RXp16	150	HSMC1_RX16+	PIN_P21
PIN_R26	HSMC1_TX16-	151	LVDS_TXn16	LVDS_RXn16	152	HSMC1_RX16-	PIN_N21
		153	3.3 V	12 V	154		
PIN_D3	HSMC1_CLKOUT2+	155	CLKOUT2p	CLKIN2p	156	HSMC1_CLKIN2+	PIN_V15
PIN_C3	HSMC1_CLKOUT2-	157	CLKOUT2n	CLKIN2n	158	HSMC1_CLKIN2-	PIN_W15
		159	3.3 V	PSNTn	160	HSMC1_PSNT#	PIN_A23

J92 Bank 2	J92 Bank 3
Single-ended	Single-ended

J92 HSMC connector pinout							
FPGA PIN	SIGNAL NAME	HSMC PIN	HSMC SIGNAL NAME	HSMC SIGNAL NAME	HSMC PIN	SIGNAL NAME	FPGA PIN
-	NC	1	XCVR_TXp7	XCVR_RXp7	2	NC	-
-	NC	3	XCVR_TXn7	XCVR_RXn7	4	NC	-
-	NC	5	XCVR_TXp6	XCVR_RXp6	6	NC	-
-	NC	7	XCVR_TXn6	XCVR_RXn6	8	NC	-
-	NC	9	XCVR_TXp5	XCVR_RXp5	10	NC	-
-	NC	11	XCVR_TXn5	XCVR_RXn5	12	NC	-
-	NC	13	XCVR_TXp4	XCVR_RXp4	14	NC	-
-	NC	15	XCVR_TXn4	XCVR_RXn4	16	NC	-
-	NC	17	XCVR_TXp3	XCVR_RXp3	18	NC	-
-	NC	19	XCVR_TXn3	XCVR_RXn3	20	NC	-
PIN_T4	HSMC2_GTX2+	21	XCVR_TXp2	XCVR_RXp2	22	HSMC2_GRX2+	PIN_U2
PIN_T3	HSMC2_GTX2-	23	XCVR_TXn2	XCVR_RXn2	24	HSMC2_GRX2-	PIN_U1
PIN_V4	HSMC2_GTX1+	25	XCVR_TXp1	XCVR_RXp1	26	HSMC2_GRX1+	PIN_W2
PIN_V3	HSMC2_GTX1-	27	XCVR_TXn1	XCVR_RXn1	28	HSMC2_GRX1-	PIN_W1
PIN_Y4	HSMC2_GTX0+	29	XCVR_TXp0	XCVR_RXp0	30	HSMC2_GRX0+	PIN_AA2
PIN_Y3	HSMC2_GTX0-	31	XCVR_TXn0	XCVR_RXn0	32	HSMC2_GRX0-	PIN_AA1
PIN_G18	HSMC2_SDA	33	SDA	SCL	34	HSMC2_SCL	PIN_D20

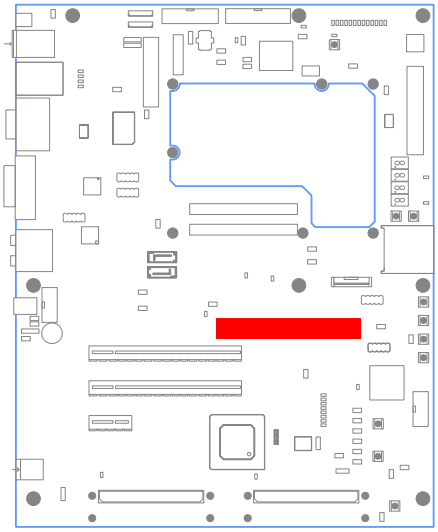
J92 HSMC connector pinout

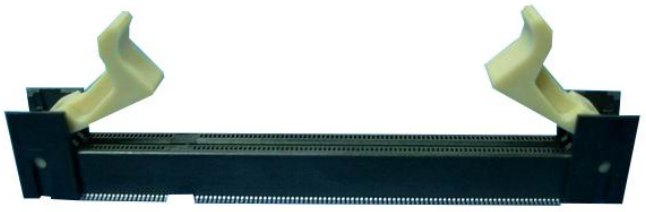
FPGA PIN	SIGNAL NAME	HSMC PIN	HSMC SIGNAL NAME	HSMC SIGNAL NAME	HSMC PIN	SIGNAL NAME	FPGA PIN
-	JTAG_TCK	35	JTAG_TCK	JTAG_TMS	36	JTAG_TMS	-
-	JTAG_HSMC2_TDO_R	37	JTAG_TDO	JTAG_TDI	38	JTAG_HSMC2_TDI_R	-
PIN_F7	HSMC2_CLKOUT0	39	CLKOUT0	CLKIN0	40	HSMC_CLKIN0	PIN_F11
PIN_B6	HSMC2_D0	41	D0	D1	42	HSMC2_D1	PIN_G12
PIN_A5	HSMC2_D2	43	D2	D3	44	HSMC2_D3	PIN_G13
		45	3.3 V	12 V	46		
PIN_A6	HSMC2_D4	47	D4	D5	48	HSMC2_D5	PIN_J9
PIN_A7	HSMC2_D6	49	D6	D7	50	HSMC2_D7	PIN_G14
		51	3.3 V	12 V	52		
PIN_C6	HSMC2_D8	53	D8	D9	54	HSMC2_D9	PIN_G6
PIN_B7	HSMC2_D10	55	D10	D11	56	HSMC2_D11	PIN_G15
		57	3.3 V	12 V	58		
PIN_D12	HSMC2_D12	59	D12	D13	60	HSMC2_D13	PIN_G20
PIN_A11	HSMC2_D14	61	D14	D15	62	HSMC2_D15	PIN_E7
		63	3.3 V	12 V	64		
PIN_C7	HSMC2_D16	65	D16	D17	66	HSMC2_D17	PIN_D8
PIN_A8	HSMC2_D18	67	D18	D19	68	HSMC2_D19	PIN_G7
		69	3.3 V	12 V	70		
PIN_D11	HSMC2_D20	71	D20	D21	72	HSMC2_D21	PIN_F6
PIN_F13	HSMC2_D22	73	D22	D23	74	HSMC2_D23	PIN_D7
		75	3.3 V	12 V	76		
PIN_B9	HSMC2_D24	77	D24	D25	78	HSMC2_D25	PIN_D4
PIN_E13	HSMC2_D26	79	D26	D27	80	HSMC2_D27	PIN_C5
		81	3.3 V	12 V	82		
PIN_C10	HSMC2_D28	83	D28	D29	84	HSMC2_D29	PIN_C4
PIN_F12	HSMC2_D30	85	D30	D31	86	HSMC2_D31	PIN_D6
		87	3.3 V	12 V	88		
PIN_C11	HSMC2_D32	89	D32	D33	90	HSMC2_D33	PIN_F14
PIN_E12	HSMC2_D34	91	D34	D35	92	HSMC2_D35	PIN_A17
		93	3.3 V	12 V	94		
PIN_E10	HSMC2_CLKOUT1+	95	D36	D37	96	HSMC2_CLKIN1+	PIN_D1
PIN_D10	HSMC2_CLKOUT1-	97	D38	D39	98	HSMC2_CLKIN1-	PIN_C2
		99	3.3 V	12 V	100		
PIN_C12	HSMC2_D40	101	D40	D41	102	HSMC2_D41	PIN_E6
PIN_A13	HSMC2_D42	103	D42	D43	104	HSMC2_D43	PIN_D5
		105	3.3 V	12 V	106		
PIN_D13	HSMC2_D44	107	D44	D45	108	HSMC2_D45	PIN_F15
PIN_C13	HSMC2_D46	109	D46	D47	110	HSMC2_D47	PIN_A9
		111	3.3 V	12 V	112		
PIN_D19	HSMC2_D48	113	D48	D49	114	HSMC2_D49	PIN_A10
PIN_B18	HSMC2_D50	115	D50	D51	116	HSMC2_D51	PIN_B10
		117	3.3 V	12 V	118		
PIN_C18	HSMC2_D52	119	D52	D53	120	HSMC2_D53	PIN_A12
PIN_D18	HSMC2_D54	121	D54	D55	122	HSMC2_D55	PIN_B12
		123	3.3 V	12 V	124		
PIN_A18	HSMC2_D56	125	D56	D57	126	HSMC2_D57	PIN_F16
PIN_C17	HSMC2_D58	127	D58	D59	128	HSMC2_D59	PIN_F17

J92 HSMC connector pinout							
FPGA PIN	SIGNAL NAME	HSMC PIN	HSMC SIGNAL NAME	HSMC SIGNAL NAME	HSMC PIN	SIGNAL NAME	FPGA PIN
		129	3.3 V	12 V	130		
PIN_D17	HSMC2_D60	131	D60	D61	132	HSMC2_D61	PIN_G17
PIN_C16	HSMC2_D62	133	D62	D63	134	HSMC2_D63	PIN_F18
		135	3.3 V	12 V	136		
PIN_D16	HSMC2_D64	137	D64	D65	138	HSMC2_D65	PIN_E18
PIN_C15	HSMC2_D66	139	D66	D67	140	HSMC2_D67	PIN_B19
		141	3.3 V	12 V	142		
PIN_D15	HSMC2_D68	143	D68	D69	144	HSMC2_D69	PIN_C19
PIN_C14	HSMC2_D70	145	D70	D71	146	HSMC2_D71	PIN_C20
		147	3.3 V	12 V	148		
PIN_A14	HSMC2_D72	149	D72	D73	150	HSMC2_D73	PIN_E15
PIN_D14	HSMC2_D74	151	D74	D75	152	HSMC2_D75	PIN_E16
		153	3.3 V	12 V	154		
PIN_G10	HSMC2_CLKOUT2+	155	D76	D77	156	HSMC2_CLKIN2+	PIN_D23
PIN_F10	HSMC2_CLKOUT2-	157	D78	D79	158	HSMC2_CLKIN2-	PIN_C23
		159	3.3 V	PSNTn	160	HSMC2_PSNT#	PIN_E19

6.3.5 DDR2 interface

FPGA banks 3, 4 and 5 are connected to DDR2 SODIMM connector.





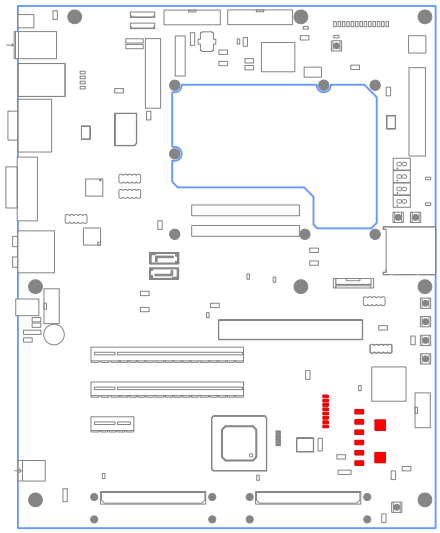
DDR2 signals	FPGA pin	I/O standard
DDR_A[0]	PIN_AF18	SSTL-18 CLASS I
DDR_A[1]	PIN_AF19	SSTL-18 CLASS I
DDR_A[10]	PIN_AK22	SSTL-18 CLASS I
DDR_A[11]	PIN_AH23	SSTL-18 CLASS I
DDR_A[12]	PIN_AK25	SSTL-18 CLASS I
DDR_A[13]	PIN_AG17	SSTL-18 CLASS I

DDR2 signals	FPGA pin	I/O standard
DDR_A[14]	PIN_AF22	SSTL-18 CLASS I
DDR_A[15]	PIN_AD23	SSTL-18 CLASS I
DDR_A[2]	PIN_AE20	SSTL-18 CLASS I
DDR_A[3]	PIN_AG19	SSTL-18 CLASS I
DDR_A[4]	PIN_AH20	SSTL-18 CLASS I
DDR_A[5]	PIN_AG20	SSTL-18 CLASS I
DDR_A[6]	PIN_AH21	SSTL-18 CLASS I
DDR_A[7]	PIN_AG22	SSTL-18 CLASS I
DDR_A[8]	PIN_AH22	SSTL-18 CLASS I
DDR_A[9]	PIN_AF21	SSTL-18 CLASS I
DDR_BA[0]	PIN_AE15	SSTL-18 CLASS I
DDR_BA[1]	PIN_Y20	SSTL-18 CLASS I
DDR_BA[2]	PIN_AA21	SSTL-18 CLASS I
DDR_CAS_n	PIN_AK12	SSTL-18 CLASS I
DDR_CKE[0]	PIN_AF16	SSTL-18 CLASS I
DDR_CKE[1]	PIN_AG16	SSTL-18 CLASS I
DDR_CLK[0]	PIN_AG24	SSTL-18 CLASS I
DDR_CLK[1]	PIN_AF4	SSTL-18 CLASS I
DDR_CLK_n[0]	PIN_AH24	SSTL-18 CLASS I
DDR_CLK_n[1]	PIN_AG4	SSTL-18 CLASS I
DDR_CS_n[0]	PIN_AJ22	SSTL-18 CLASS I
DDR_CS_n[1]	PIN_AJ19	SSTL-18 CLASS I
DDR_DM[0]	PIN_Y30	SSTL-18 CLASS I
DDR_DM[1]	PIN_AG29	SSTL-18 CLASS I
DDR_DM[2]	PIN_AE27	SSTL-18 CLASS I
DDR_DM[3]	PIN_AK23	SSTL-18 CLASS I
DDR_DM[4]	PIN_Y17	SSTL-18 CLASS I
DDR_DM[5]	PIN_AJ7	SSTL-18 CLASS I
DDR_DM[6]	PIN_AJ6	SSTL-18 CLASS I
DDR_DM[7]	PIN_AH6	SSTL-18 CLASS I
DDR_DQ[0]	PIN_V28	SSTL-18 CLASS I
DDR_DQ[1]	PIN_T23	SSTL-18 CLASS I
DDR_DQ[10]	PIN_AB26	SSTL-18 CLASS I
DDR_DQ[11]	PIN_AB25	SSTL-18 CLASS I
DDR_DQ[12]	PIN_Y27	SSTL-18 CLASS I
DDR_DQ[13]	PIN_Y25	SSTL-18 CLASS I
DDR_DQ[14]	PIN_AF30	SSTL-18 CLASS I
DDR_DQ[15]	PIN_AE26	SSTL-18 CLASS I
DDR_DQ[16]	PIN_AB30	SSTL-18 CLASS I
DDR_DQ[17]	PIN_AB28	SSTL-18 CLASS I
DDR_DQ[18]	PIN_AE29	SSTL-18 CLASS I
DDR_DQ[19]	PIN_AD27	SSTL-18 CLASS I
DDR_DQ[2]	PIN_AA29	SSTL-18 CLASS I
DDR_DQ[20]	PIN_AC28	SSTL-18 CLASS I
DDR_DQ[21]	PIN_AD30	SSTL-18 CLASS I
DDR_DQ[22]	PIN_AE28	SSTL-18 CLASS I
DDR_DQ[23]	PIN_AG30	SSTL-18 CLASS I
DDR_DQ[24]	PIN_AH25	SSTL-18 CLASS I
DDR_DQ[25]	PIN_AK26	SSTL-18 CLASS I

DDR2 signals	FPGA pin	I/O standard
DDR_DQ[26]	PIN_AE21	SSTL-18 CLASS I
DDR_DQ[27]	PIN_AE19	SSTL-18 CLASS I
DDR_DQ[28]	PIN_AJ24	SSTL-18 CLASS I
DDR_DQ[29]	PIN_AG23	SSTL-18 CLASS I
DDR_DQ[3]	PIN_W25	SSTL-18 CLASS I
DDR_DQ[30]	PIN_AA20	SSTL-18 CLASS I
DDR_DQ[31]	PIN_Y19	SSTL-18 CLASS I
DDR_DQ[32]	PIN_AE18	SSTL-18 CLASS I
DDR_DQ[33]	PIN_AH19	SSTL-18 CLASS I
DDR_DQ[34]	PIN_AJ18	SSTL-18 CLASS I
DDR_DQ[35]	PIN_AH18	SSTL-18 CLASS I
DDR_DQ[36]	PIN_AK18	SSTL-18 CLASS I
DDR_DQ[37]	PIN_AK17	SSTL-18 CLASS I
DDR_DQ[38]	PIN_AK15	SSTL-18 CLASS I
DDR_DQ[39]	PIN_AJ15	SSTL-18 CLASS I
DDR_DQ[4]	PIN_U25	SSTL-18 CLASS I
DDR_DQ[40]	PIN_AH16	SSTL-18 CLASS I
DDR_DQ[41]	PIN_AK14	SSTL-18 CLASS I
DDR_DQ[42]	PIN_AB16	SSTL-18 CLASS I
DDR_DQ[43]	PIN_AA15	SSTL-18 CLASS I
DDR_DQ[44]	PIN_AH15	SSTL-18 CLASS I
DDR_DQ[45]	PIN_AE14	SSTL-18 CLASS I
DDR_DQ[46]	PIN_AK11	SSTL-18 CLASS I
DDR_DQ[47]	PIN_AB13	SSTL-18 CLASS I
DDR_DQ[48]	PIN_AE12	SSTL-18 CLASS I
DDR_DQ[49]	PIN_AG13	SSTL-18 CLASS I
DDR_DQ[5]	PIN_T24	SSTL-18 CLASS I
DDR_DQ[50]	PIN_AH12	SSTL-18 CLASS I
DDR_DQ[51]	PIN_AG10	SSTL-18 CLASS I
DDR_DQ[52]	PIN_AJ10	SSTL-18 CLASS I
DDR_DQ[53]	PIN_AH11	SSTL-18 CLASS I
DDR_DQ[54]	PIN_AG9	SSTL-18 CLASS I
DDR_DQ[55]	PIN_AH8	SSTL-18 CLASS I
DDR_DQ[56]	PIN_AG5	SSTL-18 CLASS I
DDR_DQ[57]	PIN_AK5	SSTL-18 CLASS I
DDR_DQ[58]	PIN_AE3	SSTL-18 CLASS I
DDR_DQ[59]	PIN_AF3	SSTL-18 CLASS I
DDR_DQ[6]	PIN_V27	SSTL-18 CLASS I
DDR_DQ[60]	PIN_AK4	SSTL-18 CLASS I
DDR_DQ[61]	PIN_AJ4	SSTL-18 CLASS I
DDR_DQ[62]	PIN_AJ3	SSTL-18 CLASS I
DDR_DQ[63]	PIN_AH2	SSTL-18 CLASS I
DDR_DQ[7]	PIN_T21	SSTL-18 CLASS I
DDR_DQ[8]	PIN_AA27	SSTL-18 CLASS I
DDR_DQ[9]	PIN_AA25	SSTL-18 CLASS I
DDR_DQS[0]	PIN_W27	SSTL-18 CLASS I
DDR_DQS[1]	PIN_AC25	SSTL-18 CLASS I
DDR_DQS[2]	PIN_AA22	SSTL-18 CLASS I
DDR_DQS[3]	PIN_AD22	SSTL-18 CLASS I

DDR2 signals	FPGA pin	I/O standard
DDR_DQS[4]	PIN_AA17	SSTL-18 CLASS I
DDR_DQS[5]	PIN_AF15	SSTL-18 CLASS I
DDR_DQS[6]	PIN_AH13	SSTL-18 CLASS I
DDR_DQS[7]	PIN_AD9	SSTL-18 CLASS I
DDR_I2C_SDA	PIN_AG7	1.8 V
DDR_I2C_SCL	PIN_AF7	1.8 V
DDR_ODT[0]	PIN_AK21	SSTL-18 CLASS I
DDR_ODT[1]	PIN_AK20	SSTL-18 CLASS I
DDR_RAS_n	PIN_AK13	SSTL-18 CLASS I
DDR_WE_n	PIN_AK19	SSTL-18 CLASS I

6.3.6 FPGA GPIO and LEDs



For debug purposes, LEDs and GPIOs are connected to FPGA. 2 of GPIOs are also connected to buttons. For GPIO use, ensure FPGA internal pull-up is enabled. LEDs and GPIOs are connected to FPGA banks 3, 4 and 5.

FPGA_GPIO[1-8] can be used for connecting LPC bus to FPGA. For this purpose, 0R resistors R1410-R1417 on the bottom layer are to be installed.

LED/GPIO schematic name	FPGA pin (special function)	I/O standard
FPGA_LED1	AK3	1.8 V
FPGA_LED2	AK6	1.8 V
FPGA_LED3	AK7	1.8 V
FPGA_LED4	AK8	1.8 V
FPGA_LED5	AK9	1.8 V
FPGA_LED6	AJ9	1.8 V
FPGA_LED7	AK10	1.8 V
FPGA_LED8	AJ12	1.8 V
FPGA_GPIO1	AF10 (LPC_AD0)	1.8 V
FPGA_GPIO2	AE9 (LPC_AD1)	1.8 V
FPGA_GPIO3	AH9 (LPC_AD2)	1.8 V
FPGA_GPIO4	AE10 (LPC_AD3)	1.8 V
FPGA_GPIO5	AF13 (LPC_FRAME#)	1.8 V
FPGA_GPIO6	AA12 (LPC_SERIRQ)	1.8 V
FPGA_GPIO7	AB11 (LPC_RESET#)	1.8 V
FPGA_GPIO8	AK16 (LPC_CLK_CPLD)	1.8 V

FPGA_GPIO9	AJ25 (button SW10)	1.8 V
FPGA_GPIO10	AG27	1.8 V
FPGA_GPIO11	AG26	1.8 V
FPGA_GPIO12	AH28	1.8 V
FPGA_GPIO13	AK27	1.8 V
FPGA_GPIO14	AH29 (button SW9)	1.8 V

6.3.7 FPGA clock sources

PCIE_CLK_REF signals are provided by U26 (clock buffer), CLK_100MHz_1V8 signals are provided by U95, U100 and U101 and can be used as global clock signals for FPGA device.

CLK schematic name	FPGA pin	I/O standard	Frequency	Notes
CLK_100MHz_1V8	AJ16	1.8 V	100 MHz	
CLK_100MHz_1V8_2	V29	1.8 V	100 MHz	
CLK_100MHz_1V8_3	V30	1.8 V		DNI by default
FPGA_GPIO8 (LPC_CLK_CPLD)	AK16	1.8 V	33.3 MHz	Available if LPC is connected
PCIE_CLK_REF2+	L11	HSCL	100 MHz	
PCIE_CLK_REF2-	K11			
PCIE_CLK_REF6+	M10	HSCL	100 MHz	
PCIE_CLK_REF6-	L10			
PCIE_CLK_REF7+	V11	HSCL	100 MHz	
PCIE_CLK_REF7-	W11			
LVDS_A_CK_FPGA+	T29	LVDS	variable	Available if LVDS is connected
LVDS_A_CK_FPGA-	T30			

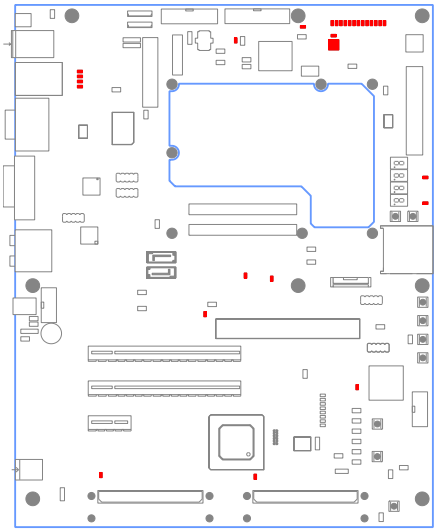
6.3.8 FPGA reset

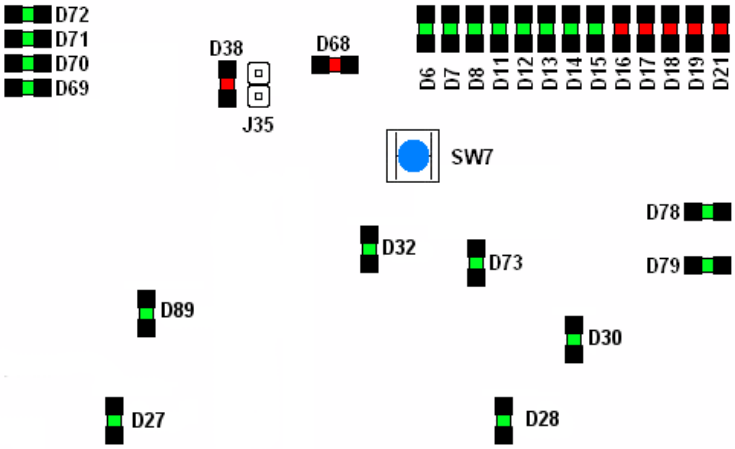
FPGA_RESET_1V8# signal is provided by U40 (reset buffer) and can be used as global reset signal for FPGA device. It is the same reset as CB_RESET/LPC reset/PCIe reset.

Schematic name	FPGA pin	I/O standard
FPGA_RESET_1V8#	AF27	1.8 V

6.4 Status LED

The onboard main status and voltage LED D6-D21 indicates the current power state of the module and if all voltages are working correctly. Some additional status LED shows active or inactive slots and signals. See table below for detailed information.



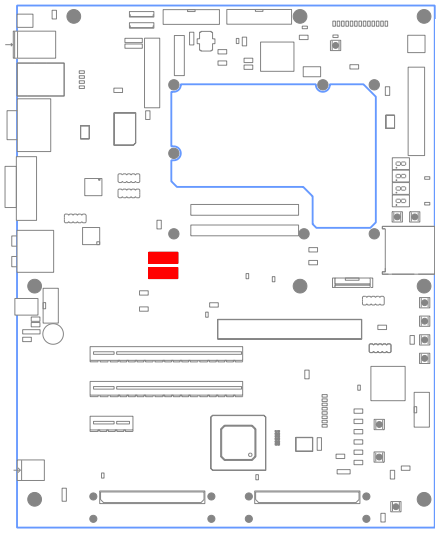


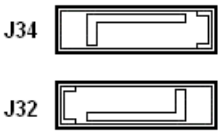
A front panel HDD LED can be connected HDD Activity connector J35. D68 indicates an active watchdog trigger WDT. The output is buffered and the switch SW7 resets the Latch. LEDs D27 and D28 indicates the presence of HSMC cards.

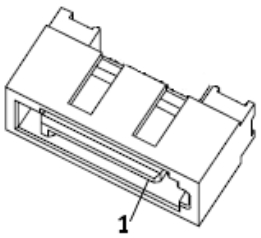
LED	Description	LED	Description
D6	VCC 3.3V	D27	HSMC1 present
D7	VCC 5V	D28	HSMC2 present
D8	VCC 5V SBY	D89	DDR2 Supply voltage
D11	VCC 12V Module	D32	USB Blaster status LED
D12	VCC 12V	D38	HDD activity
D13	VCC 3.3V SBY	D68	latched WDT
D14	VCC 1.0V	D69	GBLAN Activity
D15	VCC 1.5V	D70	GBLAN Link 10
D16	SUS_STAT#	D71	GBLAN Link 100
D17	SUS_S3#	D72	GBLAN Link 1000
D18	SUS_S4#	D73	Type10 detection
D19	SUS_S5#	D78	VCC 1.8V
D21	THRMTRIP	D79	VCC 3.3V for Silicon Image SIL1364

6.5 Serial ATA

The COM Express® Type 10 pin-out specification according to COM.0 specification revision 2.0 defines 2 SATA ports. The COM Express® FPGA Evaluation Board provides two 7-pin SATA data connectors as standard 1.27mm Pitch Serial ATA High Speed Header with Locking Latch.







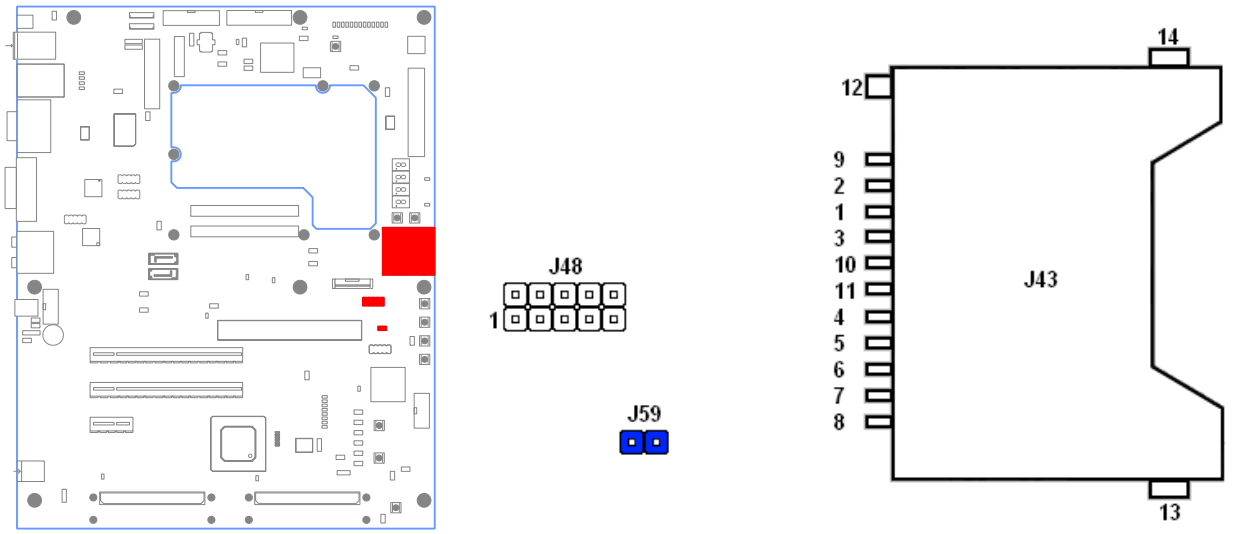
SATA Pin	Signal
1	Ground
2	Transmit +
3	Transmit -
4	Ground
5	Receive -
6	Receive +
7	Ground

Connector	SATA Port
J32	SATA #0
J34	SATA #1

6.6 SD-Card / Module GPIO

The SD-Card standard is a standard for removable memory storages designed and licensed by the SD Card Association (http://sdcard.org). The card form factor, electrical interface and protocol are all part of the SD Card specification. COM Express® Type 1 and Type 10 pin-out based modules may provide a SDIO interface shared with GPIO signals. Therefore on COM Express® FPGA Evaluation Board a SD-Card connector is available. Please check the documentation of your module if SDIO is supported and how to enable.

Close configuration jumper J59 (default) to enable SD-Card Slot J43 or open J59 to enable GPIO pin-header J48.



SD-Card J43 PIN	Description	SD-Card J43 PIN	Description
1	DAT3/CD - Data Line 3/Card Detection	8	DAT1 - Data Line 1
2	CMD - Command/Response	9	DAT2 - Data Line 2
3	VSS 1 - Supply Voltage - GND	10	Card Detect
4	VDD - Supply Voltage - 3.3V	11	Write Protect
5	CLK - Clock	12	COM (GND)
6	VSS2 - Supply Voltage - GND	13	Shield Ground 0
7	DAT0 - Data Line 0	14	Shield Ground 1

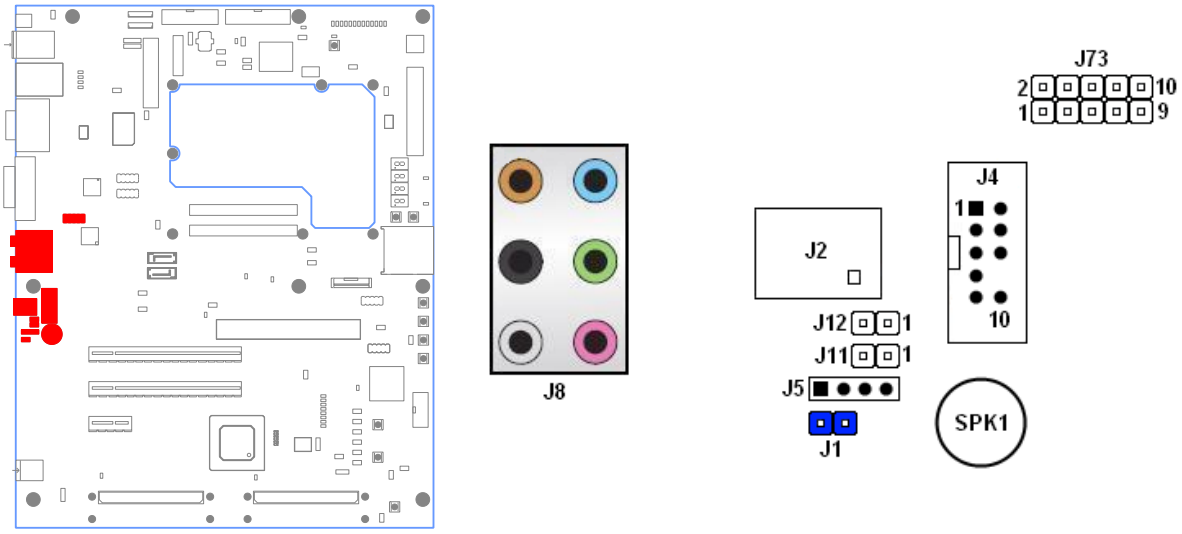
GPIO J48 PIN	Description	GPIO J48 Pin	Description
1	VCC 3.3V	2	GPO0 / SD_CLK
3	GPI0 / SD_DATA0	4	GPO1 / SD_CMD
5	GPI1 / SD_DATA1	6	GPO2 / SD_WP
7	GPI2 / SD_DATA2	8	GPO3 / SD_CD#
9	GPI3 / SD_DATA3	10	GND

Note: A SD-Card is detected if Card Detect is at low level. The write protection is active (read only) if SD_WP is at high level.

6.7 High Definition Audio

The COM Express® FPGA Evaluation Boards provides HDAudio via Realtek ALC888 High Definition Audio Codec supporting analog, optical and digital audio connections.

The onboard buzzer SPK1 can be disabled by opening jumper J1 (default closed). Optical S/PDIF for Toslink connection is available on rear panel connector J2.



Audio Connector J8 - Speaker Configuration

The Audio Connector J8 on COM Express® FPGA Evaluation Board is a full featured analog audio jack for speaker configuration up to 8-channel.

J8	2-channel	4-channel	6-channel	8-channel
Orange	-	-	Center/Subwoofer	Center/Subwoofer
Black	-	Rear Speaker	Side Speaker	Rear Speaker Out
Gray	-	-	-	Side Speaker Out
Blue	Line In	Line In	Line In	Line In
Green	Line Out	Front Speaker	Front Speaker	Front Speaker
Pink	Mic In	Mic In	Mic In	Mic In

Note1: In addition to the default speaker settings, the analog audio Jacks can be reconfigured to perform different functions via the Realtek HDAudio Driver Software which is available on Kontron website. Only microphones still must be connected to the default pink jack.

Note2: Audio is only supported with HD Audio compatible COM Express® Modules.

Front Panel Audio Connector J4

The front panel audio connector J4 allows connecting a chassis front panel audio with analog microphone input and stereo speaker output.

Pin	Description
1	MIC2-L
2	GND
3	MIC2-R (MIC Power)
4	PRESENCE#
5	LINE2-R (LineOut-R)
6	MIC2-JD
7	SENSE
8	Key Pin
9	Line2-L (LineOut-L)
10	LINE2-JD

Digital Audio Connectors J5/J11/J12

Digital audio inputs and outputs are available on connector J11 (S/PDIF input), J12 (S/PDIF output) and microphone connection on J5.

Pin	J5 (HDA GPIO / Dig. MIC)	J11 (S/PDIF in)	J12 (S/PDIF out)
1	HDA_GPIO0 / DMIC-CLK	SPDIF_II	SPDIF_OUT
2	HDA_GPIO1 / DMIC-DATA	GND	GND
3	PWR_3.3V	-	-
4	GND	-	-

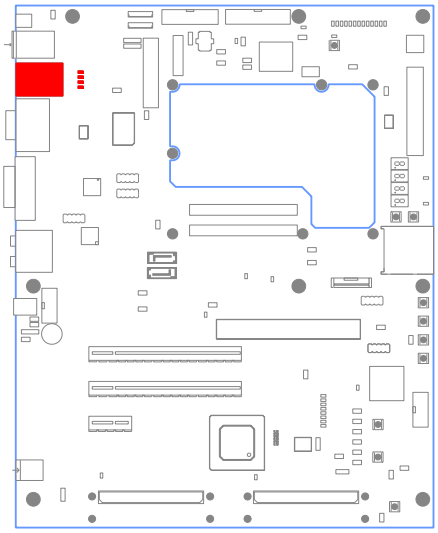
Codec connector J73

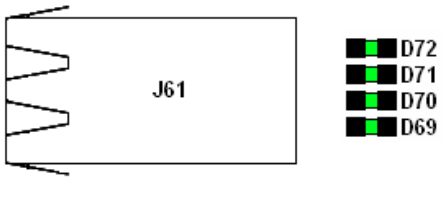
Connector J73 allows access to HD Audio interface to connect external HDAudio codec additional to the onboard Realtek ALC888.

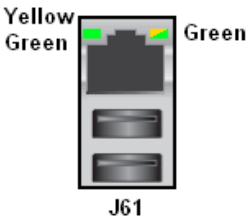
Pin	Description	Pin	Description
1	HDA_BITCLK	2	GND
3	GND	4	HDA_SDIN1
5	HDA_SDIN0_R (default n.c.)	6	HDA_SDIN2
7	GND	8	HDA_SYNC
9	HDA_SDOUT	10	HDA_RST#

6.8 Ethernet

The COM Express® FPGA Evaluation Board provides a RJ45/Dual USB Combo with a single RJ45 in combination with 2 USB ports (USB 4/6). Ethernet Connector J61 with integrated magnetics and LED is configured to support modules with Gigabit Ethernet controller only. Modules with 10/100 MBit Ethernet controller are not supported.







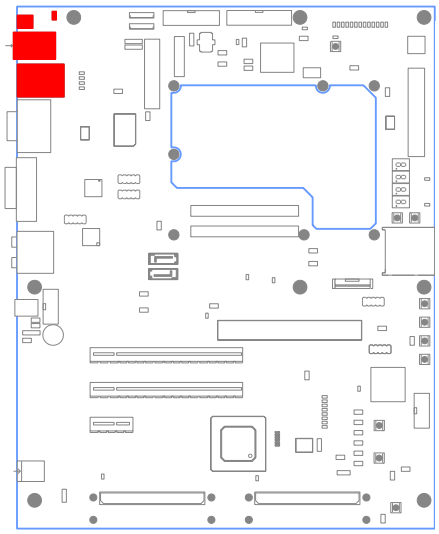
J61 LED function

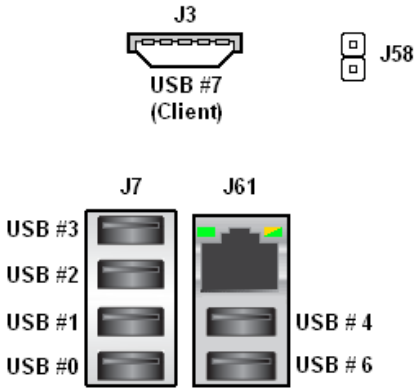
Function	J61 Left LED	J61 Right LED	Status LED
Activity	Green	-	D69
Link10	-	Off	D70
Link100	-	Yellow	D71
Link1000	-	Green	D72

6.9 USB

The COM Express® module's USB ports 0 to 3 are available on rear panel connector J7. USB port 5 is used on Express Card connector. The COM Express® FPGA Evaluation Board provides USB port 4 and 6 on RJ45/USB Combo connector J61.

Additionally USB7 is available on USB mini-A connector J3 as non-powered connector for USB client functionality. Check the documentation of your module if USB client on Port #7 is supported and J3 can be used. J58 allows connecting USB Client Power to GPIO to use it as detection input for custom USB Client driver software.

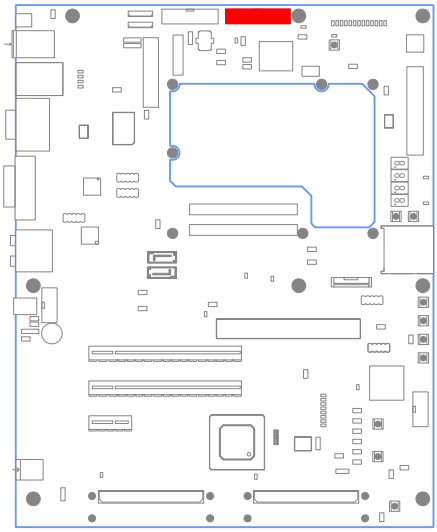


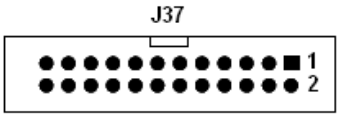


USB Client connectorJ3 - Pin	J3 Function
1	USB Client Power detect
2	USB7-
3	USB7+
4	n.c.
5	GND
6-9	Shield GND

6.10 Kontron Feature connector

The Kontron Feature connector provides additional interfaces such as I2C, SMBus or Power Control Signals. See the table below for detailed pin-out description



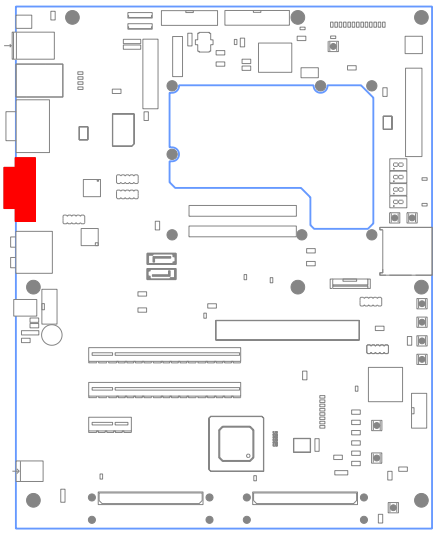


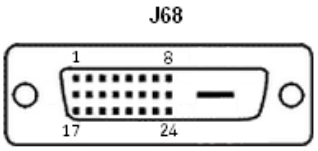
Pin	Signal	Level	Signal Description
1	PWR_+5V	5V power	+5V UL-protected with inductor (600R@100MHz, 1A)
2	GPO2	3.3V-O	General-purpose power management event output
3	#BATLOW	3.3V-I	Battery low input. May be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power management event.
4	GPI2	3.3V-I	General-purpose power management event input
5	#SYS_RESET	3.3V-I	This input may be driven low by external circuitry in order to reset the power management logic
6	WDT	3.3V-O	Indicating that a Watchdog Timeout Event has occurred (non buffered module output)
7	LPC_SERIRQ	3.3V-I	Serial interrupt request. This pin is used to support the serial interrupt protocol.
8	-	-	Not connected
9	I2C_DAT	3.3V-IO	Data line of I2C-Bus
10	#SMB_ALERT	3.3V-I	System Management Bus Alert input. May be driven low by SMB devices in order to signal an event on the SM Bus
11	I2C_CLK	3.3V-O	Clock line of I2C-Bus
12	SMB_DAT	3.3V-IO	Clock and data line of SM-Bus.
13	SMB_CLK	3.3V-O	
14	-	-	Not connected
15	#WAKE1	3.3V-I	Low driven general purpose wake-up signal
16	VCC_RTC	3V-I	3V backup cell input. Should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VBATT = 2.4 – 3.3V)
17	#THRM	3.3V-I	Input from off-module temperature sensor indicating an over temperature situation
18	GND	GND	Ground
19	PWR_OK	3.3V-I	High active input indicating that power from the power supply is ready. It can also be used as low active reset input signal.
20	GND	GND	Ground

21	#PWRBTN	3.3V-I	Power Button Input. This input is used to support the ACPI Power Button function.
22	GND	GND	Ground
23	#ATA_ACT	3.3V-O	Low active output signal, which indicates activity on IDE interfaces.
24	#CB_RESET	3.3V-O	Low active Reset output from module to carrier board

6.11 DVI-D

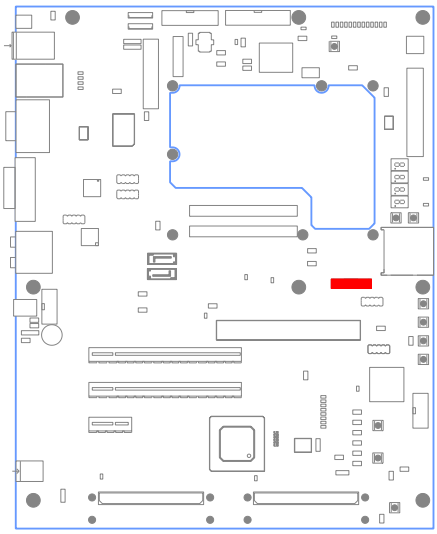
On COM Express® FPGA Evaluation Board the DVI output is available through a Silicon Image SiL1364/A SDVO to single link DVI PanelLink Transmitter. Check your module documentation if SDVO is available on DDI interface defined for Type 10 pin-out based modules or if SDVO is available on PEG multiplexed lanes for Type 2 pin-out based module.

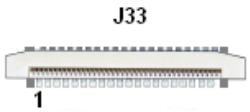




6.12 LVDS

The 40-pin JILI LVDS panel connector J33 allows connecting a flat panel directly to the module's dual channel LVDS output. Check your module documentation for available BIOS configurations for this flat panel output. LVDS signals can lead to FPGA as strap option.





Pin	LVDS Signal	Pin	LVDS Signal
1	NC	21	LCDDO13
2	LCDDO0	22	DETECT# (GND)
3	LCDDO1	23	LCDDO14
4	ENAVDD	24	LCDDO15
5	LCDDO2	25	GND
6	LCDDO3	26	LCDDO16
7	NC	27	LCDDO17
8	LCDDO4	28	GND
9	LCDDO5	29	LCDDO18
10	GND	30	LCDDO19
11	LCDDO6	31	+5V
12	LCDDO7	32	+5V
13	GND	33	+5V
14	LCDDO8	34	+5V
15	LCDDO9	35	BLON#
16	JILI_DAT	36	GND
17	LCDDO10	37	GND
18	LCDDO11	38	+12V
19	JILI_CLK	39	+12V
20	LCDDO12	40	+12V

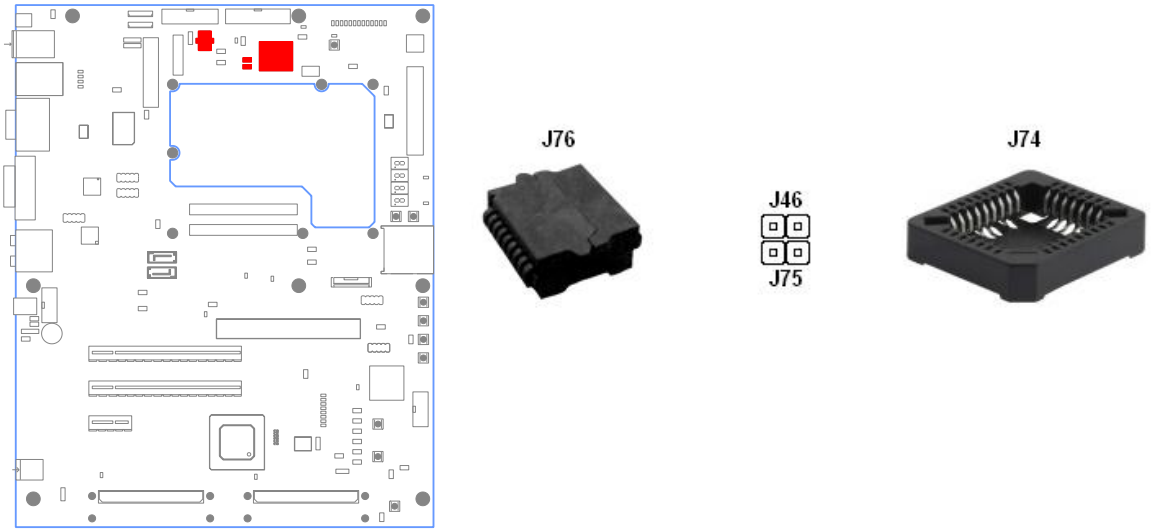
LVDS_A[0-3,_CK]_FPGA can be used for connecting LVDS video from module to FPGA. For this purpose, 0R resistors R1252-R1261 on the bottom layer are to be installed.

LVDS Video from module to FPGA	FPGA pin	I/O standard
LVDS_A0_FPGA+	D25	LVDS
LVDS_A0_FPGA-	C25	
LVDS_A1_FPGA+	E24	LVDS
LVDS_A1_FPGA-	D24	
LVDS_A2_FPGA+	D26	LVDS
LVDS_A2_FPGA-	C26	
LVDS_A3_FPGA+	A26	LVDS
LVDS_A3_FPGA-	A25	
LVDS_A_CK_FPGA+	T29	LVDS
LVDS_A_CK_FPGA-	T30	
LVDS_I2C_DAT_FPGA	B24	1.8 V
LVDS_I2C_CK_FPGA	C24	1.8 V

6.13 External BIOS

The COM Express® FPGA Evaluation Board supports external boot. By closing Jumper J46 the module's onboard BIOS is disabled and the system will boot from an external Firmware Hub in U43 PLCC socket J74.

For modules supporting SPI boot the COM Express® FPGA Evaluation Board provides a SPI socket J76 for an optional available SPI Flash. SPI is part of COM.0 Specification Rev 2.0 and external SPI boot can be enabled by closing Jumper J75. Please check the documentation of your module if SPI is supported and which SPI Flash size is required.



Booting from external BIOS:

» Close Jumper J46 to boot from the baseboard's LPC Firmware

» Close Jumper J75 to boot from the baseboard's SPI Flash

Flashing the external BIOS:

» Prepare a bootable USB flash drive and save BIOS and flash utility in the root folder

Please check Application Note KEMAP046 avialble at Kontron's customer section for more details

» Open J46/J75 to boot from the module's BIOS

» Power on the system and boot from our USB flash drive

» Close J46 to enable the LPC FWH or close J75 to enable the SPI Flash

» Execute the BIOS update command (e.g. afudos.exe bios.rom /P /B /N /C /X)

» Reboot your system if flash procedure has finished

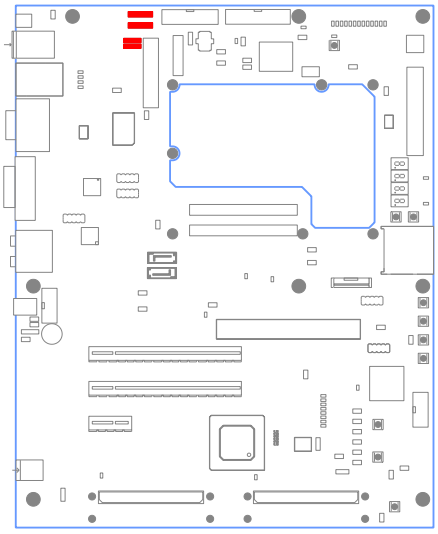
» Your system should now start from external BIOS

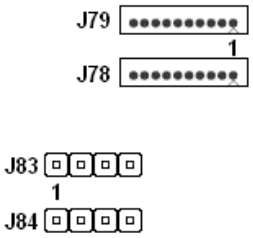
Note:	Please check module documentation if external boot from LPC FWH and/or SPI Flash is supported

Warning: Do not close both jumpers at the same time

6.14 Serial Interface

The PICMG COM.0 specification revision 2.0 defines two optional 2-pin serial interfaces on COM Express® connector pins A98/A99 and A101/A102 formerly used for 12V VCC input. Both new interfaces are available directly on optional pin-header J83 and J84.



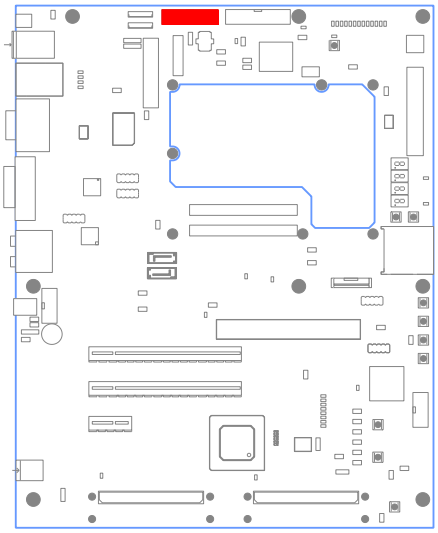


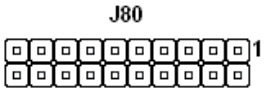
J78 and J79 allow both interfaces to be used as 2-pin RS232 interfaces COMA and COMB with Kontron Adapter cable KAB-DSUB9-2. Please check the documentation of your module if this interface is supported and how to configure.

Pin	J78 (COMA)	J79 (COMB)	J83 (SER0, A98/99)	J84 (SER1, A101/102)
1	n.c.	n.c.	+5V	+5V
2	n.c.	n.c.	SER0_TX	SER1_TX
3	RX0	RX1	SER0_RX	SER1_RX
4	n.c.	n.c.	GND	GND
5	TX0	TX1	-	-
6	n.c.	n.c.	-	-
7	n.c.	n.c.	-	-
8	n.c.	n.c.	-	-
9	GND	GND	-	-
10	+5V	+5V	-	-

6.15 Status & Debug Connector

For debugging and measurements some important status signals are available on pin-header J80 for direct access.

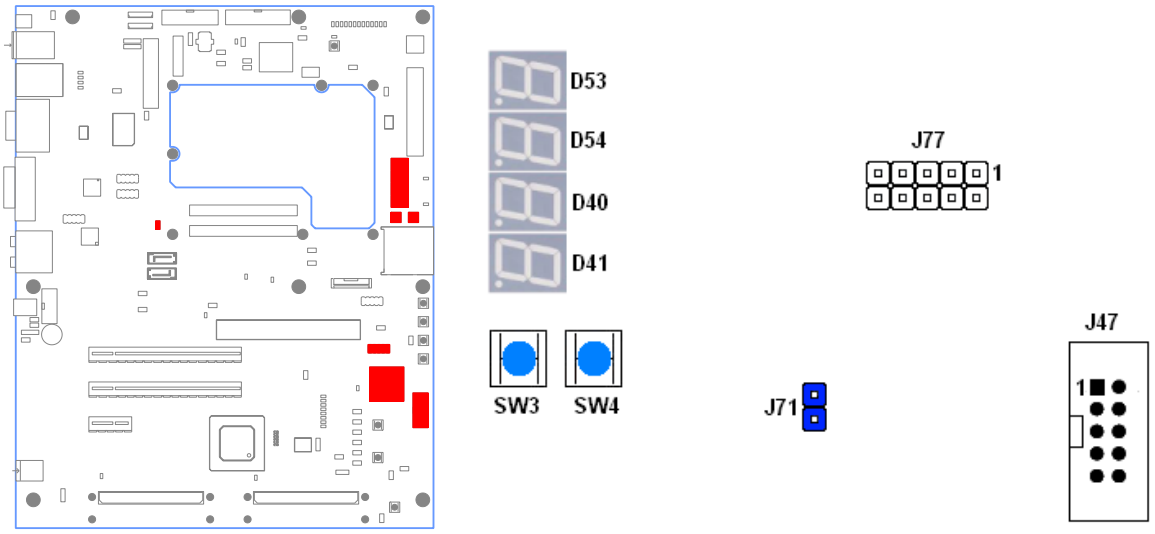




Pin	Description	Pin	Description
1	+3.3V SBY	2	GND
3	TPM_PP	4	SUS_STAT#
5	WDT_LATCHED	6	SUS_S3#
7	RST_WDT_L#	8	SUS_S4#
9	SPKR	10	SUS_S5#
11	EXCD0_CPPE#	12	GBE0_ACT#
13	EXCD0_PERST#	14	GBE0_LINK100#
15	EXCD1_CPPE#	16	GBE0_LINK1000#
17	EXCD1_PERST#	18	GBE0_LINK#
19	+3.3V	20	GND

6.16 CPLD & POST-Code Display

Power Management control, 4 digits LPC/PCI Port 80/81 Post Code and additional GPIOs are implemented in onboard Altera CPLD (U44).



Port 80/81 POST Code display

The 7-segment display D53/D54 for Port 81 and D40/41 for Port 80 shows BIOS status codes during boot-up process. Last 8 check codes are stored automatically and can be controlled by switch SW3 (Post Code step backward) and switch SW4 (Post code step forward). Pressing SW3 and SW4 simultaneously returns to newest POST code.

The POST Code display also shows current Suspend state:

- S3 -> POST code "_ _ _ 3"
- S4/S5 -> POST code "_ _ _ 5"

Power Good J71

The Power Good output generated by the CPLD must be high level to allow the module to start. Some modules may provide direct power-on support if VCC gets connected and PWR_OK (COM Exress pin B24) is open or at high level. To test this functionality configuration jumper J71 can be opened to disconnect Power Good.

J77 - CPLD I/O Port

The I/O Port J77 provides 8 I/O ports directly from the CPLD without any functionality in default configuration.

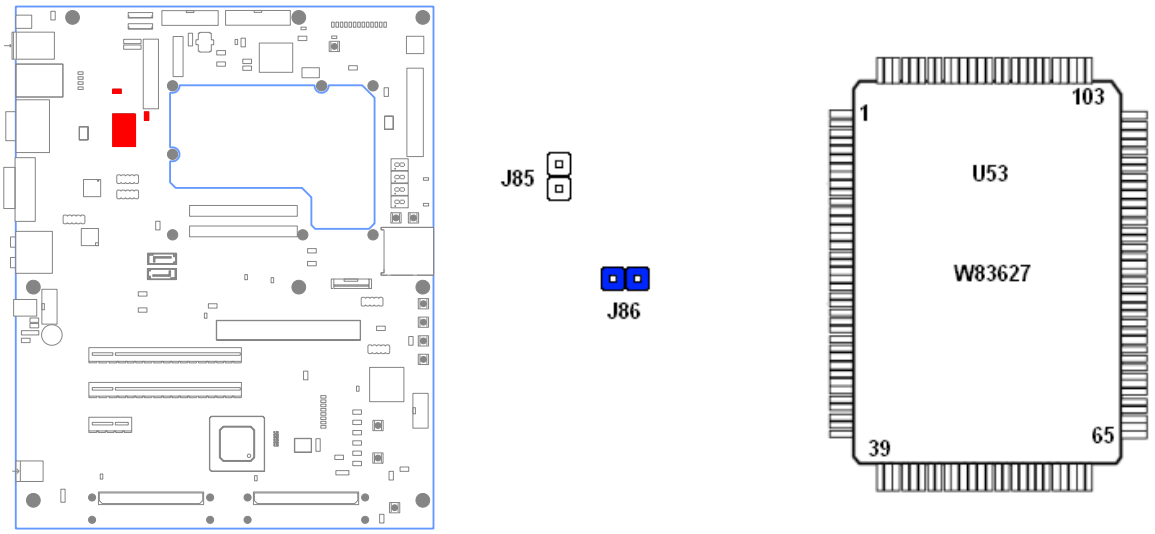
J7 pin	Function	J7 pin	Function
1	VCC 3.3V SBY	2	GND
3	CPLD_IO_PIN64	4	CPLD_IO_PIN66
5	CPLD_IO_PIN67	6	CPLD_IO_PIN68
7	CPLD_IO_PIN69	8	CPLD_IO_PIN70
9	CPLD_IO_PIN71	10	CPLD_IO_PIN72

J47 - CPLD JTAG Connector

J7 pin	Function	J7 pin	Function
1	TCK (PD 1K0)	2	GND
3	TDO (PU 1K0 3.3VSBY)	4	3.3V SBY
5	TMS (PU 1K0 3.3VSBY)	6	n.c.
7	n.c.	8	n.c.
9	TDI (PU 1K0 3.3VSBY)	10	GND

6.17 Winbond 83627 Super-I/O

A Winbond 83627HFJ Super-I/O controller (U53) is connected to module's LPC bus to offer legacy interfaces like RS232 and parallel ports additionally to temperature, FAN and voltage monitoring features. The default SIO LPC address is 2Eh.

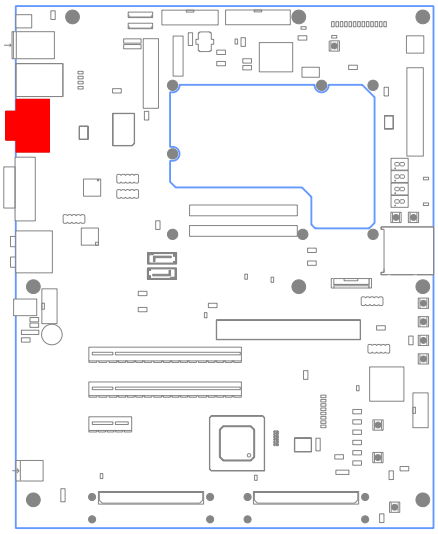


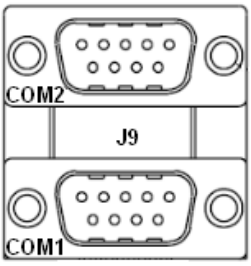
The configuration jumpers J85 enables the SIO keyboard controller when closed. Open J86 to hold the Super-I/O in reset to simulate a legacy free backplane.

Note:	A LPC Super-I/O controller requires BIOS support. Please check the documentation of your module if the Winbond 83627 is supported.

6.17.1 RS232

With Winbond 83627 LPC-I/O two serial ports are supported. Both COM ports can be configured in module BIOS setup if Super-I/O support is implemented.

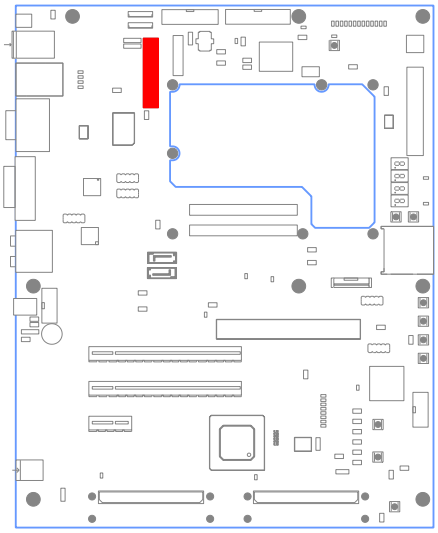


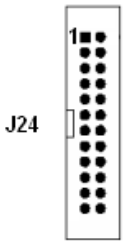


Pin	Signal
1	DCD
2	RX
3	TX
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

6.17.2 LPT

The Winbond 83627 LPC-I/O supports one parallel port available on baseboard's pin header J24. Use the optional available KAB-DSUB25-1 cable adapter to access the LPT port and check to module BIOS to configure the port resources.

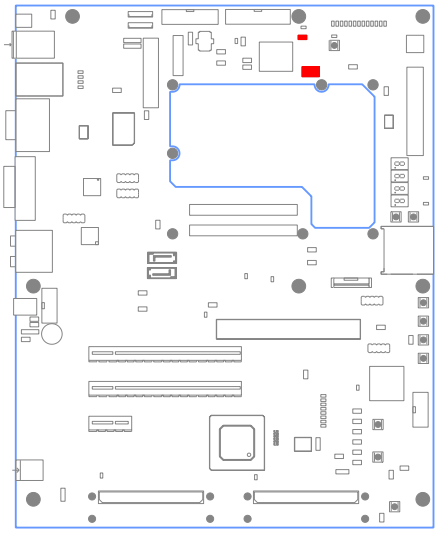


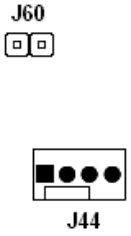


Pin	Signal	Pin	Signal
1	#STB	2	#AFD
3	PD0	4	#ERROR
5	PD1	6	#INIT
7	PD2	8	#SLCTIN
9	PD3	10	GND
11	PD4	12	GND
13	PD5	14	GND
15	PD6	16	GND
17	PD7	18	GND
19	#ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	n.c.

6.17.3 FAN

The COM Express® FPGA Evaluation Board provides one 4-pin PWM FAN connector directly controlled by the LPC-I/O PWM output 1. If configuration jumper J60 is open (default) the PWM FAN J44 is controlled by the module FAN output specified in COM.0 revision 2.0 specification if supported by the module.

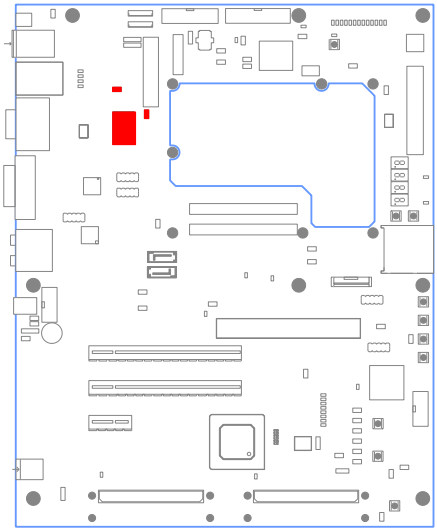


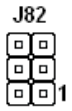


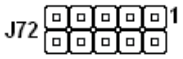
Pin	J50 on COM Express® FPGA Evaluation Board 2.0
1	GND
2	+12V
3	Sense
4	Control (PWM)

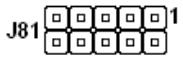
6.17.4 SIO Debug connectors

For debugging Winbond 83627 LPC-I/O GPIOs and FAN/Voltage interfaces are available via pin-header.









Pin	J72 - GPIO	J81 - FAN	J82 - Voltage
1	+5V	+3.3V	SIO HWM IN - VCOREA
2	GND	GND	SIO HWM IN - 12V
3	SIO GP10 / JOAYABTN0	Module FAN_PWMOUT#	SIO HWM IN - VCOREB
4	SIO GP11 / JOYBBTN0	Module FAN_TACHIN	SIO HWM IN - -5V
5	SIO GP12 / JOYAX	SIO HWM OUT - FANPWM1	SIO HWM IN - 3.3V
6	SIO GP13 / JOYBX	SIO HWM IN - FANIO1	GND
7	SIO GP14 / JOYBY	SIO HWM OUT - FANPWM2	-
8	SIO GP15 / JOYAY	SIO HWM IN - FANIO2	-
9	SIO GP16 / JOYBBTN1 SIO GP20 / MDRX	SIO HWM OUT - FANPWM3	-
10	SIO GP17 / JOYABTN1 SIO IRQIN / MDTX0	SIO HWM IN - FANIO3	-

Note: Check the module's BIOS how to enable the baseboard hardware monitor for monitoring voltages and fan revolutions via JIDA32/K-Station or in BIOS HWM setup page.

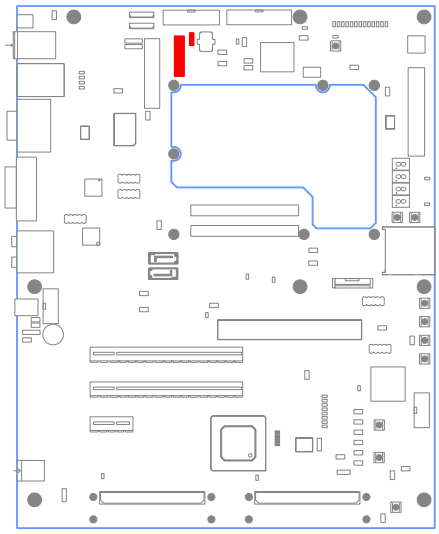
SIO GPIO are not accessible via JIDA interface.

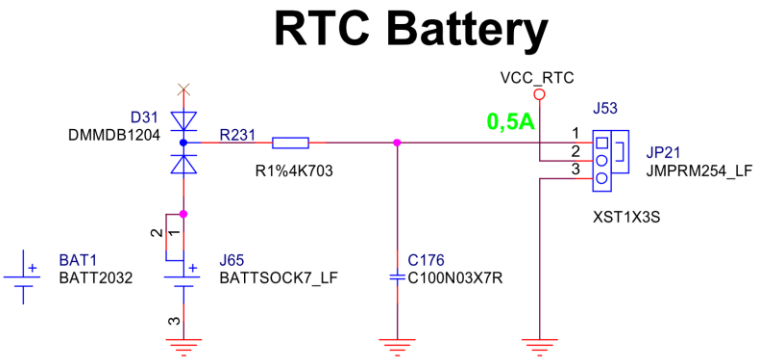
6.18 FRU-PROM (I2C EEPROM)

Following the new COM Express® specification the COM Express® FPGA Evaluation Board 2.0 provides an I2C EEPROM. The FRU-PROM (Field Replacable Unit; U76) at I2C address 07h can be used to store user specific data or baseboard configuration settings.

7 Battery Information

System RTC circuit can be powered from 2032 battery or can be tied to ground. This selection is done with jumper position on J53.





English:

CAUTION:	Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Deutsch:

VORSICHT:	Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

French:

ATTENTION:	Risque d'explosion avec l'échange inadéquat de la batterie. Remplacement seulement par le même ou un type équivalent recommandé par le producteur. L'évacuation des batteries usagées conformément à des indications du fabricant.

Danish:

ADVARSEL:	Lithiumbatteri – Eksplosionsfare ved fejlagtig Håndtering. Udskifting må kun ske med batteri af samme fabrikant og type. Lever det brugte batteri tilbage til leverandøren.

Finnish:

VAROITUS:	Paristo voi rãjähtãã, jos se on virheellisesti asennettu. Vaihda paristo ainoastaanlaltevalmistajan suosittelmaan tyyppiln. Havita kaytetty paristo valmistajan ohjeiden mukaisesti.

Spanish:

Precaución:	Peligro de explosión si la batería se sustituye incorrectamente. Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante. Disponga las baterías usadas según las instrucciones del fabricante.

Note:	The battery of this product is not considered to be accessible by the end user. Therefore the safety instructions are only given in English, German, French, Danish, Finish and Spanish language. If the battery of this product however is accessible by the end user, it is in the responsibility of the Kontron customer to give the corresponding safety instructions in the required language(s).

8 Module Single Supply and Wide Range

The Computer-on-Module power is supplied directly from ATX_12V connector J15. Kontron modules are capable of working in a wide range voltage input and therefore it's possible to connect module VCC on J15 parallel to ATX supply J22 for the baseboard.

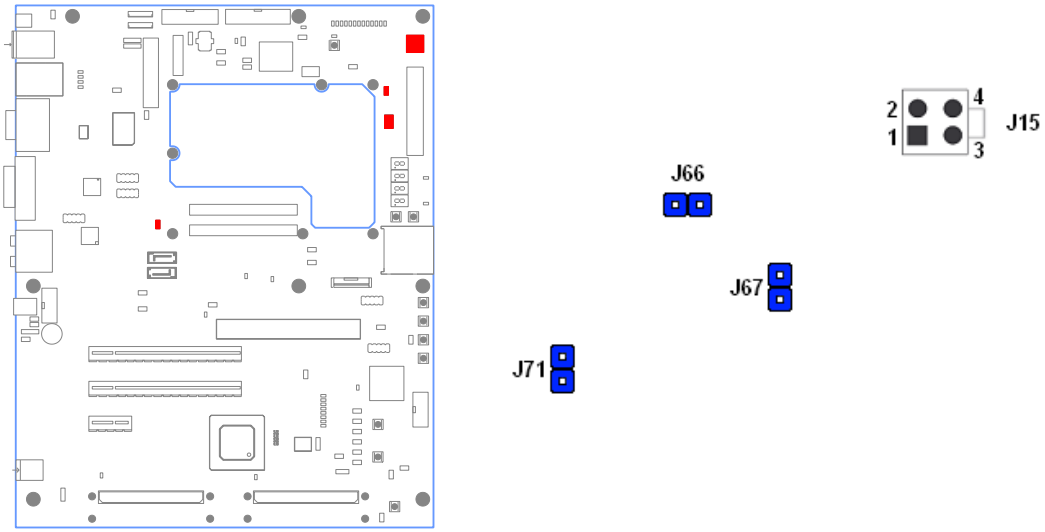
Please check the documentation of your product if a wide range voltage input is supported. Kontron Computer-on-Modules usually supports:

» COM Express® modules in ultra size form factor (nanoETXexpress):

4.75V to 14V

» COM Express® modules in compact and basic size form factor (microETXexpress® and ETXexpress®)

8.5V to 18V



Additionally Kontron modules support single supply operation without standby voltage. To enable module single supply mode open jumper:

» J66 to enable Baseboard's S5Eco mode

» J67 to disconnect 5VSB from the module

» J71 to disconnect Power Good (PWR_OK)

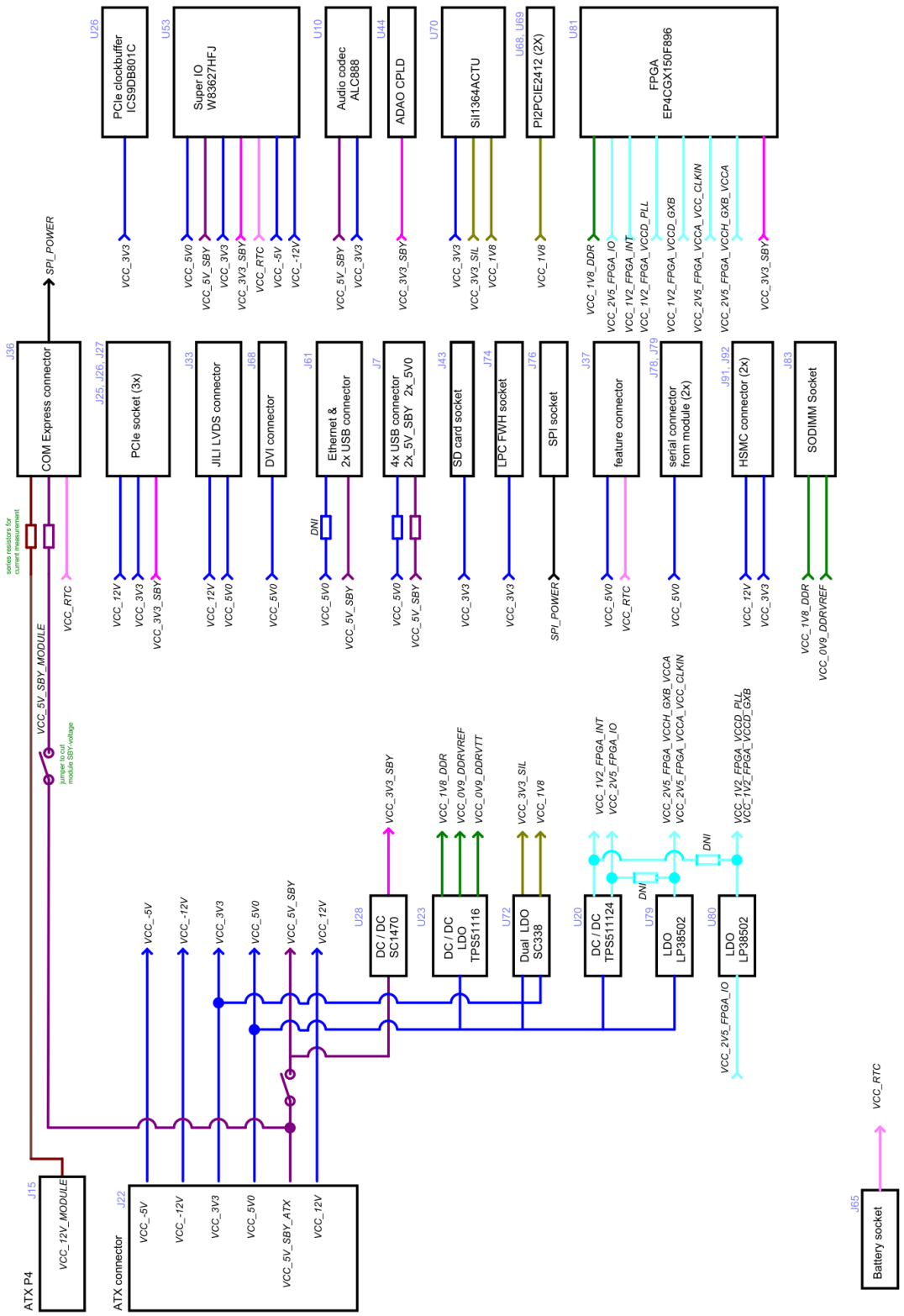
9 Compatibility Matrix

The COM Express® FPGA Evaluation Board supports Computer-on-Modules following PICMG COM.0 Revision 1.0 pin-out Type 1, COM.0 revision 2.0 pin-out Type 10 or COM.0 revision 2.0 pin-out Type 2.

See table below wich features are supported by Kontron's COM Express® mini form factor modules 'nanoETXexpress':

Con	Feature	nanoETXexpress-SP (Type1)	nanoETXexpress-TT (Type10)
J15	ATX 12V Power	4.75V - 14V	4.75V - 14V
J34	SATA1	on variants without onboard LAN	YES
J61	USB #4 / USB #5 Ethernet RJ45	USB #4: USB 2.0 only	No USB #6
J44	PWM FAN (SIO/Module)	from SIO only	from SIO only
J68	DVI-D (SDVO2DVI)	Optional	YES
J74	LPC FWH for external BIOS	YES	If SIO is disabled
J76	SPI Flash for external BIOS	NO	YES
J78	RS232 COMA from module	NO	YES
J79	RS232 COMB from module	NO	YES
J83	SER0 from module	NO	YES
J84	SER1 from module	NO	YES
SW5	LID	NO	YES
SW6	SLEEP	NO	YES

10 Power Distribution



11 Security Advice

To protect the external power lines to peripheral devices the customer has to take care about:

- The wires to the external device have the right diameter to withstand the max. available current

- The housing of the external device fulfils the fire protection requirements of IEC/EN 60950.

12 Document Revision History

Revision	Date	Edited by	Changes
0.10	8.11.2010	JB	Initial Release
0.2	29.3	JB	Picture update, general check, add chapter FPGA LEDs and GPIOs
0.3	20.06.2011	SGE	Definition correction and Trademark check
1.0	20.10.2011	UMA	Updated according to ADAP_manual_L111_110805 by JB
1.1	14.06.2012	JB, MP	Updated and added FPGA pin tables
1.2	25.06.2012	MP, UMA	Updated FPGA pin table J92, formatting, corrected product name

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