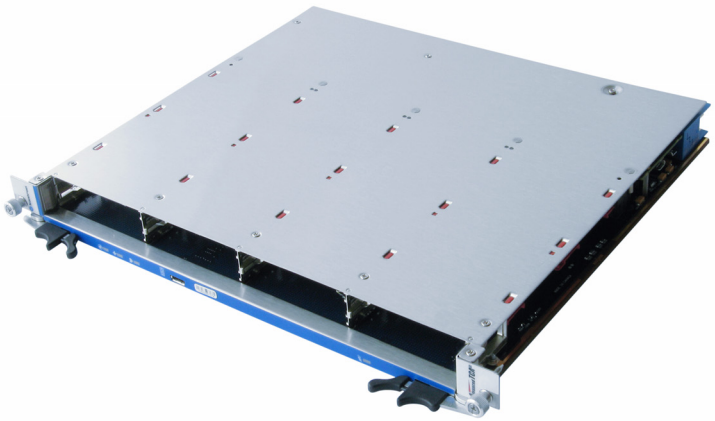
»Kontron User's Guide«

AT8404



Document Revision 1.6

Document ID: AT8404

Issue Date: 16 March, 2010

If it's embedded, it's Kontron.

Revision History

Rev. Index	Brief Description of Changes	Date of Issue
1.0	Initial Issue	9 January, 2008
1.1	Rework on chapter 4 (Software description) and chapter 1.3 (Software support), add chapter 3.2 (RTM8030)	29 February, 2008
1.2	Added Note in chapter 3.2	2 December, 2008
1.3	Rework covering SW update for FASTPATH 5.2 and WindRiver PNE 2.0	15 May, 2009
1.4	Pre-Release with major Rework in chapter 4	25 September, 2009
1.5	New Kontron outfit, chapter 4.5 and 4.6 added, chapter 5 added, major rework in chapter 4.2 and 4.3	03 November, 2009
1.6	Add chapter for OEM sensors, rework sensor list, rework PLD update chapter	16 March, 2010

Customer Service

Contact Information:

Kontron Canada, Inc.
4555 Ambroise-Lafortune
Boisbriand, Québec, Canada
J7H 0A4
Tel: (450) 437-5682
(800) 354-4223
Fax: (450) 437-8053
E-mail: support@ca.kontron.com

Kontron Modular Computer GmbH
Sudetenstrasse 7
87600 Kaufbeuren
Germany
+49 (0) 8341 803 333
+49 (0) 8341 803 339
support-kom@kontron.com

Visit our site at:www.kontron.com

Table of Contents

List of Tables

List of Figures

Proprietary Note

This document contains information proprietary to Kontron AG. It may not be copied or transmitted by any means, disclosed to others, or stored in any retrieval system or media without the prior written consent of Kontron AG or one of its authorized agents.

The information contained in this document is, to the best of our knowledge, entirely correct. However, Kontron AG cannot accept liability for any inaccuracies or the consequences thereof, or for any liability arising from the use or application of any circuit, product, or example shown in this document.

Kontron AG reserves the right to change, modify, or improve this document or the product described herein, as seen fit by Kontron AG without further notice.

Trademarks

Kontron AG and the *Kontron* logo are trade marks owned by Kontron AG, Germany. In addition, this document may include names, company logos and trademarks, which are registered trademarks and, therefore, proprietary to their respective owners.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Explanation of Symbols

CAUTION

This symbol and title indicate potential damage to hardware and tells you how to avoid the problem.

CAUTION

Electric Shock

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

WARNING

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

ESD Sensitive Device

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions”.

Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Regulatory Compliance Statements” in this manual.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

Safety Instructions

WARNING

All operations on this device must be carried out by sufficiently skilled personnel only.

WARNING

Do not connect a switch port to a telephone line.

WARNING

For installation in a Hot-Plug system, observe the safety instructions specific to the system. Read the relevant documentation.

CAUTION

Electric Shock

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.

Special Handling and Unpacking Instructions

ESD Sensitive Device

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing mezzanines, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron AG and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

Two Year Warranty

Kontron AG grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron AG.

Kontron AG warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron Modular Computers GmbH or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

Kontron provides for repair or replacement of any part, assembly or sub-assembly at their own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to Kontron Modular Computers GmbH, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by Kontron with the repaired or replaced item.

Kontron Modular Computers GmbH will not accept liability for any further claims resulting directly or indirectly from any warranty claim, other than the above specified repair, replacement or refunding. In particular, all claims for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time, are excluded. The extent of Kontron Modular Computers GmbH liability to the customer shall not exceed the original purchase price of the item for which the claim exists.

Kontron Modular Computers GmbH issues no warranty or representation, either explicit or implicit, with respect to its products' reliability, fitness, quality, marketability or ability to fulfil any particular application or purpose. As a result, the products are sold "as is," and the responsibility to ensure their suitability for any given task remains that of the purchaser. In no event will Kontron be liable for direct, indirect or consequential damages resulting from the use of our hardware or software products, or documentation, even if Kontron were advised of the possibility of such claims prior to the purchase of the product or during any period since the date of its purchase.

Please remember that no Kontron Modular Computers GmbH employee, dealer or agent is authorized to make any modification or addition to the above specified terms, either verbally or in any other form, written or electronically transmitted, without the company's consent.

Chapter 1

Introduction

1. Introduction

The Board described in this manual is designed for the Advanced Telecom Computing Architecture (AdvancedTCA® or ATCA) defined by the *PCI Industrial Computer Manufacturers Group (PICMG)*. The main advantages of AdvancedTCA include high throughput, multi-protocol support, high-power capability, hot swappability, high scalability and integrated system management. For further information regarding the AdvancedTCA standards and their use, please consult the complete AdvancedTCA specification or visit the *PICMG* web site.

1.1 Product Overview

The Kontron AT8404 is a PICMG 3.0 and 3.1 Option 9 compliant Carrier Board for Advanced TCA shelves, designed according to the RoHS directive. It is a PICMG AMC.0 compliant Conventional Carrier providing four mid-size AMC slots. A Gigabit Ethernet Switch provides connection to the base interface (BI) and fabric interface (FI).

1.1.1 AT8404 Features

The main features of the AT8404 are:

- Gigabit Ethernet Switch
- Fat Pipe Interconnect
- Storage Interconnect
- Unit Computer and Memory
- Synchronous Clock Distribution
- Up to four mid-size AMC bays
- APS (Automatic Protection Switching) for AMCs
- RTM Connector (Zone 3)
- IPMI
- Power Supply Mezzanine incl. Hold Over Circuit

1.1.1.1 Ethernet Switch

- Broadcom BCM56502: 24 Port Gigabit Layer-2/3 Switch with 2 x 10GbE Uplinks
- PCI 32b/66MHz Management IF
- Line rate switching for all packet sizes and conditions
- Supports 2 Base channels 10/100/1000Base-T
- Supports 2 Fabric channels with 10GbE XAUI

- Supports 5 AMC GbE interfaces per AMC slot
- Supports a 10/100/1000Base-T interfaces to the RTM
- Supports a GbE connection to the unit computer for fast packet transfer

1.1.1.2 Fat Pipe Interconnect

- AMC bays B1 and B2 as well as B3 and B4 are directly (copper) interconnected via AMC Fat Pipe ports 4-7

1.1.1.3 Storage Interconnect

- AMC storage ports are connected between pairs of AMC bays
- SAS/SATA HDD on RTM is supported for two AMC bays
- Flexible routing supports different configurations

1.1.1.4 Unit Computer and System Memory

- Socketless PowerPC IBM PPC405GPr-400 MHz
- Used for switch provisioning and diagnostics
- 256 MBytes of SDRAM memory, 133 MHz
- 128 MBytes of Flash memory

1.1.1.5 Synchronous Clock and PCI Express Clock Distribution

- PICMG AMC.0 Revision 2.0 compliant
- Configurable routing of Telecom clock lines between backplane and AMC bays
- PCI Express compliant clock source with optional Spread Spectrum Clock
- Switchable PCI Express clock source to all AMCs

1.1.1.6 IPMI

- PICMG 3.0 / IPMI 1.5 compliant
- Serial EEPROM for FRU storage (serial ID)
- Current, voltage and temperature sensors
- Base Board, AMC bays and RTM hot swap and power control
- Firmware update handling for field upgrades, rollbacks and watchdog functions

1.1.1.7 AMC Bays

- Up to four PICMG AMC.0 Revision 2.0 compatible mid-size AMC bays (see section 1.1.5)
- AMC B+ connectors
- 5 x 1 GbE connections (Common Option and Fat Pipe Regions)
- Full Telecom clocks and PCI Express clock support
- 7 Extended Options Region RTM links
- Update Channel (APS) link per AMC bay running at up to 2.5Gbps

1.1.1.8 RTM Connector

- Support for 7 RTM lanes from each AMC
- FE and RS232 (RJ45) management ports
- 2x Storage connections
- 1x GbE
- 12V and 3V3 sus Supply Voltage connections
- I²C support
- JTAG and production I/O support

1.1.1.9 Power Supply Mezzanine

- Isolated 48V to 12V Standard Quarterbrick intermediate bus converter
- Hot swap support
- Hold Over Circuit using high voltage capacitor and charge pump
- Isolated management power supply
- 48V power Supply 'ORing' circuit
- Supplies point of load regulators for secondary supply voltages (derived from 12V intermediate rail) on base board

1.1.2 General compliances

The AT8404 is conform to the following specifications:

- PICMG 3.0 AdvancedTCA Base Specification, Revision 2.0
- PICMG 3.1 Ethernet/Fibre Channel for AdvancedTCA Systems
- AMC.0 Advance Mezzanine Card Base Specification, Revision 2.0
- AMC.1 PCI Express and Advanced Switching
- AMC.2 AMC Gigabit Ethernet
- AMC.3 AMC Storage
- IPMI v1.5 Intelligent Platform Management Interface Specification

1.1.3 Optional Accessories

1.1.3.1 AMC

Up to four mid-size single width or up to two mid-size double width AMC bays for standard or custom AMCs are implemented.

AMC slots can be equipped with a:

- Processor-AMC
- HDD-AMC as mass storage device for the Processor-AMC
- Interface AMC, e.g. Quad GbE

1.1.3.2 RTM

The Kontron RTM8030 provides an additional GbE switch port and out-of-band management access via Fast Ethernet or RS232. Two storage lines from the AMC bays are routed to a connector on the RTM's face plate for interconnecting two carriers. They may also connect to a SATA HDD located on the RTM. For more information on the RTM8030, refer to chapter 3.2.

1.1.4 Hot Swap Capability

The board supports Full Hot Swap capability as required by PICMG 3.0 R1.0. It can be removed or installed without powering-down the system. Please refer to the PICMG 3.0 R1.0 specification for additional details.

1.1.5 Board Options

The Kontron AT8404 is available with different AMC slot configurations.

Table 1-1: AMC Slot Options

Option	AMC Slot Configuration
A	4 x single width slots
B	2 x double width slots
C	2 x single width slots and 1 x double width slot on B1/B2
D	2 x single width slots and 1 x double width slot on B3/B4

1.2 Technical Specification

Table 1-2: AT8404 Main Specifications

	AT8404	SPECIFICATIONS

Unit Computer and Memory	PowerPC IBM PPC 405 GPr-400MHz	• IBM PowerPC® 405 32-bit RISC processor core operating up to 400MHz with 16KB I- and D-caches
		• PC-133 synchronus DRAM (SDRAM) interface
		  • 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
		• 4KB on-chip memory (OCM)
		• DMA support for external peripherals, internal UART and memory
		  • Scatter-gather chaining supported
		  • Four channels
		• PCI Revision 2.2 compliant interface (32-bit, up to 66MHz)
		• Ethernet 10/100Mbps (full-duplex) support with media independent interface (MII)
		• Two serial ports (16550 compatible UART)
		• Internal processor local Bus (PLB) runs at SDRAM interface frequency
		• IEEE 1149.1 (JTAG) boundary scan

Ethernet	Broadcom 5466R	• Advanced power management Line-side and MAC-side loopback • Ethernet@WireSpeed • Cable plant diagnostics that detects cable plant impairments • Automatic detection and correction of wiring pair swaps, pair skew, and pair polarity • Robust CESD tolerance and low EMI emissions • Support for jumbo packets up to 10 KB in size • IEEE 1149.1 (JTAG) boundary scan

Ethernet	Broadcom 56502	• 24 10/100/1000 Mbps Ethernet ports
		• 2 10GbE ports
		• Fifth generation of StrataSwitch and StrataXGS product line
		• Line-rate switching for all packet sizes and conditions
		• On-chip data packet memory and table memory
		• Advanced Fast Filter Processor (FFP) Content Aware classification
		• Advanced security features in hardware
		• Port-trunking and mirroring supported across stack
		• Advanced packet flow control:
		  • Head-of-line-blocking prevention
		  • Back pressure support
		• QoS queues per port with hierarchical minimum/maximum shaping per class of Service (CoS) per queue per port
		• Standard compliant 802.1ad provider bridging
		• IEEE 1149.1 (JTAG) boundary scan

Table 1-2: AT8404 Main Specifications

	AT8404	SPECIFICATIONS
Interfaces	Backplane (Zone 2)	• Base channels 1 and 2: 1 x GbE (1000BASE-T) • Fabric channels 1 and 2: 1 x 10 GbE (XAUI) • Synchronization Clock: 2 x CLK 1/2/3 (A/B) • Update channels 0-3: APS Path
	RTM (Zone 3)	• 7 generic RTM channels from each AMC Slot • 2 SAS/SATA/FC interfaces for mass storage • 1 GbE interface to front board switch • Serial port for Unit Computer management • Fast Ethernet for Unit Computer management • I2C IPMI connection
	Front Panel	• Serial port for Unit Computer management
General	Mechanical	• 8U form factor mechanically compliant to PICMG 3.0 and AMC.0 • Single slot (6HP) • Up to four mid-size/single width AMC slots • or up to two mid-size/double width AMC slots • 280 mm x 322 mm (11.024“ x 12.677“) • 150 mm cut away in AMC area • Weight: 1.825 kg
	Power Requirements	• Typical: 40W • Maximum (4 AMCs and RTM): 210W • AMCs may consume up to 140W • Operating Voltage: -38 to -72 VDC
	Temperature	Designed to meet or exceed the following (Characteristics without AMCs): • Air Flow: 30 CFM min • Operating: 0°C to +55°C (32°F to 131°F) • Non-operating: -40°C to +70°C (-40°F to 158°F)

Table 1-2: AT8404 Main Specifications

	AT8404	SPECIFICATIONS
General	Humidity	Designed to meet or exceed the following: • Bellcore GR-63, Section 4.1 • Operating: 15%-90% (non-condensing) at 55°C (131°F) • Non-Operating: 5%-95% (non-condensing) at 40°C (104°F)
	Altitude	Designed to meet or exceed the following: • Operating: 4000 m (13123 ft) • Non-operating: 15000 m (49212 ft)
	Vibration	Designed to meet or exceed the following: • Bellcore GR-63, Section 4.4 • ETSI EN 300 019-2-3 • Operating: Sinusoidal 1.0G (5-100Hz), 0.2G (100-200Hz), each axis • Packaged: Random 0.89Grms (5-200Hz), each axis
	Shock	Designed to meet or exceed the following: • DIN/IEC 60068-2-27 • Bellcore GR-63, Section 4.3 • ETSI EN 300 019-2-3 • Operating: 3G, half-sine 11ms, each axis • Packaged: 18G, half-sine 6ms, each axis
	Safety	Designed to meet or exceed the following: • CB report to IEC 60950-1, complies with EN/CSA/ UL 60950-1
	EMC	Designed to meet or exceed the following: • FCC 47 CFR Part 15, Subpart B • EN55022, EN55024 • EN 300 386
	Reliability	• MTBF: > 384,000 hours @ 40°C/104°F (Telcordia SR-332, Issue 1)
HW Monitoring	LEDs	ATCA LEDs: • 4 LEDs ("Ready for Hot Swap", "Out of Service", "Healthy", "Activity")
	Board Management	• based on IPMI 1.5 • FRU Management • Sensors (Voltage, Current, Temperature, Fuse) • Status and Alerting • Hot Swap Management for Base Board and AMC • Electronic Keying of Base and Fabric Interfaces and AMC ports • Local SEL

1.3 Software Support

The following table contains information related to software supported by the AT8404.

Table 1-3: AT8404 Software Specifications

AT8404	SPECIFICATIONS
General	• Reliable field upgrades for all software components • Dual boot images with roll-back capability • Management via SNMP and Command Line Interface • System access via TELNET, SSH and serial line • Hot-Swap support (IPMI) • Hot-Plug support for AMC modules (IPMI)
Ethernet/Bridging	• Static link aggregation (IEEE 802.3ad) on any port combination • Classic and rapid spanning tree algorithms supported (IEEE 802.1D, IEEE 802.1w) • Quality Of Service on all ports (IEEE 802.1p) • Full Duplex operation and flow control on all ports (IEEE 802.3x) • Static MAC filtering • Port Authentication (IEEE 802.1X) • Auto negotiation of speeds and operational mode on all external GE interfaces as well as on all base fabric interfaces • Layer 2 multicast services using GARP/GMRP (IEEE 802.1p) • VLAN support including VLAN tagging (IEEE 802.3ac), dynamic VLAN registration with GARP/GVRP (IEEE 802.1Q) and Protocol based VLANs (IEEE 802.1v) • Double VLAN tagging • Port Mirroring
Applications	• NTP client for retrieving accurate time and date information • DHCP server • Onboard event management • Test and trace facilities • POST (power on self tests) diagnostics • Standards based SNMP implementation supporting SNMP v1, v2 and v3 for monitoring and management purposes • IPMI based management of the onboard AMC slots (AMC.*) • Persistent storage of configuration across restarts • Support for retrieving and installing multiple configurations
QoS	• CoS (Class of Service) • DifffServ (Differentiated Services) • ACL (Access Control List)

Table 1-3: AT8404 Software Specifications

AT8404	SPECIFICATIONS

Supported MIBS	• Switching Package MIBs
	  • RFC 1213 - MIB-II
	  • RFC 1493 - Bridge MIB
	  • RFC 1643 - Ethernet-like -MIB
	  • RFC 2233 - The Interfaces Group MIB using SMI v2
	  • RFC 2618 - RADIUS Authentication Client MIB
	  • RFC 2674 - VLAN & Ethernet Priority MIB
	  • RFC 2819 - RMON Groups 1,2,3 & 9
	  • RFC 3291 - Textual Conventions for Internet Network Addresses
	  • IANA-ifType-MIB
	  • IEEE 802.1X MIB (IEEE8021-PAE-MIB)
	  • IEEE 802.3AD MIB (IEEE8021-AD-MIB)
	• QoS Package MIB
	  • RFC 3289 - DIFFSERV-MIB & DIFFSERV-DCSP-TC MIBs
	• FASTPATH Enterprise MIB
	  • Support for all managed objects not contained in standards based MIBs.

Bootloader	u-boot Version 1.2.0 • POST • loadable bootimage via network (bootp/tftp) • reliable field upgradable • H/W protected • KCS interface to IPMC • serial console support
Operating System	• Wind River Linux PNE 2.0

Chapter 2

Installation

2. Installation

The AT8404 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the AT8404. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

WARNING

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

ESD sensitive equipment

This ATCA board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Do not touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.

2.2 AT8404 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the AT8404 in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the AT8404 in a system proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1. are observed.

WARNING

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the AT8404 refer to Chapter 4.

WARNING

Care must be taken when applying the procedures below to ensure that neither the AT8404 nor other system boards are physically damaged by the application of these procedures.

3. To install the AT8404 perform the following:
   1. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

WARNING

DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   2. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
   3. Fasten the front panel retaining screws.
   4. Connect all external interfacing cables to the board as required.
   5. Ensure that the board and all required interfacing cables are properly secured.

4. The AT8404 is now ready for operation.

2.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1. are observed.

WARNING

Care must be taken when applying the procedures below to ensure that neither the AT8404 nor system boards are physically damaged by the application of these procedures.

2. Unscrew the front panel retaining screws.
3. Lift the notch of the lower handle and pull the handle with the notch away from the faceplate until you feel a resistance. The blue LED starts blinking.
4. Wait until the blue LED is fully ON, this mean that the hot swap sequence is ready for board removal.
5. Disengage the board from the backplane by using both board ejection handles.
6. After disengaging the board from the backplane, pull the board out of the slot.

2.4 AMC Installation

To install an AMC proceed as follows:

1. Remove the AMC filler panel.
2. Carefully engage the AMC into the card guide. Push the AMC until it fully mates with its connector. Secure the AMC handle to the locking position.
3. In normal condition, the blue LED shall turn ON as soon as the AMC is fully inserted. It will turn OFF at the end of the hot swap sequence.

2.5 Software Installation

The AT8404 comes as a pre-installed system with all necessary OS, Filesystem, drivers and applications factory-installed with default configurations.

Updating the Software with new Operating System or applications or new versions is provided by a dedicated update mechanism, which is described in Chapter 4.

2.6 Quick Start

This section gives instructions for (initially) accessing the CLI (Command Line Interface) of the AT8404 using either in-band access via the BI or the out-of-band management interfaces (serial port or Fast Ethernet) accessible from the front plate serial connector or via an appropriate RTM. The CLI is required for configuring the GbE switch, as well as the storage interconnect.

2.6.1 In-Band CLI Access

The GbE switch on the AT8404 is pre-configured with a management VLAN. This VLAN is accessible over the BI. Telnet accesses to port 23 of this VLAN connect to the CLI. The VLAN is configured for DHCP and retrieves its IP address automatically when a DHCP server is found in the network. The procedure to obtain the issued IP from the DHCP server is beyond the scope of this document.

The management VLAN is configured with VLAN ID 1. The following Ethernet ports are members of the management VLAN ID 1 by default:

- Interface 0/23 connected to base interface switch in ATCA logical slot 1
- Interface 0/5, 0/10, 0/15, 0/20 connected to AMC bay B4, B3, B2, B1 on port 0

Thus connectivity to the management VLAN ID 1 is by default possible through the base interface switch in ATCA chassis logical slot 1.

For more information on the management VLAN and how to assign a fixed IP address, refer to the *AT8404 CLI Reference Manual*.

2.6.2 Out-of-band CLI Access

The CLI can also be accessed via serial port (using the front plate connector and provided cable or an appropriate RTM like the RTM8030) or Fast Ethernet (only via RTM). The serial port is ready to use offhand without further configuration.

To connect to the CLI via the Fast Ethernet serviceport on the RTM, a telnet session must be established to the IP address of this interface, port 23.

Using the default configuration, it is necessary to assign an IP address statically to the serviceport. Because the required configuration steps are done in the CLI, an initial access using the serial port or in-band connectivity via the BI is required. The procedure for assigning an IP address to the serviceport is described in the following. User input is printed in bold letters.

1. Connect to serial port on the front plate (using the Kontron DB9 adapter cable) or RTM (using a RJ45 straight cable).

   Port settings are:
   - 115200 bps (serial speed might be different for customized board variants)
   - 8 bit, no parity, 1 stop bit (8N1)
   - no flow control
2. Ensure that the board is powered up.

3. Wait for boot process to complete, i.e. until the console selection menu appears.

```
b - connect Base Fabric console
c - connect Custom Application console
! - shell escape
r - reset system
```

4. Type 'b' to connect to the Base Fabric console.

```
Connected to Base Fabric console
Press ^X or ^V to get to menu again
Base Fabric switching application release GA 2.00 starting

(Unit 1)>

User:
```

5. Log in as admin and enter privileged mode by typing 'enable' (no passwords required by default).

```
User:admin
Password:
(Ethernet Fabric) >enable
Password:

(Ethernet Fabric) #
```

6. Set IP address and netmask. (see below for an example IP address setting)

```
(Ethernet Fabric) #serviceport ip 192.168.50.107 255.255.255.0
```

The FE management interface is available from now on.

7. Save configuration by copying it to the flash, confirm by typing 'y'

```
(Ethernet Fabric) #copy system:running-config nvram:startup-config

This operation may take a few minutes.
Management interfaces will not be available during this time.

Are you sure you want to save? (y/n) y

Configuration Saved!

(Ethernet Fabric) #
```

To access the CLI via Fast Ethernet management port, open a telnet connection to the configured IP address, port 23.

For additional information on the system configuration, refer to the *AT8404 CLI Reference Manual*.

2.6.3 Storage Configuration

The storage connection on Port 2 of AMC B4 is linked to AMC B2 (port 2) by default. To establish a storage connection between AMC bays 1 (port 3) and 4 (port 2), use the following command in privileged mode:

```
(Ethernet Fabric) #set board storage connect amcb4 amcb1
```

To reset the configuration to the default settings, use the following command:

```
(Ethernet Fabric) #set board storage connect amcb4 amcb2
```

For an overview of the current configuration, use the CLI boardinfo command:

```
(Ethernet Fabric) #show boardinfo storage
The AMC B4 (port 2) is connected to AMC B2 (port 2)
```

Chapter 3

Hardware Description

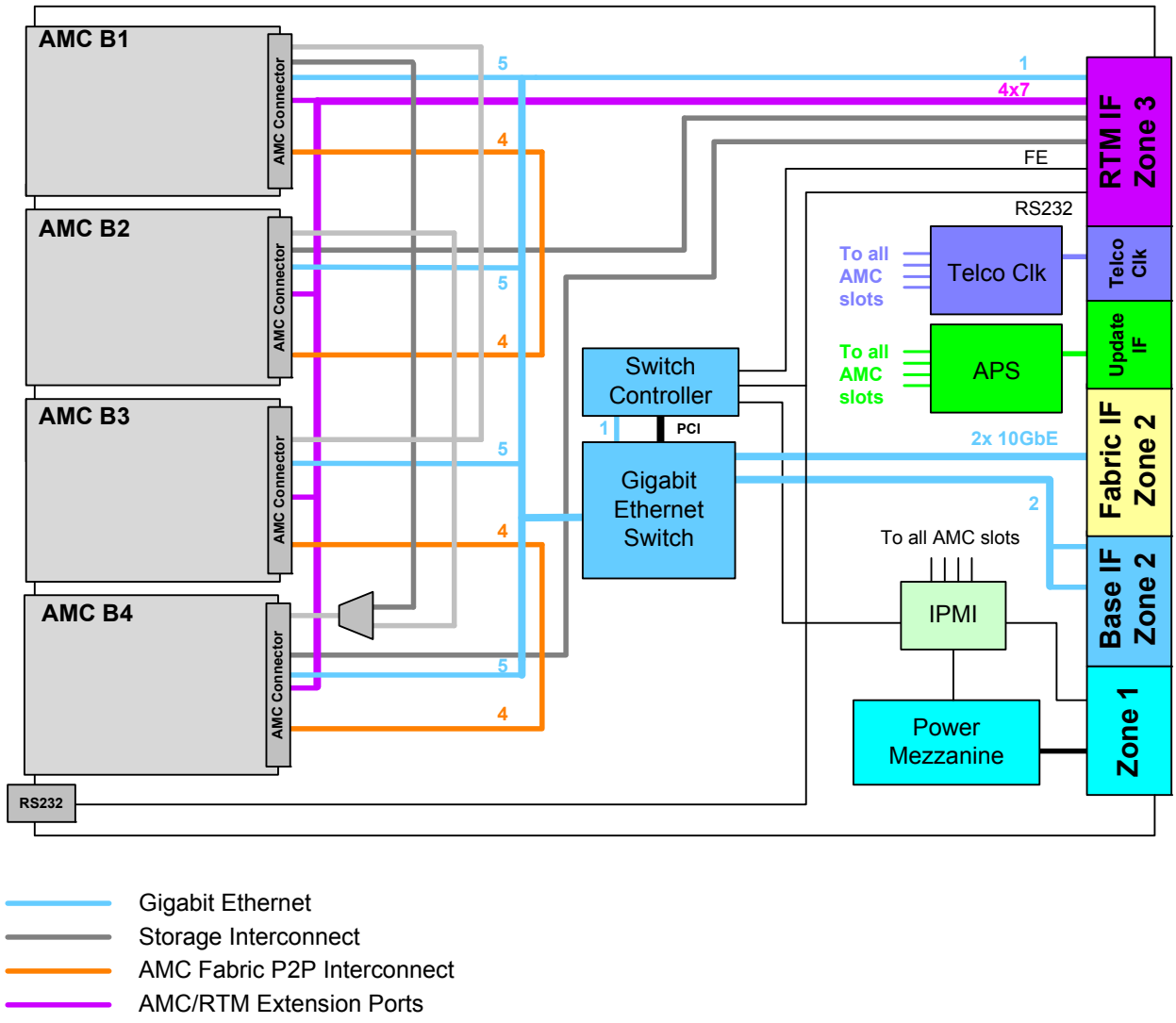
3. Hardware Description

This chapter describes the board specific items of the AdvancedTCA AMC Carrier Board AT8404 consisting of the main assembly with the Power Mezzanine Module. Also described is the RTM8030 used for management access and I/O extension.

3.1 Base Board

The base board is a PICMG 3.0 and 3.1 Option 9 compliant Carrier Board for AdvancedTCA shelves offering up to four mid-size AMC bays.

Figure 3-1: Functional Block Diagram Base Board



The main building blocks of the base board are:

- Ethernet Switch
- Unit Computer and Memory
- Fat Pipe Interconnect
- Storage Interconnect
- Synchronous Clock Distribution
- AMC Bays with APS (Automatic Protection Switching)
- IPMI
- RTM Interface
- Power Supply

3.1.1 Ethernet Switch

The main parts of the Ethernet Switch building block is a Broadcom BCM56502 24 port Gigabit Layer-2/3 Switch and a Broadcom BCM5466R QUAD 10/100/1000BASE-T PHY for the base and extension fabric interface, AMC and RTM Uplink connectivity. The BCM56502 is managed via the 32bit/33MHz PCI interface.

A BCM 5466R performs PHY functions for the 10/100/1000BASE-T ports of the Unit Computer and the two base interface links.

The ports of the BCM56502 are assigned as follows:

Table 3-1: GbE Switch Port Assignment

CLI ID	Speed	Type	Connection
0/1	1 GbE	Serdes	AMC B1, Port 8
0/2	1 GbE	Serdes	AMC B1, Port 9
0/3	1 GbE	Serdes	AMC B1, Port 10
0/4	1 GbE	Serdes	AMC B1, Port 11
0/5	1 GbE	Serdes	AMC B1, Port 0
0/6	1 GbE	Serdes	AMC B2, Port 8
0/7	1 GbE	Serdes	AMC B2, Port 9
0/8	1 GbE	Serdes	AMC B2, Port 10
0/9	1 GbE	Serdes	AMC B2, Port 11
0/10	1 GbE	Serdes	AMC B2, Port 0
0/11	1 GbE	Serdes	AMC B3, Port 8
0/12	1 GbE	Serdes	AMC B3, Port 9
0/13	1 GbE	Serdes	AMC B3, Port 10
0/14	1 GbE	Serdes	AMC B3, Port 11
0/15	1 GbE	Serdes	AMC B3, Port 0
0/16	1 GbE	Serdes	AMC B4, Port 8
0/17	1 GbE	Serdes	AMC B4, Port 9
0/18	1 GbE	Serdes	AMC B4, Port 10
0/19	1 GbE	Serdes	AMC B4, Port 11
0/20	1 GbE	Serdes	AMC B4, Port 0

Table 3-1: GbE Switch Port Assignment (Continued)

CLI ID	Speed	Type	Connection
0/21	1 GbE	100BaseTX	Unit Computer
0/22	1 GbE	Serdes	RTM SFP
0/23	1 GbE	1000BaseT	Base Channel 1
0/24	1 GbE	1000BaseT	Base Channel 2
0/25	10 GbE	XAUI	Fabric Channel 1
0/26	10 GbE	XAUI	Fabric Channel 2

3.1.2 Unit Computer and Memory

A PowerPC PPC405GPr-400MHz 32 bit RISC processor with 16KB D-cache, 256MB SDRAM and 128MB Flash memory manages the Ethernet switch via 32bit / 66MHZ PCI local bus. The CPU is accessible via serial port or 10/100BASE-T Ethernet from the RTM or in-band via the GbE switch.

Besides the direct PCI connection to the management interface of the switch, a PCI Ethernet controller links the Unit Computer to a switch port which is configured as 10/100BaseTX.

3.1.2.1 Fast Ethernet Management Interface

The 10/100BaseTX Ethernet management interface connects the Unit Computer to the RTM. It uses the following pins of the ATCA Zone 3 connector:

Table 3-2: Fast Ethernet Pins on RTM Connector

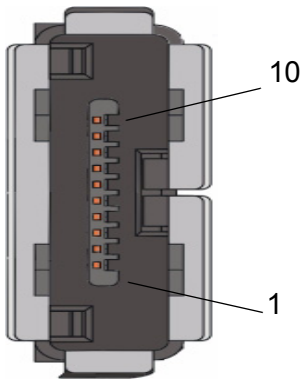
J30 Pin	Function
B8	MNG_LAN_DA-
A8	MNG_LAN_DA+
D8	MNG_LAN_DB-
C8	MNG_LAN_DB+

3.1.2.2 RS232 Management Interface

One RS232 interface of the Unit Computer is the serial port which is routed to a miniature connector on the front plate. An adapter cable is available from Kontron to establish a connection with a terminal with a standard DB9 serial port. Additionally, the Unit Computer's serial port is routed to the Zone 3 connector so that a connection can also be established by using an appropriate RTM like the RTM8030. If both ports are connected to a terminal, the front plate connection takes precedence over the RTM connection.

The front plate connector has the following pinning:

Table 3-3: Serial Port (J11) Pin Assignment

Pin Number	Signal	
1	N.C.	
2	RXD	
3	TXD	
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	CTS	
9	N.C.	
10	N.C.	

The RS232 Management Interface uses the following pins of the ATCA Zone 3 connector:

Table 3-4: RS232 Pins on RTM Connector

J30 Pin	Function
B3	RXD
A3	TXD

3.1.2.3 SDRAM

Five 512 Mbit devices, soldered directly onto the PCB, provide 256 MByte of SDRAM plus 64 MByte for ECC. The SDRAM interface of the Unit Computer is 32 bit wide and operated at 133 MHz.

3.1.2.4 Flash ROM

The CPU uses a 128 Mbyte Flash Memory device. The sector containing the boot initialization code is write protected.

3.1.3 Fat Pipe Interconnect

AMC bays B1 and B2 as well as B3 and B4 are directly (copper) interconnected via AMC Fat Pipe ports 4-7, see following table.

Table 3-5: Fat Pipe Interconnect

AMC Port	Connects to
B1 port 4	B2 port 4
B1 port 5	B2 port 5
B1 port 6	B2 port 6
B1 port 7	B2 port 7
B2 port 4	B1 port 4
B2 port 5	B1 port 5
B2 port 6	B1 port 6
B2 port 7	B1 port 7
B3 port 4	B4 port 4
B3 port 5	B4 port 5
B3 port 6	B4 port 6
B3 port 7	B4 port 7
B4 port 4	B3 port 4
B4 port 5	B3 port 5
B4 port 6	B3 port 6
B4 port 7	B3 port 7

3.1.4 Storage Interconnect

A port selector is used to configure either a storage connection between the AMC B2 and B4 or B1 and B4. The port selector is controlled by the IPMC.

Depending on the configuration, the SAS/SATA ports of the four mid-size AMC bays are interconnected as follows:

Table 3-6: AMC Storage Interconnect

AMC Port	Connects to
B1 port 2	B3 port 2
B1 port 3	B4 port 2 via port selector
B2 port 2	B4 port 2 via port selector
B2 port 3	RTM port SAS_0
B3 port 2	B1 port 2
B3 port 3	-
B4 port 2	B1 port 3 or B2 port 2 via port selector
B4 port 3	RTM port SAS_1

For more information on how to configure the AMC Storage connections, refer to the *AT8404 CLI Reference Manual*.

3.1.5 Synchronous Clock Distribution

An FPGA is the global clock distribution device on the carrier board. In conjunction with the Telecom Clock protection switch, the FPGA distributes all necessary Telecom Clocks to or from the AMCs and the backplane.

TCLKA and TCLKC of any AMC can be driven by any backplane clock (CLK1A/B, CLK2A/B or CLK3A/B). TCLKB and TCLKD of any AMC can drive any backplane clock. Any ATCA backplane clock can be used as the reference clock input.

For more information on how to configure the clock distribution, refer to the *AT8404 CLI Reference Manual*.

3.1.6 AMC Bays

Up to four mid-size and single width or up to two mid-size and double width AMC bays for standard or custom AMCs are implemented with B+ AMC connectors, depending on the board option.

Table 3-7: AMC Slot Types

Board option	B1	B2	B3	B4
A	Single width	Single width	Single width	Single width
B	-	Double width	-	Double width
C	-	Double width	Single width	Single width
D	Single width	Single width	-	Double width

Because of the AMC slot storage interconnects (see section 3.1.2. Storage Interconnect) and for thermal reasons, the preferred Processor AMC slots are B1 and B2 and the preferred HDD-AMC slots are B3 and B4.

Table 3-8: AMC B1 Port Assignment

Port	Region	Connection
0	GbE	GbE Switch 0/5
1	GbE	-
2	Storage	AMC B3 Port 2
3	Storage	AMC B4 Port 2 / -*
4	Fabric	AMC B2 Port 4
5	Fabric	AMC B2 Port 5
6	Fabric	AMC B2 Port 6
7	Fabric	AMC B2 Port 7
8	Fabric	GbE Switch 0/1
9	Fabric	GbE Switch 0/2
10	Fabric	GbE Switch 0/3
11	Fabric	GbE Switch 0/4
12	Extended	Update, APS Channel
13	Extended	RTM, AMC_B1_P13
14	Extended	RTM, AMC_B1_P14
15	Extended	RTM, AMC_B1_P15
17	Extended	RTM, AMC_B1_P17
18	Extended	RTM, AMC_B1_P18
19	Extended	RTM, AMC_B1_P19

Table 3-8: AMC B1 Port Assignment (Continued)

Port	Region	Connection
20	Extended	RTM, AMC_B1_P20
TCLKA	Clock	From Backplane
TCLKB	Clock	To Backplane
TCLKC	Clock	From Backplane
TCLKD	Clock	To Backplane
FCLKA	Clock	Fabric Reference Clock

* Depends on configuration

Table 3-9: AMC B2 Port Assignment

Port	Region	Connection
0	GbE	GbE Switch 0/10
1	GbE	-
2	Storage	AMC B4 Port 2 / -*
3	Storage	RTM SAS_0
4	Fabric	AMC B1 Port 4
5	Fabric	AMC B1 Port 5
6	Fabric	AMC B1 Port 6
7	Fabric	AMC B1 Port 7
8	Fabric	GbE Switch 0/6
9	Fabric	GbE Switch 0/7
10	Fabric	GbE Switch 0/8
11	Fabric	GbE Switch 0/9
12	Extended	Update, APS Channel
13	Extended	RTM, AMC_B2_P13
14	Extended	RTM, AMC_B2_P14
15	Extended	RTM, AMC_B2_P15
17	Extended	RTM, AMC_B2_P17
18	Extended	RTM, AMC_B2_P18
19	Extended	RTM, AMC_B2_P19
20	Extended	RTM, AMC_B2_P20
TCLKA	Clock	From Backplane
TCLKB	Clock	To Backplane
TCLKC	Clock	From Backplane
TCLKD	Clock	To Backplane
FCLKA	Clock	Fabric Reference Clock

* Depends on configuration

Table 3-10: AMC B3 Port Assignment

Port	Region	Connection
0	GbE	GbE Switch 0/15
1	GbE	-
2	Storage	AMC B1 Port 2
3	Storage	-
4	Fabric	AMC B4 Port 4
5	Fabric	AMC B4 Port 5
6	Fabric	AMC B4 Port 6
7	Fabric	AMC B4 Port 7
8	Fabric	GbE Switch 0/11
9	Fabric	GbE Switch 0/12
10	Fabric	GbE Switch 0/13
11	Fabric	GbE Switch 0/14
12	Extended	Update, APS Channel
13	Extended	RTM, AMC_B3_P13
14	Extended	RTM, AMC_B3_P14
15	Extended	RTM, AMC_B3_P15
17	Extended	RTM, AMC_B3_P17
18	Extended	RTM, AMC_B3_P18
19	Extended	RTM, AMC_B3_P19
20	Extended	RTM, AMC_B3_P20
TCLKA	Clock	From Backplane
TCLKB	Clock	To Backplane
TCLKC	Clock	From Backplane
TCLKD	Clock	To Backplane
FCLKA	Clock	Fabric Reference Clock

Table 3-11: AMC B4 Port Assignment

Port	Region	Connection
0	GbE	GbE Switch 0/20
1	GbE	-
2	Storage	AMC B1 Port 3 / AMC B2 Port 2*
3	Storage	RTM SAS_1
4	Fabric	AMC B3 Port 4
5	Fabric	AMC B3 Port 5
6	Fabric	AMC B3 Port 6
7	Fabric	AMC B3 Port 7
8	Fabric	GbE Switch 0/16
9	Fabric	GbE Switch 0/17
10	Fabric	GbE Switch 0/18
11	Fabric	GbE Switch 0/19
12	Extended	Update, APS Channel
13	Extended	RTM, AMC_B4_P13
14	Extended	RTM, AMC_B4_P14
15	Extended	RTM, AMC_B4_P15
17	Extended	RTM, AMC_B4_P17
18	Extended	RTM, AMC_B4_P18
19	Extended	RTM, AMC_B4_P19
20	Extended	RTM, AMC_B4_P20
TCLKA	Clock	From Backplane
TCLKB	Clock	To Backplane
TCLKC	Clock	From Backplane
TCLKD	Clock	To Backplane
FCLKA	Clock	Fabric Reference Clock

* Depends on configuration

Gigabit Ethernet

Port 0 and ports 8 to 11 of each AMC are connected to the Ethernet switch. The Ethernet switch supports 1000BASE-BX Gigabit Ethernet.

Storage

Ports 2 and 3 of the AMC slots are reserved for storage connections to other AMC bays or the RTM (see section 3.1.2. Storage Interconnect).

PCI Express

Bays B1 and B3 and bays B2 and B4 implement a x4 direct connection on ports 4 to 7.

Automatic Protection Switching

Port 12 on each AMC bay is used as a 2.5 Gbps direct interconnect to the neighbouring Carrier Board via the update channel for line card applications.

Interconnects to RTM

Each AMC Bay has seven generic interconnects to the RTM Zone 3 (ports 13 to 20).

3.1.7 IPMI

The AT8404 supports an intelligent hardware management system based on the Intelligent Platform Management Interface (IPMI) Specification 1.5. It provides the ability to manage the power, cooling and interconnect needs of intelligent devices, to monitor events and to log events to a central repository.

The main building blocks of the IPMI architecture of the AT8404 are:

- IPMC Intelligent Platform Management Controller
- FPGA (Field Programmable Gate Array)

3.1.7.1 IPMC

The IPMC controls all hotswap and E-Keying processes required by ATCA. It activates the board power supply and enables communication with the AMC card and the RTM. The IPMC manages the Ethernet switch E-Keying and the baseboard ATCA feature. The controller is connected to the ATCA shelf manager via IPMB bus on the backplane.

All voltages and currents on the base board are monitored by the IPMC, including the management and AMC supply. Six temperature sensors on the board make sure that thermal conditions are met. Following is a list of the temperature sensors and their positions. For information on how to obtain sensor values and thresholds, refer to the *AT8404 CLI Reference Manual*.

Table 3-12: Temperature Sensors

Temperature Sensor	Position
Temp PPC Inlet	Lower board edge, rear third, near Unit Computer
Temp PPC Outlet	Near Unit Computer
Temp AMC Inlet	Lower board edge, middle of AMC area
Temp AMC Outlet	Upper board edge, middle of AMC area
Temp PCB Outlet	Upper board edge, rear third
Temp BCM Outlet	Near GbE switch

The internal Flash memory of the IPMC is divided into two distinct parts, the IPMI firmware and the boot block. This allows maintaining a permanent boot block and only erasing the IPMI firmware for upgrade procedure. This is the key feature to achieve a fail-safe upgrade procedure.

The IPMC executes normally the IPMI firmware located in its internal Flash memory. During an update, the IPMC transfers the new IPMI firmware to one of the two external menory banks. Then, it programs its internal Flash memory with the new contents of the external memory and restarts. The restart does not affect board operation in any way. In case of a failure, the IPMC memory is restored from the second external bank. A two-stage (internal and external) watchdog mechanism enables a reliable fault detection.

3.1.7.2 FPGA

The Field Programmable Gate Array (FPGA) is the central device for all glue logic resources. It is configured after the management voltages are stable by an external serial Flash device. The FPGA implements the Synchronous Clock Distribution (see section 3.1.5) and is part of the board management. It connects the Unit Computer to the IPMC and handles the serial interfaces of Unit Computer, IPMC, RTM and the RS232 connector on the front panel. The FPGA controls the LEDs for the whole board, handles the signals to control and to monitor the AMCs, the RTM and all payload devices connected to the FPGA and it is responsible for the power and reset sequencing.

The FPGA provides a MultiBoot feature that allows to load one of two FPGA images, either the factory image or the user image. In combination with a watchdog and fallback mechanism, this allows fail-safe in-field upgrades of the FPGA code.

3.1.8 RTM Interface

Management and I/O interfaces from the base board are routed to Zone 3 where a connector mates with the RTM. This allows base boards to be quickly and reliably serviced without the issues associated with disconnecting and reconnecting multiple cable assemblies. The RTM connection is compliant to the PICMG 3.0 standard.

For the connection between the AT8404 and the RTM, three connectors with 40 differential pairs are used (J30, J31 and J32).

Each AMC Bay has seven generic interconnects to the RTM Zone 3. Two SAS/SATA interfaces for mass storage are implemented. There is a JTAG connection for FPGA update or Boundary Scan-Test. An I²C IPMI interface is implemented for board management. The Unit Computer's management interfaces (Fast Ethernet and RS232) are also connected to the RTM. A GbE port allows connection to the GbE switch.

The Zone 3 connectors have the following pin assignments.

Table 3-13: J30 Assignment

J30	ROW A	AB	ROW B	ROW C	CD	ROW D
1	12V	GND	12V	12V	GND	3V3_SUS
2	12V	GND	12V	12V	GND	JTAG_AMC_EN#
3	SPA_RX#	GND	SPA_TX#	JTAG_TDI	GND	JTAG_TDO
4	N.C.	GND	N.C.	N.C.	GND	N.C.
5	RS232_TX1	GND	N.C.	RS232_TX2	GND	N.C.
6	AMC_B2_P15_TX+	GND	AMC_B2_P15_TX-	AMC_B3_P15_TX+	GND	AMC_B3_P15_TX-
7	AMC_B2_P15_RX+	GND	AMC_B2_P15_RX-	AMC_B3_P15_RX+	GND	AMC_B3_P15_RX-
8	MNG_LAN_TXD+	GND	MNG_LAN_TXD-	MNG_LAN_RXD+	GND	MNG_LAN_RXD-
9	SAS_1_TX+	GND	SAS_1_TX-	SAS_1_RX+	GND	SAS_1_RX-
10	N.C.	GND	N.C.	N.C.	GND	N.C.
J30	**ROW E**	**EF**	**ROW F**	**ROW G**	**GH**	**ROW H**
1	N.C.	GND	RTM_PRNT#	N.C.	GND	RTM_EN#
2	IPMB_SCL	GND	IPMB_SDA	N.C.	GND	N.C.
3	JTAG_TMS	GND	JTAG_TCK	JTAG_TRST	GND	TEST_ON#
4	RTML_TX	GND	RTML_RX	RTML_CLK	GND	RST_PROG
5	AMC_B4_P15_RX+	GND	AMC_B4_P15_RX-	AMC_B1_P15_TX+	GND	AMC_B1_P15_TX-
6	AMC_B4_P15_TX+	GND	AMC_B4_P15_TX-	SFP_SCL	GND	SFP_SDA
7	PPC_RST#	GND	N.C.	AMC_B1_P15_RX+	GND	AMC_B1_P15_RX-
8	MNG_LAN_CT	GND	JTAG_EN#	FLASH_WE	GND	FLASH_WP
9	SAS_0_TX+	GND	SAS_0_TX-	SAS_0_RX+	GND	SAS_0_RX-
10	GE22_TX+	GND	GE22_TX-	GE22_RX+	GND	GE22_RX-

Table 3-14: J31 Assignment

J31	ROW A	AB	ROW B	ROW C	CD	ROW D
1	N.C.	GND	N.C.	N.C.	GND	N.C.
2	N.C.	GND	N.C.	N.C.	GND	N.C.
3	N.C.	GND	N.C.	N.C.	GND	N.C.
4	N.C.	GND	N.C.	N.C.	GND	N.C.
5	N.C.	GND	N.C.	N.C.	GND	N.C.
6	AMC_B1_P13_TX+	GND	AMC_B1_P13_TX-	AMC_B1_P13_RX+	GND	AMC_B1_P13_RX-
7	N.C.	GND	N.C.	N.C.	GND	N.C.
8	AMC_B1_P19_TX+	GND	AMC_B1_P19_TX-	AMC_B1_P19_RX+	GND	AMC_B1_P19_RX-
9	AMC_B2_P17_TX+	GND	AMC_B2_P17_TX-	AMC_B2_P17_RX+	GND	AMC_B2_P17_RX-
10	AMC_B2_P19_TX+	GND	AMC_B2_P19_TX-	AMC_B2_P19_RX+	GND	AMC_B2_P19_RX-
J31	**ROW E**	**EF**	**ROW F**	**ROW G**	**GH**	**ROW H**
1	N.C.	GND	N.C.	N.C.	GND	N.C.
2	N.C.	GND	N.C.	N.C.	GND	N.C.
3	N.C.	GND	N.C.	N.C.	GND	N.C.
4	N.C.	GND	N.C.	N.C.	GND	N.C.
5	AMC_B1_P14_TX+	GND	AMC_B1_P14_TX-	AMC_B1_P14_RX+	GND	AMC_B1_P14_RX-
6	AMC_B1_P17_TX+	GND	AMC_B1_P17_TX-	AMC_B1_P17_RX+	GND	AMC_B1_P17_RX-
7	AMC_B1_P18_TX+	GND	AMC_B1_P18_TX-	AMC_B1_P18_RX+	GND	AMC_B1_P18_RX-
8	AMC_B1_P20_TX+	GND	AMC_B1_P20_TX-	AMC_B1_P20_RX+	GND	AMC_B1_P20_RX-
9	AMC_B2_P18_TX+	GND	AMC_B2_P18_TX-	AMC_B2_P18_RX+	GND	AMC_B2_P18_RX-
10	AMC_B2_P20_TX+	GND	AMC_B2_P20_TX-	AMC_B2_P20_RX+	GND	AMC_B2_P20_RX-

Table 3-15: J32 Assignment

J32	ROW A	AB	ROW B	ROW C	CD	ROW D
1	N.C.	GND	N.C.	N.C.	GND	N.C.
2	AMC_B2_P14_TX+	GND	AMC_B2_P14_TX-	AMC_B2_P14_RX+	GND	AMC_B2_P14_RX-
3	N.C.	GND	N.C.	N.C.	GND	N.C.
4	AMC_B3_P14_TX+	GND	AMC_B3_P14_TX-	AMC_B3_P14_RX+	GND	AMC_B3_P14_RX-
5	AMC_B3_P17_TX+	GND	AMC_B3_P17_TX-	AMC_B3_P17_RX+	GND	AMC_B3_P17_RX-
6	AMC_B3_P19_TX+	GND	AMC_B3_P19_TX-	AMC_B3_P19_RX+	GND	AMC_B3_P19_RX-
7	N.C.	GND	N.C.	N.C.	GND	N.C.
8	AMC_B4_P14_TX+	GND	AMC_B4_P14_TX-	AMC_B4_P14_RX+	GND	AMC_B4_P14_RX-
9	AMC_B4_P17_TX+	GND	AMC_B4_P17_TX-	AMC_B4_P17_RX+	GND	AMC_B4_P17_RX-
10	AMC_B4_P19_TX+	GND	AMC_B4_P19_TX-	AMC_B4_P19_RX+	GND	AMC_B4_P19_RX-
J32	**ROW E**	**EF**	**ROW F**	**ROW G**	**GH**	**ROW H**
1	AMC_B2_P13_TX+	GND	AMC_B2_P13_TX-	AMC_B2_P13_RX+	GND	AMC_B2_P13_RX-
2	N.C.	GND	N.C.	N.C.	GND	N.C.
3	AMC_B3_P13_TX+	GND	AMC_B3_P13_TX-	AMC_B3_P13_RX+	GND	AMC_B3_P13_RX-
4	N.C.	GND	N.C.	N.C.	GND	N.C.
5	AMC_B3_P18_TX+	GND	AMC_B3_P18_TX-	AMC_B3_P18_RX+	GND	AMC_B3_P18_RX-
6	AMC_B3_P20_TX+	GND	AMC_B3_P20_TX-	AMC_B3_P20_RX+	GND	AMC_B3_P20_RX-
7	AMC_B4_P13_TX+	GND	AMC_B4_P13_TX-	AMC_B4_P13_RX+	GND	AMC_B4_P13_RX-
8	N.C.	GND	N.C.	N.C.	GND	N.C.
9	AMC_B4_P18_TX+	GND	AMC_B4_P18_TX-	AMC_B4_P18_RX+	GND	AMC_B4_P18_RX-
10	AMC_B4_P20_TX+	GND	AMC_B4_P20_TX-	AMC_B4_P20_RX+	GND	AMC_B4_P20_RX-

Signals with TX in their name are driven by the front board, those with RX are driven by the RTM.

3.1.9 Power Supply

The power supply fulfils the PICMG3.0 requirements and has the following characteristics:

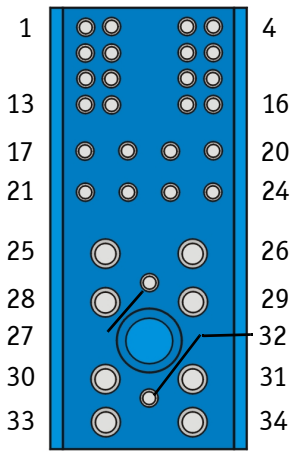
- Full operation at -38VDC to -72VDC
- No damage inflicted to board at 0VDC to -75VDC
- Typical payload power consumption (no RTM, no AMCs): 40W
- Management power consumption (suspend power): <10W
- Additional AMC payload power consumption: 140W

3.1.9.1 Power Connector

The power connector supplies the board with two 48V redundant rails, digital ground and chassis ground. It also provides the redundant IPMB Shelf Manager connection.

Table 3-16: Power Connector (P10)

Signal	Pin		Pin	Signal
N.C.	1		2	N.C.
N.C.	3		4	N.C.
HA0	5		6	HA1
HA2	7		8	HA3
HA4	9		10	HA4
HA6	11		12	HA5
SCL_A	13		14	SDA_A
SCL_B	15		16	SDA_B
MT1_TIP(N.C.)	17		18	MT2_TIP(N.C.)
RING_A(N.C.)	19		20	RING_B(N.C.)
MT1_RING(N.C.)	21		22	MT2_RING(N.C.)
RRTN_A(N.C.)	23		24	RRTN_B(N.C.)
SHELF_GND	25		26	LOGIC_GND
ENABLE_B	27		28	VRTN_A
VRTN_B	29		30	EARLY_A
EARLY_B	31		32	ENABLE_A
-48V_A	33		34	-48V_B



3.1.9.2 Power Supply Mezzanine

The Filter, the Hot-Swap-Controller, the Hold Over circuit and the Quarter-Brick are situated on the Power Supply Mezzanine Module. It shall only be removed or exchanged by authorized personnel.

3.1.9.3 Power Distribution

The Telecom DC voltage (-48V) is supplied by the backplane via two independent rails, primary (A) and secondary (B). The rails are mixed using power Schottky rectifiers. A 7A fuse protects each -48V line and a 10A fuse protects each RTN line. A hot swap controller enables the 48V power to the board.

On the mezzanine module, a quarter brick DC/DC converter transforms the 48 Volts to secondary 12 Volts for payload supply and 3.3 Volts for management supply.

Several point of load converters generate the various required voltages.

The management (or suspend) power is present once the board is connected to the backplane. It supplies the IPMI part which in turn controls the payload power. The various payload voltages are switched on and off in a sequenced manner.

3.1.9.4 Power Supply AMCs

Each AMC has its own power supply. The 12V payload power is generated by a hot swap controller and for the 3V3 management power a current limit switch is used. The maximum power dissipation for an AMC is 60W.

For further details please refer the AMC Specification.

3.1.9.5 Power Supply RTM

The RTM has its own power supply. The 12V payload power is generated by a hot swap controller and for the management power a current limit switch is used. The maximum power dissipation for an RTM is 10W.

For further details please refer the PICMG 3.0 standard.

3.1.9.6 Power Transients

The board provides continuous operation in the presence of transients shown in the following table of the PICMG 3.0 standard:

Table 3-17: Power Transients

Voltage	Duration	Comments	Protected by
- 200 Volts	5 µs	- 100 to - 200 Volts	Frame or Shelf
- 100 Volts	10 µs	- 75 to - 100 Volts	Board
- 75 Volts	10 ms	10 Volts per ms-Rise or Fall	Board
- 0 Volts	5 ms	50 Volts per ms-Fall 12.5 Volts per ms-Rise Assumes prior voltage is above -44 VDC for Shelves, -43 VDC for Boards	Board

In case of a 0V transient the board is able to keep the board alive for 5ms. The necessary energy is buffered in a capacitor.

3.1.9.7 Optional Chassis to Logic Ground Connection

According to NEBS requirement R9-14 of GR-1089-CORE issue 3, the AT8404 provides a connection between chassis and logic ground. It is made up of a screw that connects the PCB to the bottom sheet.

If chassis and logic ground shall be isolated, the screw with its washer can be removed. It is located near the jumper header J7 and is labelled "GND TO CHASSIS".

3.1.10 Jumpers

Eight jumpers in the upper right corner allow debug settings (J7). The IPMI and AMC E-Keying override jumpers enable bypassing communication with the ShMC for bench operation. The JTAG jumpers configure the boundary scan path. JTAG operation requires the use of the RTM8030.

WARNING

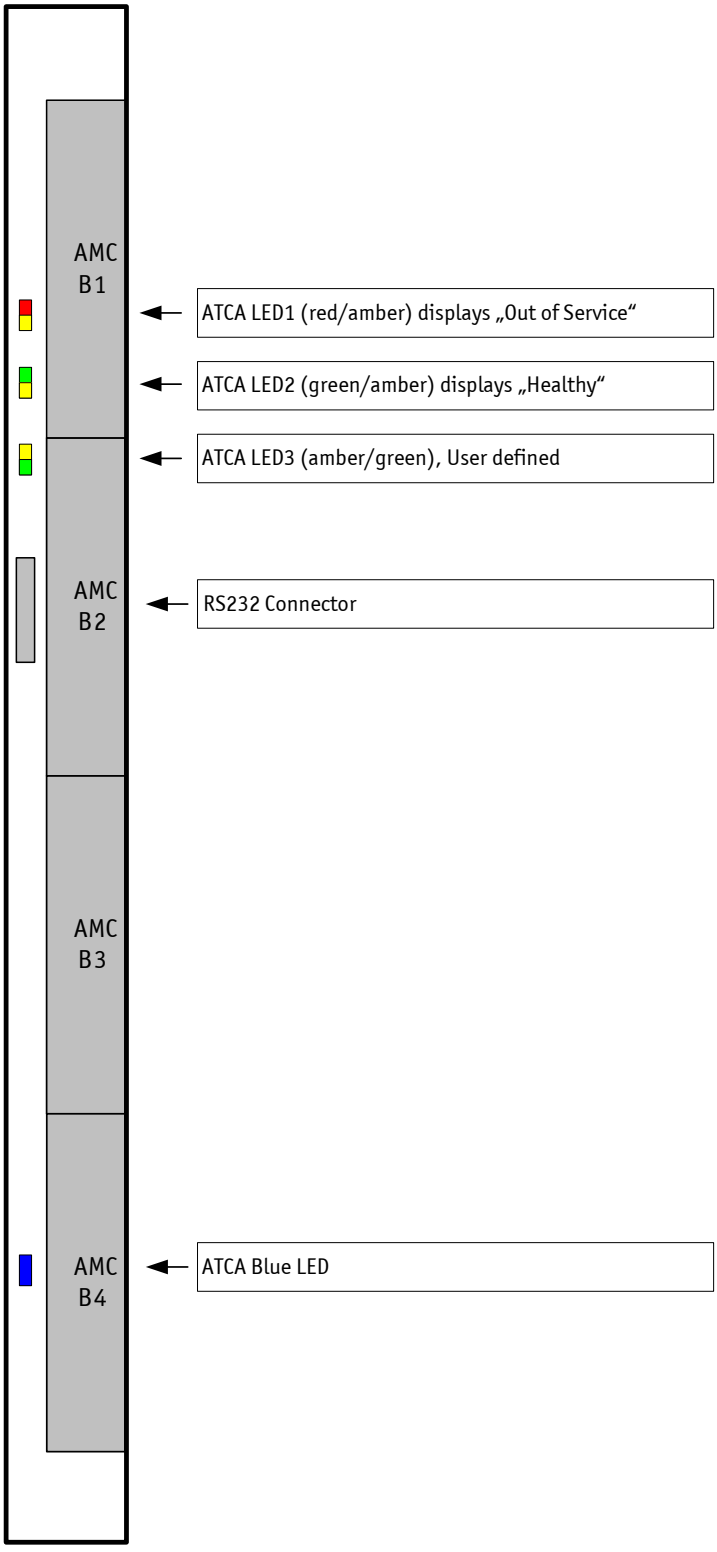
Operation with any of these jumpers set is not supported by the standard application software.

Table 3-18: Jumper Settings (• Default Setting)

F_SPI_PROG	
FPGA Configuration Programming	in
• Normal Operation	out
RES_OVR	
Reserved	in
• Reserved	out
AMC_OVR	
IPMC AMC override	in
• Normal Operation	out
SHMC_OVR	
IPMC Shelf Manager override	in
• Normal Operation	out
JTAG_AMC_EN	
Enable JTAG on AMCs only	in
• Full JTAG Chain	out
JTAG_BDI_EN	
PPC Debug interface enable	in
• Normal Operation	out
TEST_ON	
IPMI Board activation override	in
• Normal IPMI activation	out
POWER_ON	
Voltage enable override	in
• Normal power sequencing	out

3.1.11 Front Panel Elements

Figure 3-2: Front Panel of AT8404



The four front panel ATCA LEDs display the status of the board’s health.

Table 3-19: Symbols Chart

LED	Signification	LED
	Activity	ATCA LED3 (amber/green)
	Healthy	ATCA LED2 (green/amber)
	Out of Service	ATCA LED1 (red/amber)
	Hot Swap	ATCA BLUE LED

Table 3-20: ATCA LEDs Signification

LED	Signification
ATCA LED3 (HB) (amber/green)	not used, can be controlled by application using PICMG API
ATCA LED2 (HY) (green/amber)	Off=Payload power down ON(green)=Health OK ON(amber)=Health error (Critical) Application defined=Can be controlled by application using PICMG API
ATCA LED1 (OOS) (red/amber)	On=Out of Service Blink=Firmware Update in Progress or Power denied
ATCA BLUE LED (H/S)	On=Ready for Hot Swap Blink=Hot Swap in Progress

3.2 RTM8030

The RTM8030 is a single slot (6HP) ATCA Rear Transition Module. This RTM provides additional connectivity to the Kontron AT8030 CPU board and the AT8404 10G AMC Carrier board. This chapter describes the RTM features which are usable for the AT8404. For a general and AT8030 specific description, please refer to the RTM8030 User's Guide.

Note...

Not all of the front plate elements are used in combination with the AT8404. E.g., the USB port and rotary switch are only used for operation with the AT8030.

WARNING

There is a risk of damaging the AT8404 or the AMC when enabling the serial connection for an AMC that does not support this feature.

The RTM8030 has a connector (P30) with 40 differential pairs which contact the corresponding counterpart on the AT8404 (J30). The connector pinning can be found in section 3.1.8.

Following features are offered by the RTM8030 for operation with the AT8404:

- Hot swap mechanism
- Unit Computer RS232 management interface
- Unit Computer FE management interface
- One GbE SFP port (connected to the front board GbE switch)
- Two external SAS connections
- Optional SAS Hard Drive

Typical power dissipation of the RTM8030 is 10W. Operation of the optional hard drive increases power consumption to 20W.

Note...

When using AT8030 RTM with AT8404 carrier, by default the serial connection between RTM and AMC on carrier will not be granted.

Default E-Keying prevents such connection.

Default E-Keying behaviour could be change by the user in order to permit serial connection between RTM and AMC on AT8404 ATCA carrier but the following limitation will apply.

AT8030 RTM are equipped with rotary switch that permits to redirect RTM serial connection to different AMC on carrier. There is a risk to damage AMC by changing the selection with the RTM rotary switch. This risk is only present once serial connection has been established between RTM and an AMC on ATCA carrier.

3.2.1 Hot Swap

The RTM8030 supports hot swapping by using the switch connected to the face plate lower ejector. The insertion or extraction procedure is identical to the ATCA AMC behaviour. The hot swap procedure is controlled by the RTM's Module Management Controller (MMC).

3.2.1.1 Inserting the RTM8030 into the slot

The presence of the RTM is indicated by one signal. The front blade IPMC recognizes the RTM insertion when this signal is low. As soon as inserted, the MMC on the RTM turns the blue LED ON and enables the management power to the RTM. Once the I2C link is working, the IPMC of the front blade accesses the serial EEPROM to retrieve FRU data. After knowing the type of RTM inserted, the IPMC negotiates with shelf manager in order to activate the payload power. After RTM local voltages have been ramped up, the IPMC on the front blade enables the RTM Link.

3.2.1.2 Removing the RTM8030 from the slot

Opening the RTM lower ejector handle indicates to the front blade IPMC that a hot swap action is going to take place. The IPMC then negotiates the removal with the shelf manager and if it is granted, it proceeds with the removal process.

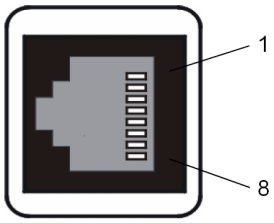
The MMC is notified that the RTM blade can be removed. The MMC then activates reset to the RTM blade, disables the RTM Link and turns off the payload power. When it is safe to remove the RTM blade from the slot, the MMC turns the Blue / Hot Swap LED on.

3.2.2 Unit Computer RS232 Management Interface

The Unit Computer's RS232 management interface is implemented as a RJ45 connector. It the lowest one of the threefold RJ45 connector, labelled with "0". The connector labelled with "1-7" is not in use.

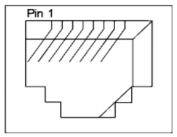
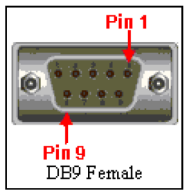
The connector has the following pinning.

Table 3-21: Serial Port (RJ45) Pin Assignment

Pin Number	Signal	RJ45
1	RTS	
2	DTR	
3	TXD	
4	GND	
5	GND	
6	RXD	
7	DSR	
8	CTS	

Connection to the RJ45 can be established with a straight through Ethernet cable and a RJ45 (female) to SubD (female) adapter if required. The adapter is described in the following table.

Table 3-22: Serial console terminal cable interface: RJ45 Female to DB9 Female

RJ45 Female	RJ45 Pin Number	Signal	Connected	Description	DB9 Pin Number	DB9 Female
 Front View	1	RTS	Y	Request To Send	8	 Front View
	2	DTR	Y	Data Terminal Ready	76	
	3	TXD	Y	Transmit	2	
	4	GND	N	Ground	-	
	5	GND	Y	Ground	5	
	6	RXD	Y	Receive	3	
	7	DSR	Y	Data Set Ready	4	
	8	CTS	N	Clear To Send	7	
	-	RI	N	Ring Indicator (Not Used)	9	
	-	DCD	N	Carrier Detect (Not Used)	1	

3.2.3 Unit Computer Fast Ethernet Management Interface

The Fast Ethernet port of Unit Computer is used as a management interface. The external FE PHY device on the front board is connected to the top RJ45 connector of the RTM.

The default setting of the AT8404's PHY is to operate in autonegotiation enabled mode, 10/100, Full or Half duplex. The two LEDs of the RJ 45 connector are controlled by the CPLD.

The connection is established with a straight trough Ethernet cable.

Table 3-23: FE Port (RJ45) Pin Assignment

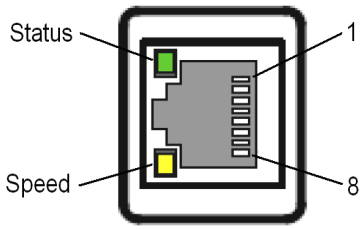
Pin Number	Signal	RJ45
1	TX+	
2	TX-	
3	RX+	
4	NC	
5	NC	
6	RX-	
7	NC	
8	NC	

Table 3-24: Fast Ethernet Management (RJ45) LEDs Signification

Speed LED (Yellow)	
OFF	10BASE-T
ON	100BASE-T
Status LED (Green)	
OFF	Link down
ON	Link up and no activity
BLINK	Link up and activity

3.2.4 GbE Port

The SFP port is connected to the front board's GbE switch. The corresponding interface is identified as 0/22.

The SFPs uplink ports are according the Small Form-factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA), Sept. 14th, 2000. The fabric switch controls the SFPs via an I²C bus. The SFP connectors have the following pin assignment:

Table 3-25: SFP Connectors Pin Assignment

Signal	Contact	Contact	Signal
GND	1	20	GND
TX_FAULT	2	19	TD-
TX_DIS	3	18	TD+
MODDEF2	4	17	GND
MODDEF1	5	16	3.3V TX
MODDEF0	6	15	3.3V RX
R_SEL	7	14	GND
LOS	8	13	RD+
GND	9	12	RD-
GND	10	11	GND

CAUTION

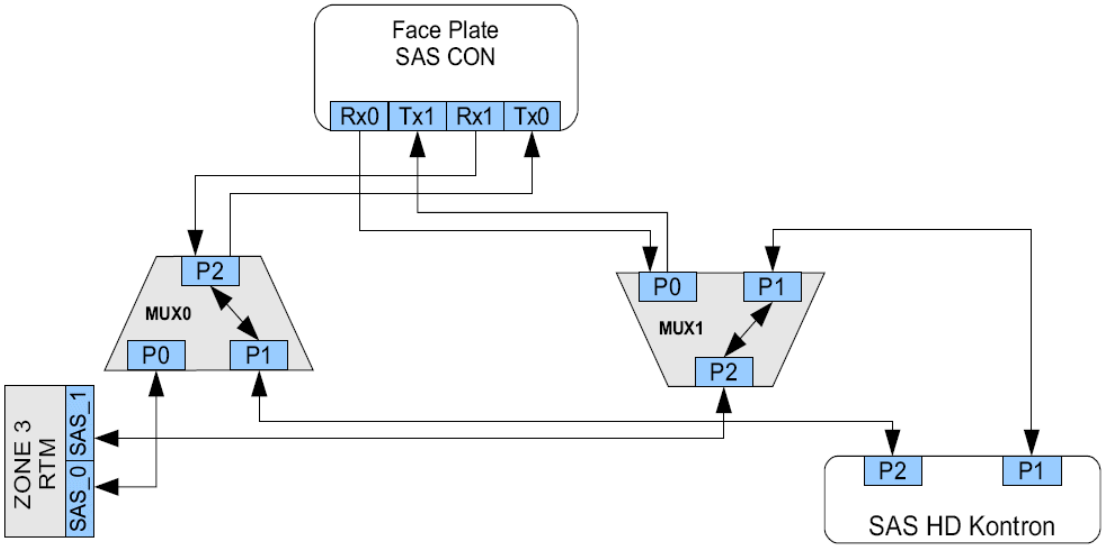
Do not look into the laser beam! The SFP modules are fitted with a class 1 or 1M laser. To avoid possible exposure to hazardous levels of invisible laser radiation, do not exceed maximum ratings.

3.2.5 SAS Channels

An external x4 SAS/SATA connector provides access to two of the AT8404 AMC bays, See “Storage Interconnect” on page 23.. The connector is a SFF-8470 fixed (receptacle) shielded connector with jack screws.

A SAS signal conditioner (repeater) and multiplexer is needed to guarantee SAS signal integrity over the cable between two RTM blades. The maximum SAS cable length between two RTM blades is 4m. SAS links work after both RTM units have been powered up. SAS port mapping is drawn below:

Figure 3-3: SAS Port Mapping

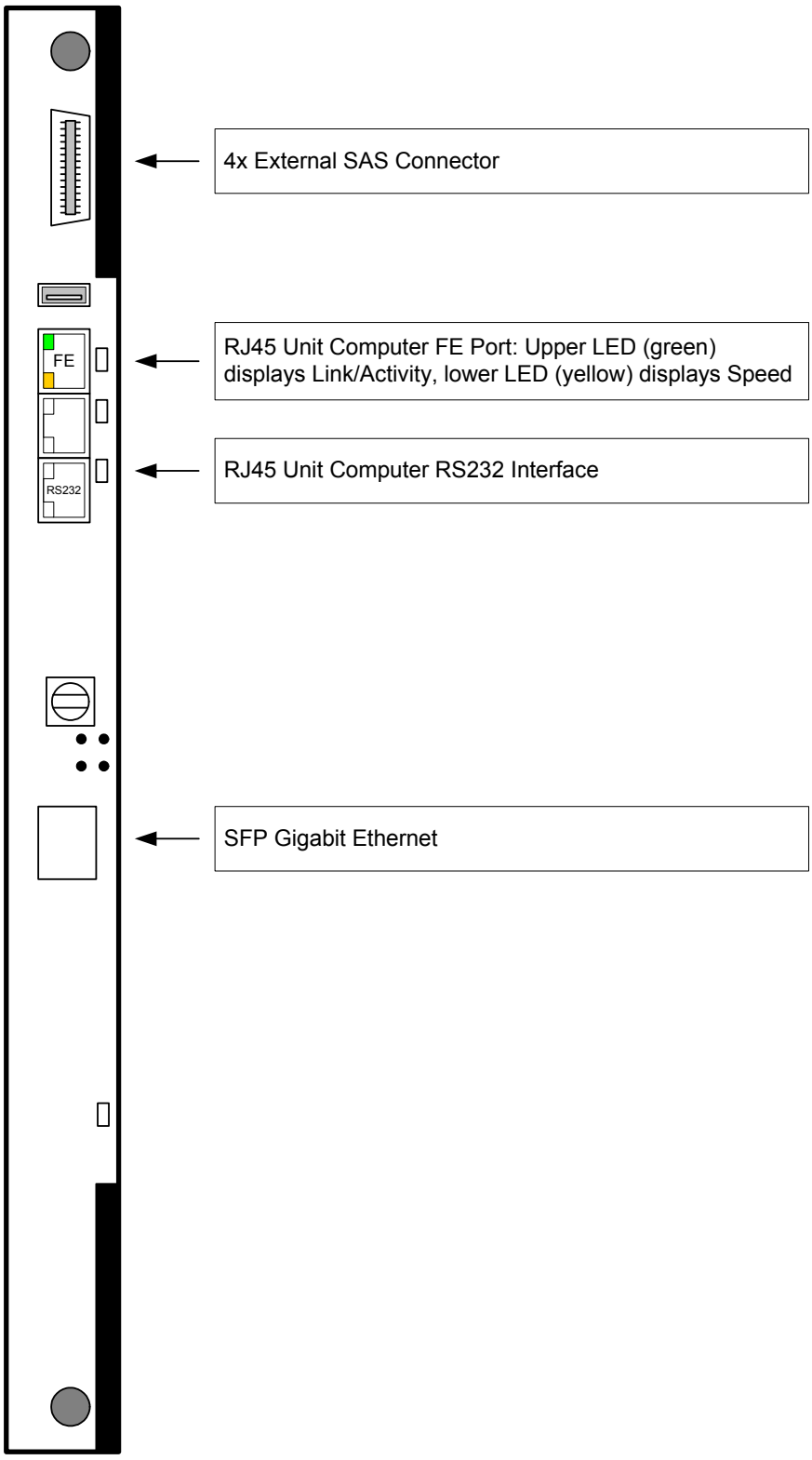


3.2.6 SAS Hard Drive Option

Kontron offers the option of adding a SAS hard drive on the RTM8030. This hard drive is located on the component side of the PCB, in the lower part of the RTM8030.

3.2.7 Display Elements

Figure 3-4: Front Panel of the RTM8030



Chapter 4

Software Description

4. Software Description

Software on the AT8404 includes the following parts:

- Bootloader
- OS (rootFS, kernel)
- Application SW
- IPMI FW

The Software accomplishes operation of the switching hardware and is therefore also referenced as firmware. It is pre-installed on the system and can only be updated by a dedicated update procedure. This manual only describes bootloader, its self tests and IMPI Firmware and introduces the update procedure.

For additional information of system configuration using CLI commands refer to documentation *AT8404 CLI Reference Manual*.

4.1 Supported RFCs, Standards and MIBs

4.1.1 Fastpath Switching

4.1.1.1 Core Features

- IEEE 802.1AB – Link level discovery protocol
- IEEE 802.1D – Spanning tree
- IEEE 802.1p – Ethernet priority with user provisioning and mapping
- IEEE 802.1Q – Virtual LANs w/ port-based VLANs
- IEEE 802.1S – Multiple spanning tree compatibility
- IEEE 802.1v – Protocol-based VLANs
- IEEE 802.1W – Rapid spanning tree
- IEEE 802.1AB – LLDP
- IEEE 802.1X – Port-based authentication
- IEEE 802.3 – 10BASE-T
- IEEE 802.3u – 100BASE-T
- IEEE 802.3ab – 1000BASE-T
- IEEE 802.3ac – VLAN tagging
- IEEE 802.3ad – Link aggregation
- IEEE 802.3ae – 10 GbE
- IEEE 802.3x – Flow control
- ANSI/TIA-1057 – LLDP-MED
- GARP – Generic Attribute Registration Protocol: clause 12, 802.1D-2004

- GMRP – Dynamic L2 multicast registration: clause 10, 802.1D-2004
- GVRP – Dynamic VLAN registration: clause 11.2, 802.1Q-2003
- RFC 4541 – IGMP snooping and MLD snooping

4.1.1.2 Additional Layer 2 Functionality

- Broadcast storm recovery
- Double VLAN/vMAN tagging
- Independent VLAN Learning (IVL) support
- Jumbo Ethernet frames
- Port mirroring
- Static MAC filtering
- IGMP and MLD snooping querier
- Port MAC locking
- MAC-based VLANs
- IP subnet-based VLANs
- Voice VLANs
- Protected ports
- Network and host DoS attack suppression

4.1.1.3 System Facilities

- Event and error logging facility
- Run-time and configuration download capability
- PING utility
- XMODEM
- RFC 768 – UDP
- RFC 783 – TFTP
- RFC 791 – IP
- RFC 792 – ICMP
- RFC 793 – TCP
- RFC 826 — ARP
- RFC 951 – BootP
- RFC 1321 – Message digest algorithm
- RFC 1534 – Interop. between BootP and DHCP
- RFC 2030 – Simple Network Time Protocol (SNTP) V4 for IPv4, IPv6, and OSI
- RFC 2131 – DHCP Client/Server
- RFC 2132 – DHCP options and BootP vendor ext.
- RFC 2865 – RADIUS client
- RFC 2866 – RADIUS accounting

- RFC 2868 – RADIUS attributes for tunnel protocol support
- RFC 2869 – RADIUS extensions
- rfc28869bis — RADIUS support for Extensible Authentication Protocol (EAP)
- RFC 3164 – The BSD syslog protocol
- RFC 3580 – 802.1X RADIUS usage guidelines

4.1.1.4 Switching MIBs (via Management Module)

- IEEE 802.1X MIB (IEEE 802.1-PAE-MIB)
- IEEE 802.1AB – LLDP MIB
- ANSI/TIA 1057 – LLDP-MED MIB
- RFC 1213 – MIB II
- RFC 1493 – Bridge MIB
- RFC 1643 – Definitions of managed objects for the Ethernet-like interface types
- RFC 2233 – Interfaces group MIB using SMI v2
- RFC 2618 – RADIUS authentication client MIB
- RFC 2620 – RADIUS accounting MIB
- RFC 2674 – VLAN MIB
- RFC 2819 – RMON groups 1, 2, 3, and 9
- RFC 2737 – Entity MIB version 2
- FASTPATH Enterprise MIBs supporting switching features

4.1.2 Fastpath Quality of Service

4.1.2.1 DiffServ

- RFC 2474 – Definition of the differentiated services field (DS Field) in the IPv4 and IPv6 headers
- RFC 2475 – An architecture for differentiated services
- RFC 2597 – Assured forwarding PHB group
- RFC 3246 – An expedited forwarding PHB (Per-Hop Behavior)
- RFC 3260 – New terminology and clarifications for DiffServ

4.1.2.2 Access Control Lists (ACLs)

- Permit/deny actions for inbound or outbound IP traffic classification based on:
  - Type of service (ToS) or differentiated services (DS) DSCP field
  - Source IP address
  - Destination IP address
  - TCP/UDP source port
  - TCP/UDP destination port
  - IP protocol number
  - IPv6 flow label

- Permit/deny actions for inbound or outbound Layer 2 traffic classification based on:
  - Source MAC address
  - Destination MAC address
  - Ethertype
  - 802.1p user priority (outer and/or inner VLAN tag)
  - VLAN identifier value or range (outer and/or inner VLAN tag)
- Optional rule attributes:
  - Assign matching traffic flow to a specific queue
  - Redirect or mirror (flow-based mirroring) matching traffic flow to a specific port
  - Generate trap log entries containing rule hit counts

4.1.2.3 Class of Service (CoS)

- Direct user configuration of the following:
  - IP DSCP to traffic class mapping
  - IP precedence to traffic class mapping
  - Interface trust mode: 802.1p, IP Precedence, IP DSCP, or untrusted
  - Interface traffic shaping rate
  - Minimum and maximum bandwidth per queue
  - Strict priority versus weighted (WRR/WFQ) scheduling per queue
  - Tail drop versus Weighted Random Early Detection (WRED) queue depth management

4.1.2.4 Quality of Service MIBs (via Management Module)

- RFC 3289 – Management Information Base for the DiffServ architecture (read-only)
- Private MIBs for full configuration of DiffServ, ACL, and CoS functionality

4.1.3 Fastpath Management

4.1.3.1 Core Features

- RFC 854 – Telnet
- RFC 855 – Telnet option specifications
- RFC 1155 – SMI v1
- RFC 1157 – SNMP
- RFC 1212 – Concise MIB definitions
- RFC 1867 – HTML/2.0 forms with file upload extensions
- RFC 1901 – Community-based SNMP v2
- RFC 1905 – Protocol operations for SNMP v2
- RFC 1906 – Transport mappings for SNMP v2
- RFC 1907 – Management Information Base for SNMP v2
- RFC 1908 – Coexistence between SNMP v1 and SNMP v2
- RFC 2068 – HTTP/1.1 protocol as updated by draft-ietf-http-v11-spec-rev-03
- RFC 2271 – SNMP framework MIB

- RFC 2295 – Transparent content negotiation
- RFC 2296 – Remote variant selection; RSVA/1.0 state management “cookies” – draft-ietf-http-state-mgmt-05
- RFC 2570 – Introduction to SNMPv3
- RFC 2571 – Architecture for describing SNMP
- RFC 2572 – Message processing and dispatching for SNMP
- RFC 2573 – SNMP v3 applications
- RFC 2574 – User-based security model for SNMP v3
- RFC 2575 – View-based access control model for SNMP
- RFC 2576 – Coexistence between SNMP v1, v2, and v3
- RFC 2578 – SMI v2
- RFC 2579 – Textual conventions for SMI v2
- RFC 2580 – Conformance statements for SMI v2
- Configurable management VLAN
- SSL 3.0 and TLS 1.0
  - RFC 2246: The TLS protocol, version 1.0
  - RFC 2346: AES ciphersuites for Transport layer security
  - RFC 2818: HTTP over TLS
- SSH 1.5 and 2.0
  - RFC 4253 - SSH transport layer protocol
  - RFC 4252 - SSH authentication protocol
  - RFC 4254 - SSH connection protocol
  - RFC 4251 - SSH protocol architecture
  - RFC 4716 - SECSH public key file format
  - RFC 4419 - Diffie-Hellman group exchange for the SSH transport layer protocol

4.1.3.2 Advanced Management Features

- Industry-standard CLI with the following features:
  - Scripting capability
  - Command completion
  - Context-sensitive help
- Optional user password encryption
- Multisession telnet server

4.2 Bootloader

On the AT8404 Carrier board, the bootloader 'u-boot' (universal bootloader) is used. The bootloader initializes the main components of the board like CPU, SDRAM, serial lines etc. for operation. After this, kernel and application are started from Flash.

4.2.1 Power on self Test

4.2.1.1 Test Routines

Upon power on or system reset, the bootloader performs a set of Power On Self Tests (POST) to check the integrity of specific components. Components where a POST is available are:

- SDRAM
- KCS
- PPC405 serial line
- PPC405 I2C
- PPC405 FE

In the case that a POST fails, a POST error code is written into the postcode high byte register of the onboard FPGA. The boot process is not stopped as there are good chances the board can boot even in case of POST errors. The postcode high byte register is also accessible by the IPMC which can report error codes to a separate management instance. Thus more comprehensive diagnostic tests could be started.

The following table shows a list of available POST routines including POST error codes.

Table 4-1: POST routines and error codes

Device	Test	POST Error Code
SDRAM	Data bus - walking 1 test	PCW_DLINE
SDRAM	Address bus - walking 1 test	PCW_ALINE
SDRAM	Memory - read/write test	PCW_MEM
PPC405 UART	Serial loopback teststring	PCW_SERIAL
PPC405 I2C	Bus scan for devices from I2C_ADDR_LIST	PCW_I2C
PPC405 FE	Phy access	PCW_ETH1
PPC405 FE	Phy loopback test using special Ethernet test frame	PCW_ETH2
KCS	KCS READY signal test	KCSCTL

4.2.1.2 Boot Steps

In addition to the Power On Self Tests described above, the bootloader logs the board startup sequence in the postcode low byte register. A postcode value is written each time a step in the start sequence has been completed successfully. The postcode stored is also accessible by the IPMC. In the case that an error occurs during execution of a step, the boot sequence is stopped because a fatal error has occurred with great likelihood. In this case, a management instance can read the last postcode written via the IPMC and thus determine where the fatal error has occurred.

A list of defined postcodes is shown in the table below.

Table 4-2: POST Boot Steps

POST Step Code	Value	Boot Step
PC_INIT	0x00	Initial PC, EBC has been set up
PC_BINIT	0x01	Board early init (interrupt settings)
PC_CLOCKS	0x02	Get system clocks
PC_TIMEB	0x03	Init timebase
PC_ENVINIT	0x04	Init environment
PC_BAUD	0x05	Init baudrate
PC_SERIAL	0x06	Init UART
PC_CPU	0x07	Check CPU
PC_PHY	0x08	Setup PHY
PC_I2C	0x09	Init I2C
PC_INITRAM	0x0A	Init SDRAM controller and SDRAM
PC_TESTRAM	0x0B	Test SDRAM
PC_INITSEQ	0x0F	Board init sequence completed
PC_INITBOARD	0x10	Board init ok, stack set up ok, board info struct set up
PC_RELOC	0x11	Relocation completed
PC_TRAP	0x18	Setup trap handler
PC_FLASH	0x19	Flash OK
PC_CPU2	0x1A	Init higher level parts of CPU
PC_RELOCENV	0x1B	Relocation of environment Ok
PC_BDINFO	0x1C	Fill missing fields of bdinfo
PC_PCI	0x1D	PCI configuration done
PC_DEVICES	0x1E	Device init done
PC_JUMPTABLE	0x1F	Jumptable init done
PC_CONSOLE	0x20	Console init done
PC_MAIN	0x2F	Enter main loop
PC_START_OS	0x3F	Pass control to OS, leave bootloader

4.2.2 Bootloader shell options

The boot process can be interrupted by entering the bootstopkey “stop”. This will open a bootloader shell session.

“?” provides a list of possible commands, “printenv” provides a list of environment settings.

The bootloader shell can be used to customize boot options and system startup.

CAUTION

Changing bootloader environment variables must be taken very carefully. It will change system behaviour.

For additional information about the bootloader and the tools to customize the u-boot, refer to:

http://sourceforge.net/projects/u-boot/

Table 4-3: Bootloader environment variables

Name	Description
ethaddr	contains the default base MAC address of the board. If this is not set, the MAC address from VPD is used.
bootcmd	This variable defines a command string that is automatically executed when the initial countdown is not interrupted. This command is only executed when the variable bootdelay is also defined!
bootcmdflash	contains the standard startup script for loading OS image from flash partition command.
bootcmdnet	contains the standard startup script for loading OS image from network
bootcmdprd	contains the standard startup script for use during board production
bootdelay	After reset, U-Boot will wait this number of seconds before it executes the contents of the bootcmd variable. During this time a countdown is printed, which can be interrupted by pressing any key. Set this variable to 0 boots without delay. Be careful: depending on the contents of your bootcmd variable, this can prevent you from entering interactive commands again forever! Set this variable to -1 to disable autoboot.
bootsetup	checks for the boot image number detected on startup and sets the OS load address respectively. It is strongly recommended not to change this variable.
bootsource	When the standard boot sequence is used, contains the boot source, either flash, net, prd to select the respective boot sequence to activate. It is only used when bootcmd contains the default startup script, which may be overridden by the user. default: flash
ethact	Current network interface used by network commands (bootp, tftpboot et al) default: ppc_4xx_eth0
loadaddr	Default load address for network transfers. This is used as a temporary storage for netbooting and firmware updates. default: 0x8000000
early_cmd	contains the standard script for setting up the pBMWD watchdog after POST has finished, but before the bootstopkey is checked

Table 4-3: Bootloader environment variables (Continued)

Name	Description
watchdogboot	0 – disable boot monitor watchdog (default) 5...n – timeout in seconds before boot monitor watchdog fires Note: This is the pBMWD watchdog
watchdogos	0 – disable OS load watchdog (default) 15...n – timeout in seconds before load OS watchdog fires Note: This is the pOSWD watchdog
ignore_posterr	0 – stop boot process if power on self test errors are detected 1 – continue boot in the presence of power on self test errors (default)
postresult	Contains the power on self tests results, as reported in the IPMI SDR.
pbmwdfire	triggers the bBMWD watchdog in case that loading the OS from flash fails. It is strongly recommended not to change this variable.
pbmwdsetup	sets the pBMWD watchdog timeout. It is strongly recommended not to change this variable.
poswdsetup	sets the pOSWD watchdog timeout. It is strongly recommended not to change this variable.

4.3 IPMI Firmware

The Unit Computer communicates with the Intelligent Platform Management Controller (IPMC) using the Keyboard Controller Style (KCS) interface. The bootloader is able to communicate with the IPMC, e.g. for POST error logging purposes and fault resilient purposes.

The memory subsystem of the IPMC consists of an integrated flash memory to hold the IPMC operation code and integrated RAM for data. The field replaceable unit (FRU) inventory information is stored in the nonvolatile memory on an EEPROM connected via a local I2C interface to the IPMC micro controller. It is possible to store up to 4 KBytes within the FRU inventory information. Communication over IPMB bus to the ShMC ensures that 'post-mortem' logging information is available even if the main processor becomes disabled.

The IPMC provides six I2C bus connections. Two are used as the redundant IPMB bus connections to the backplane, one is used for IPMB-L bus with AMC modules, one for the connection to a managed RTM, one for the Base Board and one is for local EEPROM storage.

If an IPMB bus fault or IPMC failure occurs, IPMB isolators are used to switch from and isolate the backplane/system IPMB bus from the faulted Carrier Board. If possible, the IPMC activates the redundant IPMB bus to re-establish system management communication to report the fault.

The onboard DC voltage, current, and temperature sensors are monitored by the IPMC micro controller continuously. The IPMC will log an event into the ShMC's System Event Log (SEL) if any of the thresholds are exceeded.

To increase the reliability of the AT8404 management subsystem, an external watchdog supervisor for the IPMC is implemented. The IPMC strobes the external watchdog at two-second intervals to ensure continuity of operation of the board's management subsystem. If the IPMC ceases to strobe the watchdog supervisor for more than six seconds, the watchdog isolates the IPMC from the IPMBs and resets the IPMC. The watchdog supervisor does not reset the payload power and the restart of the IPMC will not affect the payload and will restore the previous Hot Swap state and power level negotiated with the ShMC. The external watchdog supervisor is not configurable and must not be confused with the IPMI v1.5 watchdog timer commands.

4.3.1 Sensor Data Record (SDR)

Every sensor on the Base Board is associated with a Sensor Data Record (SDR). Sensor Data Records contain information about the sensor's identification such as sensor type, sensor name, sensor unit. SDR also contain the configuration of a specific sensor such as threshold/hysteresis and event generation capabilities that specifies sensor behaviour. Some field of the sensor SDR are configurable through IPMI v1.5 commands and are set to built-in initial value.

The AT8404 management controller supports sensor devices and uses the IPMI dynamic sensor population feature of IPMI v1.5 to merge the AMC hot swap sensor with the AT8404 sensors population. AMC hot swap events indicated by this sensor are passed to the ShMC. Additionally, the IPMC updates the sensor population change indicator timestamp accessible through the Get Device SDR Info command to remain compliant to IPMI v1.5.

All SDRs can be queried using Device SDR commands. Base Board sensors that have been implemented are listed below.

Table 4-4: AT8404 sensors

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
0	AT8404		-		FRU Device locator Record (SDR type 0x11)
1	IPMC Reboot	0x24 (Platform Alert)	0x03 (Digital Discrete)	Generates an event when the IPMC starts or reboots	offset 0: event trigger, Normal Condition (IPMC is running) offset 1: event trigger, IPMC has reboot see IPMI v1.5 table 36.3, Sensor type code 24h for sensor definition
2	IPMI Watchdog	0x23 (Watchdog 2)	0x6F (Sensor Specific)	Generates an event when the IPMI watchdog triggers	
3	IPMC Storage Err	0x24 (Platform Alert)	0x03 (Digital Discrete)	Generates an event when the IPMC detects an error on I2C EEPROM	offset 0: offset 1:
4	SEL State	0x10 (Event Logging Disable)	0x6F (Sensor Specific)	SEL state Generates an event for SEL fill state	offset 2: event trigger, The SEL has been cleared offset 4: event trigger, The SEL is Full offset 5: event trigger, The SEL has reached 75% of its capacity see IPMI v1.5 table 36.3, Sensor type code 10h (Event Log Disable) for sensor definition
5	FRU0 Reconfig	0x12 (System Event)	0x6F (Sensor Specific)	Generates an event when the IPMC changes configuration	offset 0:
6	EventRcv ComLost	0x1B (Cable/Interconnect)	0x03 (Digital Discrete)	Genearates an event when the IPMC loses communication to the Event receiver (ShMC)	offset 0: event trigger, communication with ShMC lost offset 1: event trigger, communication with ShMC regain see IPMI v1.5 table 36.2 and table 36.3 for sensodefinition
7	Board Reset	0xCF (Reset Sensor)	0x03 (Digital Discrete)	Generates an event when IPMC detects a reset of the payload (PPC 405)	offset 0,1 are used for details see 4.3.1.1 OEM sensor description
8	PPC Boot Error	0x1E (Boot Error)	0x6F (Sensor Specific)	Generates an event when an system boot error is detected	offset 0: event trigger - OS load failed offset 3: event trigger - Boot monitor load failed see IPMI v1.5 table 36.3, Sensor type code 1Eh (Boot Error) for sensor definition

Table 4-4: AT8404 sensors (Continued)

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
9	PPC POST Error	0x0F (System Firmware Progress)	0x6F (Sensor Specific)	Generates an event when a POST error occurred	offset 0/event data 2: 00h (unspecified): event trigger, A Boot monitor POST failure offset 0/event data 2: 0Bh (Firm. corruption.): event trigger, Boot monitor backup image loaded/ Primary boot monitor corrupted see IPMI v1.5 table 36.3, Sensor type code 0Fh (System Firmware Progress) for sensor definition
10	PPC POST Value	0xC6 (POST value sensor)	0x6F (Sensor Specific)		offset 0 to 7 and 14 are used for details see 4.3.1.1 OEM sensor description
11	PPC OS Stop	0x20 (OS Critical Stop)	0x6F (Sensor Specific)	Generates an event when OS critical stop condition occurred	only offset 1 is used for details see 4.3.1.1 OEM sensor description
12	PPC Critical Int	0x13 (Critical Interrupt)	0x03 (Digital Discrete)	Generates an event when PPC critical interrupt occurred	offset 0,1 are used, offset 0: event trigger, normal condition, no checkstop offset 1: event trigger, processor is in checkstop condition see IPMI v1.5 table 36.3, Sensor type code 03h for sensor definition
13	PPC Diag Status	0xC9 (Diagnostic Status)	0x6F (Sensor Specific)	Generates an event for the diagnostic result state	offset 0,1,2 are used for details see 4.3.1.1 OEM sensor description
14	Ext fwupg Status	0xCA (External Component Firmware Upgrade Status)	0x6F (Sensor Specific)	Generates an event for the update state of the system SW	offset 0,1,2 are used for details see 4.3.1.1 OEM sensor description
15	Switch Status	0xC8 OEM (Switch Management Status)	0x6F (Sensor Specific)	Generates an event when Swtich SW state changes	offset 0,1,2,3 are used for details see 4.3.1.1 OEM sensor description
16	FRU0 Hot Swap	0xF0 (PICMG Hot Swap)	0x6F (Sensor Specific)	PICMG hotswap sensor for FRU0	see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
17	FRU1 Hot Swap	0xF0 (PICMG Hot Swap)	0x6F (Sensor Specific)	PICMG hotswap sensor for AMC B1	see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition

Table 4-4: AT8404 sensors (Continued)

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
18	FRU2 Hot Swap	0xF0 (PICMG Hot Swap)	0x6F (Sensor Specific)	PICMG hotswap sensor for AMC B2	see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
19	FRU3 Hot Swap	0xF0 (PICMG Hot Swap)	0x6F (Sensor Specific)	PICMG hotswap sensor for AMC B3	see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
20	FRU4 Hot Swap	0xF0 (PICMG Hot Swap)	0x6F (Sensor Specific)	PICMG hotswap sensor for AMC B4	see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
21	FRU5 Hot Swap	0xF0 (PICMG Hot Swap)	0x6F (Sensor Specific)	PICMG hotswap sensor for the RTM	see PICMG 3.0R2.0 section 3.2.4.3 for event trigger and sensor definition
22	IPMB0 Link State	0xF1 (PICMG Physical IPMB-0)	0x6F (Sensor Specific)	PICMG IPMB0 link state	see PICMG 3.0R2.0 section 3.8.4.2 for event trigger and sensor definition
23	FRU0 IPMBL State	0xC3 OEM (IPMB-L link state)	0x6F (Sensor Specific)	IPMB-L link state to FRU0	offset 2 and 3 are used for details see 4.3.1.1 OEM sensor description
24	FRU1 IPMBL State	0xC3 OEM (IPMB-L link state)	0x6F (Sensor Specific)	IPMB-L link state to AMC B1	offset 2 and 3 are used for details see 4.3.1.1 OEM sensor description
25	FRU2 IPMBL State	0xC3 OEM (IPMB-L link state)	0x6F (Sensor Specific)	IPMB-L link state to AMC B2	offset 2 and 3 are used for details see 4.3.1.1 OEM sensor description
26	FRU3 IPMBL State	0xC3 OEM (IPMB-L link state)	0x6F (Sensor Specific)	IPMB-L link state to AMC B3	offset 2 and 3 are used for details see 4.3.1.1 OEM sensor description
27	FRU4 IPMBL State	0xC3 OEM (IPMB-L link state)	0x6F (Sensor Specific)	IPMB-L link state to AMC B4	offset 2 and 3 are used for details see 4.3.1.1 OEM sensor description
28	FRU5 IPMBL State	0xC3 (IPMB-L link state)	0x6F (Sensor Specific)	IPMB-L link state to the RTM	offset 2 and 3 are used for details see 4.3.1.1 OEM sensor description
29	FRU0 FRU Agent	0xC5 (FRU Info Agent)	0x6F (Sensor Specific)	Generates an event when the FRU data of this devices is parsed	offset 6,8 are used for details see 4.3.1.1 OEM sensor description
30	FRU1 FRU Agent	0xC5 (FRU Info Agent)	0x6F (Sensor Specific)	Generates an event when the FRU data of this devices is parsed	offset 6,8 are used for details see 4.3.1.1 OEM sensor description
31	FRU2 FRU Agent	0xC5 (FRU Info Agent)	0x6F (Sensor Specific)	Generates an event when the FRU data of this devices is parsed	offset 6,8 are used for details see 4.3.1.1 OEM sensor description
32	FRU3 FRU Agent	0xC5 (FRU Info Agent)	0x6F (Sensor Specific)	Generates an event when the FRU data of this devices is parsed	offset 6,8 are used for details see 4.3.1.1 OEM sensor description

Table 4-4: AT8404 sensors (Continued)

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
33	FRU4 FRU Agent	0xC5 (FRU Info Agent)	0x6F (Sensor Specific)	Generates an event when the FRU data of this devices is parsed	offset 6,8 are used for details see 4.3.1.1 OEM sensor description
34	FRU5 FRU Agent	0xC5 (FRU Info Agent)	0x6F (Sensor Specific)	Generates an event when the FRU data of this devices is parsed	offset 6,8 are used for details see 4.3.1.1 OEM sensor description
35	FRU0 Pwr Denied	0xCD (FRU Power denied),	0x03 (Digital Discrete)	Generates an event when power for this FRU was denied.	offset 0,1 are used offset 0: event trigger, Normal Condition (Power Deny deasserted) offset 1: event trigger, Shelf Manager deny Power to this FRU for details see 4.3.1.1 OEM sensor description
36	FRU1 Pwr Denied	0xCD (FRU Power denied)	0x03 (Digital Discrete)	Generates an event when power for this FRU was denied.	offset 0,1 are used, offset 0: event trigger, Normal Condition (Power Deny deasserted) offset 1: event trigger, Shelf Manager deny Power to this FRU for details see 4.3.1.1 OEM sensor description
37	FRU2 Pwr Denied	0xCD (FRU Power denied)	0x03 (Digital Discrete)	Generates an event when power for this FRU was denied.	offset 0,1 are used, offset 0: event trigger, Normal Condition (Power Deny deasserted) offset 1: event trigger, Shelf Manager deny Power to this FRU for details see 4.3.1.1 OEM sensor description
38	FRU3 Pwr Denied	0xCD (FRU Power denied)	0x03 (Digital Discrete)	Generates an event when power for this FRU was denied.	offset 0,1 are used, offset 0: event trigger, Normal Condition (Power Deny deasserted) offset 1: event trigger, Shelf Manager deny Power to this FRU for details see 4.3.1.1 OEM sensor description

Table 4-4: AT8404 sensors (Continued)

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
39	FRU4 Pwr Denied	0xCD (FRU Power denied)	0x03 (Digital Discrete)	Generates an event when power for this FRU was denied.	offset 0,1 are used, offset 0: event trigger, Normal Condition (Power Deny deasserted) offset 1: event trigger, Shelf Manager deny Power to this FRU for details see 4.3.1.1 OEM sensor description
40	FRU5 Pwr Denied	0xCD (FRU Power denied)	0x03 (Digital Discrete)	Generates an event when power for this FRU was denied.	offset 0,1 are used, offset 0: event trigger, Normal Condition (Power Deny deasserted) offset 1: event trigger, Shelf Manager deny Power to this FRU for details see 4.3.1.1 OEM sensor description
41	Temp PCB Outlet	0x01 (Temperature)	0x01 (Threshold)	PCB Outlet temperature	For sensor thresholds, see Table 4-18 on page 67
42	Temp BCM Outlet	0x01 (Temperature)	0x01 (Threshold)	BCM Outlet temperature	For sensor thresholds, see Table 4-18 on page 67
43	Temp AMC Outlet	0x01 (Temperature)	0x01 (Threshold)	AMC Outlet temperature	For sensor thresholds, see Table 4-18 on page 67
44	Temp PPC Inlet	0x01 (Temperature)	0x01 (Threshold)	PowerPC Inlet temperature	For sensor thresholds, see Table 4-18 on page 67
45	Temp AMC Inlet	0x01 (Temperature)	0x01 (Threshold)	AMC Inlet temperature	For sensor thresholds, see Table 4-18 on page 67
46	Temp PPC Outlet	0x01 (Temperature)	0x01 (Threshold)	PowerPC Outlet temperature	For sensor thresholds, see Table 4-18 on page 67
47	Icc 12v FRU0	0x03 (Current)	0x01 (Threshold)	Current on 12v board power supply	For sensor thresholds, see Table 4-16 on page 66
48	Vcc 12v FRU0	0x02 (Voltage)	0x01 (Threshold)	Voltage on 12v board power supply	For sensor thresholds, see Table 4-17 on page 67
49	Icc 3.3vSus FRU0	0x03 (Current)	0x01 (Threshold)	Current on 3.3v suspend (management) power supply	For sensor thresholds, see Table 4-16 on page 66
50	Vcc 3.3vSus FRU0	0x02 (Voltage)	0x01 (Threshold)	Voltage on 3.3v suspend (management) power supply	For sensor thresholds, see Table 4-17 on page 67
51	Vcc 1.2vSUS FRU0	0x02 (Voltage)	0x01 (Threshold)	Voltage on 1.2v suspend (management) power supply	For sensor thresholds, see Table 4-17 on page 67
52	Vcc 3.3v FRU0	0x02 (Voltage)	0x01 (Threshold)	Voltage on 3.3v board power supply	For sensor thresholds, see Table 4-17 on page 67

Table 4-4: AT8404 sensors (Continued)

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
53	Vcc 2.5v FRU0	0x02 (Voltage)	0x01 (Threshold)	Voltage on 2.5v board power supply	For sensor thresholds, see Table 4-17 on page 67
54	Vcc 1.8v FRU0	0x02 (Voltage)	0x01 (Threshold)	Voltage on 1.8v board power supply	For sensor thresholds, see Table 4-17 on page 67
55	Vcc 1.25v FRU0	0x02 (Voltage)	0x01 (Threshold)	Voltage on 1.25v board power supply	For sensor thresholds, see Table 4-17 on page 67
56	Vcc 12v FRU1	0x02 (Voltage)	0x01 (Threshold)	Voltage on 12v board power supply of FRU1	For sensor thresholds, see Table 4-17 on page 67
57	Vcc 12v FRU2	0x02 (Voltage)	0x01 (Threshold)	Voltage on 12v board power supply of FRU2	For sensor thresholds, see Table 4-17 on page 67
58	Vcc 12v FRU3	0x02 (Voltage)	0x01 (Threshold)	Voltage on 12v board power supply of FRU3	For sensor thresholds, see Table 4-17 on page 67
59	Vcc 12v FRU4	0x02 (Voltage)	0x01 (Threshold)	Voltage on 12v board power supply of FRU4	For sensor thresholds, see Table 4-17 on page 67
60	Vcc 12v FRU5	0x02 (Voltage)	0x01 (Threshold)	Voltage on 12v board power supply of FRU5	For sensor thresholds, see Table 4-17 on page 67
61	Handle Switch	0x24 (Platform Alert)	0x6F (Sensor Specific)	Shows the physical handle switch state.	offset 1 is used
62	-48V FUSES	0x08 (Power Supply)	0x6F (Sensor Specific)	Shows the state of the power entry fuses.	offset 1 and 2 are used
63	Ver change	0x2B (Version Change)	0x6F (Sensor Specific)	Generates an event when IPMC firmware changed occurred.	offset 1 is used
64	IPMI Info-1	0xC0 (Firmware Debug)	0x6F (Sensor Specific)	Internal IPMC firmware diagnostic	only for debugging purposes
65	IPMI Info-2	0xC0 (Firmware Debug)	0x6F (Sensor Specific)	Internal IPMC firmware diagnostic	only for debugging purposes

Table 4-4: AT8404 sensors (Continued)

SDR ID	Name	Sensor Type Code	Reading Type Code	Description	Event Offset
66	IPMC FwUp	0xCA (External Component Firmware Upgrade Status)	0x6F (Sensor Specific)	Generates an event for the Firmware Update manager.	for details see 4.3.1.1 OEM sensor description
67	CLK1 Status	0xD4 OEM (Clock Input Status)	0x6F (Sensor Specific)	Generates an event when CLOCK presence status for CLK1 changes.	for details see Kontron Clock Input Status
68	CLK2 Status	0xD4 OEM (Clock Input Status)	0x6F (Sensor Specific)	Generates an event when CLOCK presence status for CLK2 changes.	for details see Kontron Clock Input Status
69	PLL Status	0xD5 OEM (PLL Status)	0x6F (Sensor Specific)	Generates an event when PLL status changes. The sensor only returns valid values when payload is activatwed.	for details see Kontron PLL Status

4.3.1.1 OEM sensor description

Kontron FRU Info Agent

Table 4-5: Kontron FRU info agent sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x0A	0xC5 OEM Kontron FRU Info Agent	0x06	Transition to degraded Event Data 2 is used a bit flag error Bit 7: unspecifiedError Bit 6: notPresentError Bit 5: multirecHeaderError Bit 4: multirecDataError Bit 3: timeout error Bit 2: ipmcError Bit 1: fruDataError Bit 0: commonHeaderError Event Data 3 is used a bit flag error Bit 7: reserved Bit 6: reserved Bit 5: SetPortState Not Supported Bit 4: SetPortState Error Bit 3: reserved Bit 2: reserved Bit 1: reserved Bit 0: Match Error, Not in single link matches
		0x08	Install Error Event Data 2 is used a bit flag error Bit 7: unspecifiedError Bit 6: notPresentError Bit 5: multirecHeaderError Bit 4: multirecDataError Bit 3: timeout error Bit 2: ipmcError Bit 1: fruDataError Bit 0: commonHeaderError Event Data 3 is used a bit flag error Bit 7: SetClockState Not Supported Bit 6: SetClockState Error Bit 5: SetPortState Not Supported Bit 4: SetPortState Error Bit 3: Clock Internal Mismatch Bit 2: Clock Match Error, Not a single clock matches Bit 1: Internal mismatch Bit 0: Match Error, Not in single link matches

Kontron IPMB-L Link

Table 4-6: Kontron IPMB-L Link sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x6F	0xC3 OEM Kontron IPMB-L Link	0x02	IPMB-L Disable Event Data 2: always 0 Event Data 3: bit[7:3]: always 0 bit [2:0]: 0h = no failure 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = clock low timeout 6h = Under test (the IPM Controller is attempting to determine who is causing a bus hang) 07h = Undiagnosed Communication Failure
		0x03	IPMB-L Enable Event Data 2: always 0 Event Data 3: bit[7:3]: always 0 bit [2:0]: 0h = no failure 1h = Unable to drive clock HI 2h = Unable to drive data HI 3h = Unable to drive clock LO 4h = Unable to drive data LO 5h = clock low timeout 6h = Under test (the IPM Controller is attempting to determine who is causing a bus hang) 07h = Undiagnosed Communication Failure

Kontron POST Code Value

Table 4-7: Kontron POST code value sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x6F	0xC6 OEM Kontron POST Code Value	0x00 to 0x07	POST code LOW byte value, no event genarated on these offsets
		0x14	POST Code Error Event Trigger Event Data 2: POST Low Nibble Event Data 3: POST High Nibble

Kontron Switch Management Status

Table 4-8: Kontron Switch management status sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x6F	0xC8 OEM Kontron Switch Management Status	0x00	Switch Management Software Not Loaded (No event generated)
		0x01	Switch Management Software Initializing (No event generated)
		0x02	Switch Management Ready (No event generated)
		ox03	Switch Management Software Fail Event Data 2: 0x00 :OS configuration file corrupted 0x01: OS startup failure 0x02: Switch Management Application Fail

Kontron Diagnostic Status

Table 4-9: Kontron diagnostic status sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x6F	0xC9 OEM Kontron Diagnostic Status	0x00	Diagnostic Started
		0x01	Diagnostic PASS
		0x02	Diagnostic FAIL

Kontron External Component Firmware Upgrade Status

Table 4-10: Kontron external comp. firmw. Upgrd. Status sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x6F	0xCA OEM Kontron External Component Firmware Upgrade Status	0x00	Firmware Upgrade in Progress (no event)
		0x01	Firmware upgrade succeeded
		0x02	Firmware upgrade failed

Kontron FRU Over Current

Table 4-11: Kontron FRU over current sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x6F	0xCB OEM Kontron FRU Over Current	0x00 0x01 State Asserted / State Deasserted	Event Data 2: 0x00: Over Current on Management power. 0x01: Over Current on Payload power. Event Data 3:FRU ID

Kontron FRU Power Denied

Table 4-12: Kontron FRU Power Denied sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x03	0xCD OEM Kontron FRU Power Denied	0x00 0x01 State Asserted / State Deasserted	Event Data 2: undef ined Event Data 3: FRU ID

Kontron Reset

Table 4-13: Kontron reset sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x6F	0xCA OEM Kontron RESET	0x00 0x01 State Asserted / State Deasserted	Event Data 2: Reset Type 0x00: Warm reset 0x01: Cold reset 0x02: Forced Cold [Warm reset reverted to Cold] 0x03: Soft reset [Software jump] Event Data 3: Reset Source 0x00: IPMI Watchdog [cold, warm or forced cold] (IPMI Watchdog2 sensors gives additionnal details) 0x01: IPMI commands [cold, warm or forced cold] (Chassis control, FRU control) 0x02: Processor internal checkstop 0x03: Processor internal reset request 0x04: Reset button [warm or forced cold] 0x05: Power up [cold] 0x06: Legacy Initial Watchdog / Warm Reset Loop Detection * [cold reset] 0x07: Legacy Programmable Watchdog [cold, warm or forced cold] 0x08: Software Initiated [soft, cold, warm of forced cold] 0x09: Setup Reset [Software Initiated Cold] 0xFF: Unknown

Kontron Clock Input Status

Table 4-14: Kontron clock input status sensor

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x6F	0xD1 OEM Kontron Clock Input Status	0x00 (assertion)	CLK line A not present, CLK line B not present
		0x01 (assertion)	CLK line A present, CLK line B not present
		0x02 (assertion)	CLK line A not present, CLK line B present
		0x03 (assertion)	CLK line A present, CLK line B present

Kontron PLL Status

Table 4-15: Kontron PLL status

Event/Reading type code	Sensor type	Sensor specific offset	Event trigger
0x6F	0xD2 OEM Kontron PLL Status	0x00 - PLL locked to primary reference clock (assertion) 0x01 - PLL locked to secondary reference clock (assertion) 0x02 – PLL in holdover mode (assertion) 0x03 – PLL in free-run mode (assertion) 0x04 - PLL primary reference clock line failure (assertion/de-assertion) 0x05 - PLL secondary reference clock line failure (assertion/de-assertion)	Event Data 2: [0]: PLL locked to primary reference [1]: PLL locked to secondary reference [2]: failure on primary reference [3]: failure on secondary reference [4]: CLK1 A/B selected as reference [5]: CLK2 A/B selected as reference [6]: CLK3 A/B selected as reference [7]: Reserved Event Data 3: [0]: CLK1A 8 kHz signal present [1]: CLK1B 8 kHz signal present [2]: CLK2A 19.44 MHz signal present [3]: CLK2B 19.44 MHz signal present [4-7]: Reserved

4.3.1.2 Sensor Thresholds

Following tables show sensor thresholds for temperature, voltage, current and power sensors.

Table 4-16: Current Sensor Thresholds

SENSOR Number / ID string	Lower Non-Recoverable	Lower critical	Lower non critical	Upper non critical	Upper critical	Upper Non-Recoverable
ID=46: Icc 12v FRU0	na	na	na	3.72 A	4.50 A	na
ID=48: Icc3.3vSus FRU0	na	na	na	2.96 A	4.13 A	na

Table 4-17: Voltage Sensor Thresholds

SENSOR Number / ID string	Lower Non-Recoverable	Lower critical	Lower non critical	Upper non critical	Upper critical	Upper Non-Recoverable
ID=47: Vcc 12v FRU0	na	10.81 V	11.02 V	12.98 V	13.18 V	na
ID=49: Vcc 3.3vSus FRU0	na	2.96 V	3.15 V	3.47 V	3.66 V	na
ID=50: Vcc 1.2vSus FRU0	na	1.11 V	1.18 V	1.27 V	1.34 V	na
ID=51: Vcc 3.3v FRU0	na	2.99 V	3.17 V	3.47 V	3.66 V	na
ID=52: Vcc 2.5v FRU0	na	2.20 V	2.44 V	2.66 V	2.95 V	na
ID=53: Vcc 1.8v FRU0	na	1.74 V	1.78 V	1.93 V	1.98 V	na
ID=54: Vcc 1.25v FRU0	na	1.02 V	1.20 V	1.30 V	1.53 V	na
ID=56: Vcc 12v FRU1	na	10.09 V	10. V	13.08 V	13.80 V	na
ID=59: Vcc 12v FRU2	na	10.09 V	10.92 V	13.08 V	13.80 V	na
ID=62: Vcc 12v FRU3	na	10.09 V	10.92 V	13.08 V	13.80 V	na
ID=65: Vcc 12v FRU4	na	10.09 V	10.92 V	13.08 V	13.80 V	na
ID=68: Vcc 12v FRU5	na	10.09 V	10.92 V	13.08 V	13.80 V	na

Table 4-18: Temperature Sensor Thresholds

SENSOR Number / ID string	Lower Non-Recoverable	Lower critical	Lower non critical	Upper non critical	Upper critical	Upper Non-Recoverable
ID=40: Temp PPC Inlet	na	-40.00 °C	0.00	55.00 °C	70.00 °C	80.00 °C
ID=41: Temp PPC Outlet	na	-40.00 °C	0.00	70.00 °C	85.00 °C	95.00 °C
ID=42: Temp AMC Inlet	na	-40.00 °C	0.00	55.00 °C	70.00 °C	80.00 °C
ID=43: Temp AMC Outlet	na	-40.00 °C	0.00	70.00 °C	85.00 °C	95.00 °C
ID=44: Temp PCB Outlet	na	-40.00 °C	0.00	70.00 °C	85.00 °C	95.00 °C
ID=45: Temp BCM Outlet	na	-40.00 °C	0.00	75.00 °C	90.00 °C	100.00 °C

4.3.2 OEM Commands

The AT8404 supports the following OEM commands.

Table 4-19: Board-specific OEM Command Overview

Command Name	NetFn	LUN	Command Number
OemApGetReleaseInfo	0x30	3	0x01
OemApGetFirmCap	0x30	3	0x03
OemApSetFirmCap	0x30	3	0x04
CmdClockSetBplDriver	0x30	3	0x72
CmdClockGetBplDriver	0x30	3	0x73
CmdClockSetPLLConfig	0x30	3	0x74
CmdClockGetPLLConfig	0x30	3	0x75
CmdClockGetPLLStatus	0x30	3	0x76
ClockSetClkMux	0x30	3	0x77
ClockGetClkMux	0x30	3	0x78
ClockSetAmcClkBufferOverrride	0x30	3	0x79
CmdGetStoragePortSelection	0x30	3	0x91
CmdSetStoragePortSelection	0x30	3	0x92
CmdGetPcieClkSrc	0x30	3	0x95
CmdSetPcieClkSrc	0x30	3	0x96
Set ClockState		0	0x2C
Get ClockState		0	0x2D

4.3.2.1 OemApGetReleaseInfo

This command reads the release Information for the IPMI Firmware build.

Command Name	NetFn	LUN	Command Number
OemApGetReleaseInfo	0x30	3	0x01

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
Response Data	1	Completion Code
	2..6	Release
	7..12	Sub-Release
	13..20	Date

4.3.2.2 OemApGetFirmCap

Command Name	NetFn	LUN	Command Number
OemApGetFirmCap	0x30	3	0x03

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
Response Data	1	Completion Code
	2..19	Data

4.3.2.3 OemApSetFirmCap

Command Name	NetFn	LUN	Command Number
OemApSetFirmCap	0x30	3	0x04

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
	6..23	Data
Response Data	1	Completion Code

4.3.2.4 CmdClockSetBplDriver

This command controls the LVDS driver device on the backplane for the TELCO clocks.

Command Name	NetFn	LUN	Command Number
CmdClockSetBplDriver	0x30	3	0x72

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
	6	Device: 0 - backplane Clock Driver 1A 1 - backplane Clock Driver 1B 2 - backplane Clock Driver 2A 3 - backplane Clock Driver 2B 4 - backplane Clock Driver 3A 5 - backplane Clock Driver 3B
	7	Setting: 0 - disable 1 - enable
Response Data	1	Completion Code

4.3.2.5 CmdClockGetBplDriver

This command provides information about the LVDS driver device on the backplane for the TELCO clocks.

Command Name	NetFn	LUN	Command Number
CmdClockGetBplDriver	0x30	3	0x73

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
	6	Device: 0 - backplane Clock Driver 1A 1 - backplane Clock Driver 1B 2 - backplane Clock Driver 2A 3 - backplane Clock Driver 2B 4 - backplane Clock Driver 3A 5 - backplane Clock Driver 3B 0xFF - get all states (1 byte for each driver)
Response Data	1	Completion Code
	2	Setting

4.3.2.6 CmdClockSetPLLConfig

Command Name	NetFn	LUN	Command Number
CmdClockSetPLLConfig	0x30	3	0x74

	Byte Num	Data Field	
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)	
	6..7	Parameter (byte 6)	Setting (Byte 7)
		0 - HAL_PLL_PARAM_PLL_TIE_CLR	Adjust Interval Error Adjustment 0 – adjust phase to match reference 1 – normal
		1 - HAL_PLL_PARAM_PLL_MODE	PLL operation mode 0 – normal mode 1 – freerun mode
		2 - HAL_PLL_PARAM_PLL_OOR	Out-of-range selection 0 – 40-52ppm 1 – 64-83ppm
		3 - HAL_PLL_PARAM_RESET	Hardware reset 0 – normal operation 1 – reset
		4 - HAL_PLL_PARAM_REFERENCE_SRC	PLL Reference Clock Source Selection 0 – no PLL inputs specified 1 - PLL inputs from CLK1A & CLK1B 2 - PLL inputs from CLK2A & CLK2B 3 - PLL inputs from CLK3A & CLK3B
Response Data	1	Completion Code	

4.3.2.7 CmdClockGetPLLConfig

Command Name	NetFn	LUN	Command Number
CmdClockGetPLLConfig	0x30	3	0x75

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
	6	Parameter: 0 - HAL_PLL_PARAM_PLL_TIE_CLR 1 - HAL_PLL_PARAM_PLL_MODE 2 - HAL_PLL_PARAM_PLL_OOR 3 - HAL_PLL_PARAM_RESET 4 - HAL_PLL_PARAM_REFERENCE_SRC
Response Data	1	Completion Code
	2	Setting: Adjust Interval Error Adjustment 0 – adjust phase to match reference 1 – normal PLL operation mode 0 – normal mode 1 – freerun mode Out-of-range selection 0 – 40-52ppm 1 – 64-83ppm Hardware reset 0 – normal operation 1 – reset PLL Reference Clock Source Selection 0 – no PLL inputs specified 1 - PLL inputs from CLK1A & CLK1B 2 - PLL inputs from CLK2A & CLK2B 3 - PLL inputs from CLK3A & CLK3B

4.3.2.8 CmdClockGetPLLStatus

Command Name	NetFn	LUN	Command Number
CmdClockGetPLLStatus	0x30	3	0x76

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
Response Data	1	Completion Code
	2	Status: [0] – CLK1A monitoring status [1] – CLK1B monitoring status [2] – CLK2A monitoring status [3] – CLK2B monitoring status 1b = clock is present 0b = clock is absent] [4] – PLL reference select input status 0b = primary clock selected, 1b = secondary clock selected] [5] – PLL REF0 fail with OOR setting 0b = passed, 1b = failed [6] – PLL REF1 fail with OOR setting 0b = passed, 1b = failed [7] – PLL lock status 0b = PLL not locked, 1b = PLL locked]

4.3.2.9 ClockSetClkMux

With this command the clock MUX 0 and MUX 1 can be configured to select the sources for AMC clocks (MUX domain 0) and the sources for the backplane clocks (MUX domain 1). This configurations will be stored in NV memory of the IPMC and will be restored after powerup.

For clock e-keying purposes the indirect clock descriptors of the carrier has to be set in case of direct backplane connection, e.g. when sourcing backplane clock 3A from AMC B4 TCLKD the corresponding descriptor has to be provisioned (local clock resource 5, clock ID 8). So the IPMC can do clock match finding and send a PICMG SetClockState command to the AMC in B4 with enable state in case of a match.

For additional information about clocking configuration, see chapter 4.5 Carrier Clocking.

Command Name	NetFn	LUN	Command Number
ClockSetClkMux	0x30	3	0x77

	Byte Num	Data Field	
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)	
	6	MUX ID: 0 - MUX Domain 0	MUX ID: 1 – MUX Domain 1
	7	Device: 0 – AMC B1 TclkA 1 – AMC B1 TclkC 2 – AMC B2 TclkA 3 – AMC B2 TclkC 4 – AMC B3 TclkA 5 – AMC B3 TclkC 6 – AMC B4 TclkA 7 – AMC B4 TclkC MUX	Device: 0 – backplane 1A 1 – backplane 1B 2 – backplane 2A 3 – backplane 2B 4 – backplane 3A 5 – backplane 3C
	8	Sourced by: 0 – PLL (8kHz /19,44MHz auto selected by Clk ekeying) 1 – backplane 1A 2 – backplane 1B 3 – backplane 2A 4 – backplane 2B 5 – backplane 3A 6 – backplane 3B 7 – AMC B1 TclkB 8 – AMC B1 TclkD 9 – AMC B2 TclkB 10 – AMC B2 TclkD 11 – AMC B3 TclkB 12 – AMC B3 TclkD 13 – AMC B4 TclkB 14 – AMC B4 TclkD	Sourced by: 0 – AMC B1 TclkB 1 – AMC B1 TclkD 2 – AMC B2 TclkB 3 – AMC B2 TclkD 4 – AMC B3 TclkB 5 – AMC B3 TclkD 6 – AMC B4 TclkB 7 – AMC B4 TclkD
Response Data	1	Completion Code	

4.3.2.10 ClockGetClkMux

See CmdClockSetClkMux() command.

Command Name	NetFn	LUN	Command Number
ClockGetClkMux	0x30	3	0x78

	Byte Num	Data Field	
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)	
	6	0 – MUX A	0 – MUX B
	7	Device: 0 – AMC B1 TclkA 1 – AMC B1 TclkC 2 – AMC B2 TclkA 3 – AMC B2 TclkC 4 – AMC B3 TclkA 5 – AMC B3 TclkC 6 – AMC B4 TclkA 7 – AMC B4 TclkC	Device: 0 – backplane 1A 1 – backplane 1B 2 – backplane 2A 3 – backplane 2B 4 – backplane 3A 5 – backplane 3C
Response Data	1	Completion Code	
	2	Setting	

4.3.2.11 ClockSetAmcClkBufferOverrride

Controls the LVDS driver device on the backplane for the TELCO clocks and configure the PLL in case that the MUX domain0 is configured for PLL usage.

Command Name	NetFn	LUN	Command Number
ClockSetAmcClkBufferOverrride	0x30	3	0x79

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
	6	Device: 0 – AMC B1 TclkA 1 – AMC B1 TclkC 2 – AMC B2 TclkA 3 – AMC B2 TclkC 4 – AMC B3 TclkA 5 – AMC B3 TclkC 6 – AMC B4 TclkA 7 – AMC B4 TclkC
	7	Setting: 0 - disable 1 - enable
	8	PLL select 8Optional9 1 – 19.44MHz 2 – 8kHz 3 – 2kHz This parameter is optional when Clock Mux domain 0 is configured for PLL source
Response Data	1	Completion Code

4.3.2.12 CmdGetStoragePortSelection

This command reads the current setting of the storage switch between AMC B4 and AMC B1/AMC B3.

Command Name	NetFn	LUN	Command Number
CmdGetStoragePortSelection	0x30	3	0x91

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
	6	Device: 0 – switch located at AMC B4
Response Data	1	Completion Code
	2	Setting: 0 - the AMC B4 (port 2) is connected to AMC B1 (port 3) 1 - the AMC B4 (port 2) is connected to AMC B2 (port 2)

4.3.2.13 CmdSetStoragePortSelection

Command Name	NetFn	LUN	Command Number
CmdSetStoragePortSelection	0x30	3	0x92

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
	6	Device: 0 - switch located at AMC B4
	7	Setting: 0 - the AMC B4 (port 2) is connected to AMC B1 (port 3) 1 - the AMC B4 (port 2) is connected to AMC B2 (port 2)
Response Data	1	Completion Code

4.3.2.14 CmdGetPcieClkSrc

This command returns the selected character of the PCIe clock source.

Command Name	NetFn	LUN	Command Number
CmdGetPcieClkSrc	0x30	3	0x95

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
Response Data	1	Completion Code
	2	Clock source: 0x00 – PCIe CLK SSC 0x01 – PCIe CLK NSSC

4.3.2.15 CmdSetPcieClkSrc

This command sets the character of the PCIe clock source.

Command Name	NetFn	LUN	Command Number
CmdSetPcieClkSrc	0x30	3	0x96

	Byte Num	Data Field
Request Data	1...5	Token: 0xAB - (~T) 0xCA - (~5) 0xCC - (~3) 0xCF - (~0) 0xC8 - (~7)
	6	Clock source: 0x00 – PCIe CLK SSC 0x01 – PCIe CLK NSSC
Response Data	1	Completion Code

4.3.2.16 SetClockState

Command Name	NetFn	LUN	Command Number
Set ClockState	PICMG OEM	0	CmdId: 0x2C

See PICMG AMC.0 R2.0 table 3-44.

```
Ipmitool clk set <CLK-ID> <index> <setting> <family> <acc-lvl> <freq> [<DEV-ID>]

<CLK-ID>:
<index>:here always 0
<settings>:[7:4] ignore
[3] 1-enable, 0-disable
[2] 1-source, 0-receiver
[1:0] PLL ctrl ()
<family>:1 (Sonet/SDH/PDH)
<acc-lvl>:50 (stratum3a)
```

For complete information refer to PICMG AMC.0 R2.0 section 3.9.2.5.

From backplane (resource 5):

```
AMC B1 tclk A:ipmitool picmg clk set 1 0 0x08 1 50 8000 5
AMC B1 tclk C:ipmitool picmg clk set 2 0 0x08 1 50 8000 5

AMC B2 tclk A:ipmitool picmg clk set 3 0 0x08 1 50 8000 5
AMC B2 tclk C:ipmitool picmg clk set 4 0 0x08 1 50 8000 5

AMC B3 tclk A:ipmitool picmg clk set 5 0 0x08 1 50 8000 5
AMC B3 tclk C:ipmitool picmg clk set 6 0 0x08 1 50 8000 5

AMC B4 tclk A:ipmitool picmg clk set 7 0 0x08 1 50 8000 5
AMC B4 tclk C:ipmitool picmg clk set 8 0 0x08 1 50 8000 5
```

To backplane (resource 4):

```
AMC B1 tclk B:ipmitool picmg clk set 1 0 0x0c 1 50 8000 4
AMC B1 tclk D:ipmitool picmg clk set 2 0 0x0c 1 50 8000 4

AMC B2 tclk B:ipmitool picmg clk set 3 0 0x0c 1 50 8000 4
AMC B2 tclk D:ipmitool picmg clk set 4 0 0x0c 1 50 8000 4

AMC B3 tclk B:ipmitool picmg clk set 5 0 0x0c 1 50 8000 4
AMC B3 tclk D:ipmitool picmg clk set 6 0 0x0c 1 50 8000 4

AMC B4 tclk B:ipmitool picmg clk set 7 0 0x0c 1 50 8000 4
AMC B4 tclk D:ipmitool picmg clk set 8 0 0x0c 1 50 8000 4
```

4.3.2.17 GetClockState

Command Name	NetFn	LUN	Command Number
Set ClockState	PICMG OEM	0	CmdId: 0x2D

See PICMG AMC.0 R2.0 table 3-45.

4.3.3 Field Replaceable Unit (FRU) Information

This FRU information contains the IPMI defined Board and Product Information areas that hold the part number and serial number of the board and the Multirecord Information Area that contains the PICMG defined Point to Point Information records.

The Internal Use Area is pre-allocated to 384 bytes and is free for customer use.

This FRU information responds to FRU ID #0, which is the ID for the IPMC.

4.3.4 E-Keying

E-Keying has been defined in the PICMG 3.0 Specification to prevent board damage, prevent wrong operation, and verify fabric compatibility. The FRU data contains the board point-to-point connectivity record as described in Section 3.7.2.3 of the PICMG 3.0 specification.

When the board enters M3 power state, the shelf manager reads in the board point-to-point connectivity record from FRU and determines whether the board can enable the Gigabit Ethernet ports to the back plane. Set/Get Port State IPMI commands defined by the PICMG 3.0 specification are used for either granting or rejecting the E-keys.

Additional E-Keying is provided for connectivity between the AMC carrier and the AMC bays as described the in Section 3.9 of the AMC.0 R.2.0 specification. The Set/Get AMC Port State IPMI commands defined by the AMC.0 specification are used for either granting or rejecting the E-keys.

4.3.4.1 Clock e-keying

On the AT8404 the synchronous clock distribution can be monitored and controlled.

The synchronous clock circuit includes

- a Zarlink ZL30108 PLL that can be fed from a primary and secondary clock source coming from the ATCA backplane
- a FPGA that controls the clock distribution from and to the AMC bays
- MVLDS buffers to disable all clock outputs to backplane or AMC bays

The AT8404 implements the clock ekeying mechanism defined in the AMC.0 Rev 2 specification to prevent damage to the AT8404 and the AMC if an incompatible AMC is inserted.

The AT8404 also implements IPMI OEM commands as well as adequate CLI commands to control and monitor the on-board PLL as well as the MVLDS buffers to the ATCA backplane.

For additional information about clock e-keying please refer to the appropriate Application Note.

4.3.5 IPMC Firmware Code

IPMC firmware code is organized into boot code and operational code, both of which are stored in a flash module. Upon an IPMC reset, the IPMC executes the boot code and performs the following:

- Self test to verify the status of its hardware and memory.
- Calculates a checksum of the operational code.
- Communicates with the Firmware Upgrade Manager (FUM) in order to inform the IPMC watchdog that the current IPMC firmware is suitable for execution.

Upon successful verification of the operational code checksum, the firmware will jump to the operational code.

4.3.6 LEDs

For LED positions on the front panel, refer to chapter 3.1.11 Front Panel Elements.

4.3.6.1 Hot Swap LED (Blue LED)

The AT8404 Carrier Board supports a blue Hot Swap LED mounted on the front panel. This LED indicates when it is safe to remove the Carrier from the chassis. The on-board IPMC drives this LED to indicate the hot swap state. The following states are possible:

Table 4-20: LED state

LED state	Description
OFF	Board is in M4 state, normal state when board is in operation.
ON	Ready for hot swap
Short blink	Board is in M5 state. Deactivation in progress
Long blink	Activation in progress.

4.3.6.2 Out-Of-Service (OOS) LED (ATCA LED1)

Red LED

Table 4-21: OOS LED state

LED state	Description
ON	1) The bootup handshake between FUM and IPMC is not finished or failed 2) The firmware update is in progress and the new IPMC firmware image is copied to the FUM 3) power denied from ShMgr
Blinking	The FUM is programming the IPMC due to a firmware update or a rollback
OFF	The IPMC is operational

4.3.6.3 Health LED (ATCA LED2)

Green/Amber LED

Table 4-22: Health LED state

LED state	Description
ON (green)	None of the health sensors is asserted
ON (amber)	At least one health sensor is asserted
OFF	Payload is not activated

4.3.6.4 Customer Definable LED (ATCA LED 3)

This is an amber LED which can be used by a customer application. This LED can be controlled by PICMG 3.0 defined LED commands.

4.3.7 Hot Swap Process

The AT8404 Carrier Board has the ability to be hot-swapped in and out of a chassis. The onboard IPMC manages the power-up and power-down transitions.

In addition to captive retaining screws, the AT8404 Carrier Board has two ejector mechanisms to provide a positive cam action; this ensures the blade is properly seated. The bottom ejector handle also has a switch that is connected to the IPMC to determine if the board has been properly inserted.

When the lower ejector handle is disengaged from the faceplate, the hot swap switch will assert a signal to the IPMC, and the IPMC will move from the M4 state to the M5 state. At the M5 state, the IPMC will ask the ShMC for permission to move to the M6 state. The Hot Swap LED will indicate this state with a short blink. Once permission is received from the ShMC or higher-level software, the board will move to the M6 state. The ShMC or higher level software can reject the request to move to the M6 state. If this occurs, the Hot Swap LED returns to a solid off condition, indicating that the Carrier Board has returned to M4 state.

If the Carrier Board reaches the M6 state, either through an extraction request through the lower ejector handle or a direct command from higher-level software. The Hot Swap LED continues to flash during this preparation time, just like it does in M5 state. When payload power is successfully turned off, the Hot Swap LED remains lit, indicating it is safe to remove the AT8404 from the chassis.

4.4 Firmware Administration

On a running AT8404 system, the switching application is executed from within the WindRiver Linux operating system environment. This includes the linux kernel itself which is started by the systems bootmonitor, the root file system and the FASTPATH switching application itself. These software components, together with the IPMC image, make the AT8404 firmware.

The flash holding the AT8404 software is divided into nine partitions. Partition mtd8 which holds the basic boot initialization code is hardware write protected by default thus preventing it from being accidentially overwritten by any update procedure. Partitions mtd3 and mtd7 hold a combined image containing bootmonitor, kernel and root file system including the switching application. Four partitions are reserved for a pair of redundant bootloader environment for each image. The partition scheme of the flash is shown below.

Table 4-23: FLASH Partition Scheme (128MB)

Partition	Size [MB]	Start Address	End Address	Partition name
mtd8	0.25	FFFC0000	FFFFFFFF	Boot initialization code (U_Boot, write protected by hardware setting
mtd7	0.25	FFF80000	FFFBFFFF	SW0 - boot monitor image (U-Boot) Note (4)
	0.25	FFF40000	FFF7FFFF	SW0 - Copy of boot monitor image for SW1 (U-Boot) Note (4)
	24.75	FE680000	FFF3FFFF	SW0 - OS Image Note (1)
mtd6	38.00	FC080000	FE67FFFF	SW0 - Non-volatile storage area (JFFS2) Note (2)
mtd5	0.25	FC040000	FC07FFFF	SW0 - Redundant U-Boot environment A Note (3)
mtd4	0.25	FC000000	FC03FFFF	SW0 - Redundant U-Boot environment B Note (3)
	0.25	FBFC0000	FBF80000	Unused
mtd3	0.25	FBF80000	FBFBFFFF	SW0 - boot monitor image (U-Boot) Note (4)
	0.25	FBF40000	FBF7FFFF	SW1 - Copy of boot monitor image for SW0 (U-Boot) Note (4)
	24.75	FA680000	FBF3FFFF	SW1 - OS Image Note (1)
mtd2	38.00	F8080000	FA67FFFF	SW1 - Non-volatile storage area (JFFS2) Note (2)
mtd1	0.25	F8040000	F807FFFF	SW1 - Redundant U-Boot environment A Note (3)
mtd0	0.25	F8000000	F803FFFF	SW1 - Redundant U-Boot environment B Note (3)

Note (1)The board does support OS images up to 24,75 MB size.

Note (2)Note that only the flash partitions mtd2 and mtd6 are using the JFFS2 file system for storage. All other flash partitions are not formatted and accessible from Linux only as raw devices.

Note (3)The U-Boot boot loader uses one flash sector for storing its environment variables. These can be saved and manipulated from the U-Boot CLI and using Linux tools. To enable atomic updates of the environment variables, U-Boot uses redundant environment sectors; in case of a failure in completely writing the current sector (e.g. due to loss of power or reset during writes), it will automatically use the redundant environment. Therefore each boot monitor uses two flash sectors (partitions) for storing its environment and redundant copy.

Note (4)The boot monitor is different for firmware image 0 and firmware image 1. This is because early parts of the boot monitor have to be relocated at build time for the address they execute from. Therefore both firmware images (SW0 and SW1) contain boot monitor images able to execute on any of the possible addresses. This allows for doing a verbatim copy of SW0 to SW1 and vice versa.

4.4.1 Updating the Firmware

The update package comes as a group of packages, located in the \release\data\update folder (example release: GA-2.04):

- t5307-GA-2.04.pkg T5307 SYSTEM update (bootloader and system FW)
- t5307-ipmi-GA-2.04.hpm T5307 IPMI HPM update
- t5307-pld-update-GA-2.04.pkg T5307 PLD update

The firmware - including bootloader - image is updated using the CLI. The following precautions are met to ensure a reliable and failsafe update procedure:

- Two independent system partitions, containing system 1 and system 2 firmware. The active system is either system 1 or system 2. The independant systems are stored in flash partitions mtd3 and mtd7. This allows switching to the redundant system in case that update fails due to power loss or similar errors.
- Redundant bootloader environment sectors: When the system is updated, the bootloader environment must be changed to be able to start the updated version. The bootloader environment sector is stored twice in flash, one active version and one backup version. In case the active version is deleted during update the redundant environment is still valid and allows the bootloader to start the updated system.

A software release for the AT8404 consists of one software package file, t5307-<release>.pkg. The package contains an image of bootloader, kernel and root filesystem as well as a MD5 checksum file for consistency check.

When performing a firmware update, the software package is loaded from a remote TFTP server. A software update of the AT8404 Carrier Board is done by performing the following steps:

1. Prepare network access of the board
2. log in to the privileged exec mode of the CLI of the board
3. Download initrd image into the appropriate system (1 or 2) of the flash memory. Ensure that the currently active images are not overwritten

```
(Ethernet Fabric) #copy tftp://192.168.50.5/<image-name>.pkg image1
```

This downloads the specified initrd package file via TFTP and writes the image into the partition of the specified system (1). The CRC32 checksum of the image is checked while writing it into flash. It is recommended **not** to use the currently active image.

4. Note: New SW will always use a default configuration
5. Select a system for next boot

```
(Ethernet Fabric) #boot system image1
```

This command enables the system 1 for the next system restart. In the case that the board hangs due to a corrupted software image, this will be detected and the board is automatically rebooted with the second image (2). This way, a fail-safe upgrade of the AT8404 software is possible.

6. Check availability of valid boot image in image1 using the command

```
(Ethernet Fabric) #show bootvar
Image Descriptions
    image1 : Product ID          : 5307
             Product Variant     : 0
             U-Boot Release      : GA 2.04
             Manufacturer ID     : 15000
             Build-Date          : 20080131185554
```

```
  image2 : Product ID          : 5307
           Product Variant     : 0
           U-Boot Release      : GA 2.03
           Manufacturer ID     : 15000
           Build-Date          : 20080131185554

Images currently available on Flash

image1 (U-Boot)   image2 (U-Boot)   current-active  next-active
----------------  ----------------  --------------  --------------
GA 2.04           GA 2.03           image2          image1
```

7. Restart the board

```
(Ethernet Fabric) #reload
```

8. It is recommended to copy image 1 to image 2 to have a fully redundant system

```
(Ethernet Fabric) #copy image2 image1
```

4.4.2 Updating IPMI FW

Updating the IPMI firmware is different from updating the other software parts as updating is done directly when invoking the download command. In case that the update procedure fails or the update image is corrupted, the IPMC will be able to restart all the same by means of its rollback functionality. The IPMI software package file is stored in the result/ppc405/firmware path of the release directory tree. To update the IPMI firmware, the CLI command 'download' is used:

```
(Ethernet Fabric) #download ipmifw tftp://10.0.111.1/t5307-ipmi-GA-2.04.hpm

Flashing a new IPMI firmware will disable the IPMI Controller for some minutes.
Are you sure to update the IPMI firmware? (y/n)y

Please ignore watchdog messages on console while download is in progress!

Downloading image, this may take some minutes...
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
IPMI Watchdog: response: Error ff on cmd 22
PICMG HPM.1 Upgrade Agent 1.0.2:
Validating firmware image integrity...OK
Performing preparation stage...OK
Performing upgrade stage:
```

```
--------------------------------------------------------------------------------
|ID | Name       |    Versions           |    Upload Progress   | Upload| Image |
|   |            | Active| Backup| File  |0%       50%     100%| Time  | Size  |
|---|------------|-------|-------|-------||----+----+----+----||-------|-------|
| 1 |IPMC        |  5.24 |  5.24 |  5.24 ||...................Performing activation
stage:
|| 01.26 | 354e5 |
--------------------------------------------------------------------------------
Waiting firmware activation...OK

Firmware upgrade procedure successful

Successfully transferred IPMI firmware image tftp://10.0.111.1/t5307-ipmi-GA-
2.04.hpm

(Ethernet Fabric) #
```

4.4.2.1 Updating IPMI FW of an AMC

There is also a possibility to update the IPMI FW of any AMC plugged into an AMC slots. Pre-requisite is an HPM.1 compatible format of the IPMI FW update image.

To do the update use the CLI command (example updating AMC FW plugged into slot B1):

```
(Ethernet Fabric) #download amcipmifw tftp://192.168.50.5/ipmi.hpm amcb1

Flashing a new IPMI firmware will disable the IPMI Controller for some minutes.
Are you sure to update the IPMI firmware? (y/n)y
...
(Ethernet Fabric) #
```

4.4.3 Updating PLD

Note...

PLD (FPGA) updates should be treated very carefully. Please refer to Software Release Notes about information, whether a PLD update is required at all.

Note...

To update from GA 2.03 or earlier to GA 2.04 or later, please install first new system firmware, since the PLD package format and thus update procedure has changed.

The onboard FPGA can be updated using the 'copy' command from the Fastpath CLI:

```
(Ethernet Fabric) #copy tftp://<ip_addr>/t5307-pld-update-GA-2.04.pkg image2

Mode........................................... TFTP
Set Server IP.................................. 192.168.50.5
Path........................................... ./
Filename....................................... t5307-pld-update-GA-2.04.pkg
Data Type...................................... Code
Destination Filename........................... image2

Management access will be blocked for the duration of the transfer
Are you sure you want to start? (y/n) y
Write image to flash starting...

File transfer operation completed successfully.

(Ethernet Fabric) #
```

Note...

The new FPGA code will be used after the next power-cycle of the complete board. This means that the board must be removed and re-inserted from its slot.

4.5 Carrier Clocking

4.5.1 Clock source to AMC

The receive clocks of each AMC in the Carrier can be provided by different sources:

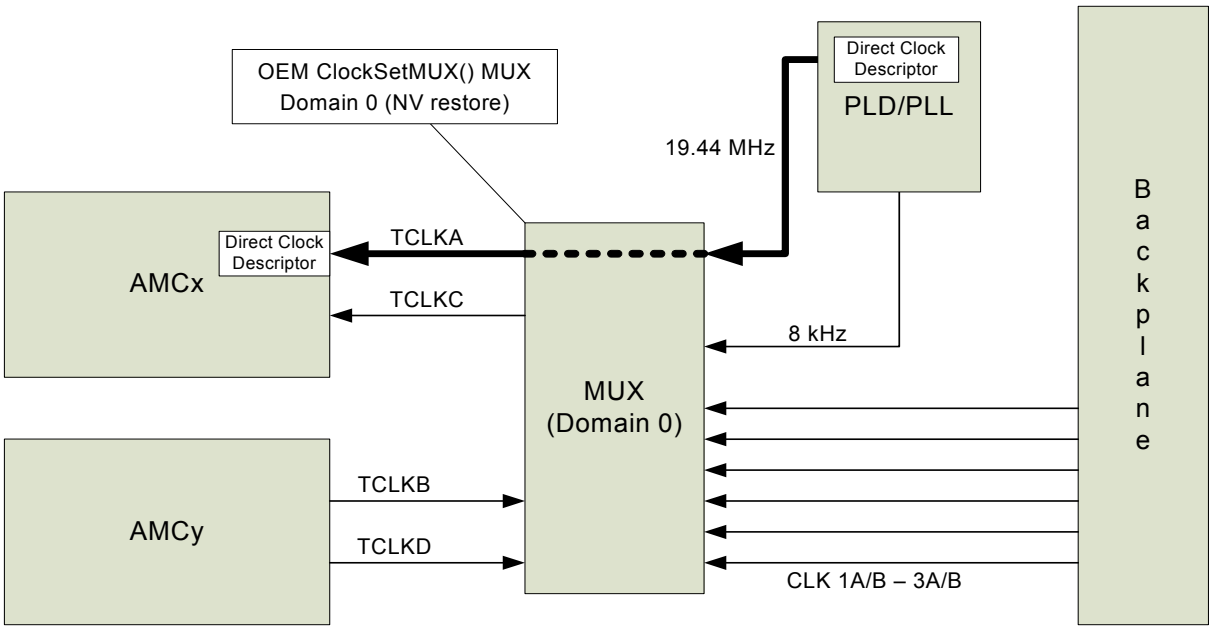
- From PLL (8kHz frame-pulse or 19,44MHz)
- From backplane clock
  This needs indirect clock configuration that has to be set previously, see example.
- From another AMC in the carrier
  The FPGA can route all AMC output clocks (TCLKB or TCLKD) of all four AMC slots to all AMC input clocks (TCLKA and TCLKC) of all four AMC slots.

4.5.1.1 Clock ekeying

IPMI needs preselected connection settings for automatic "matchfinder" (see 4.5.3 Examples), e.g. AMC B1 TCLKA is sourced by:

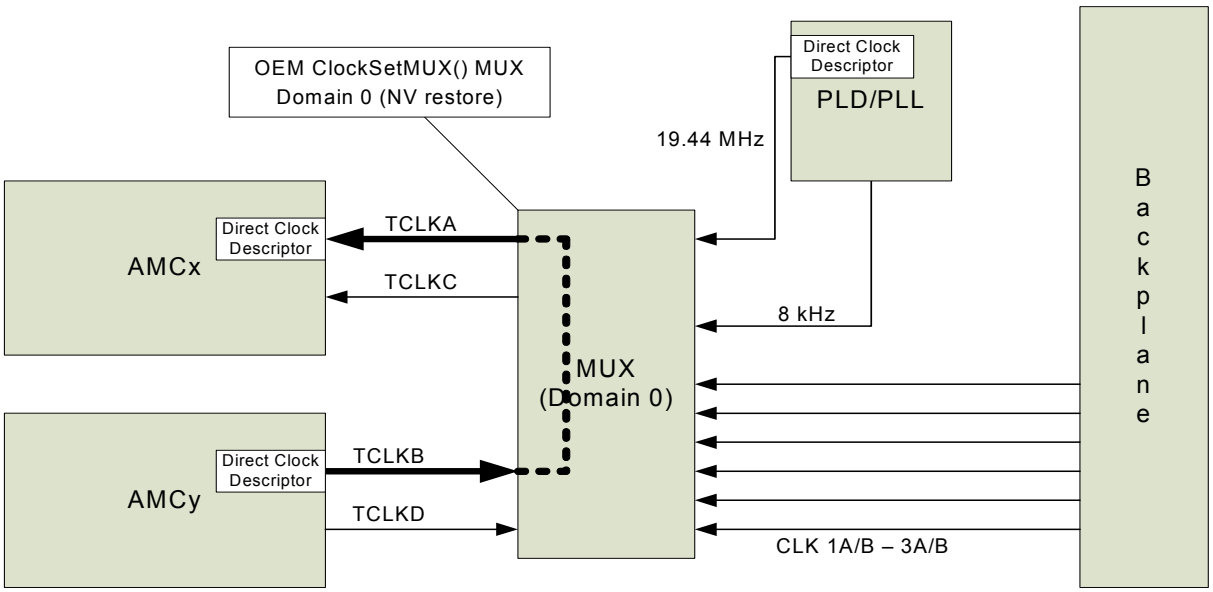
- PLL

Figure 4-1: AMC TCLKA sourced by PLL



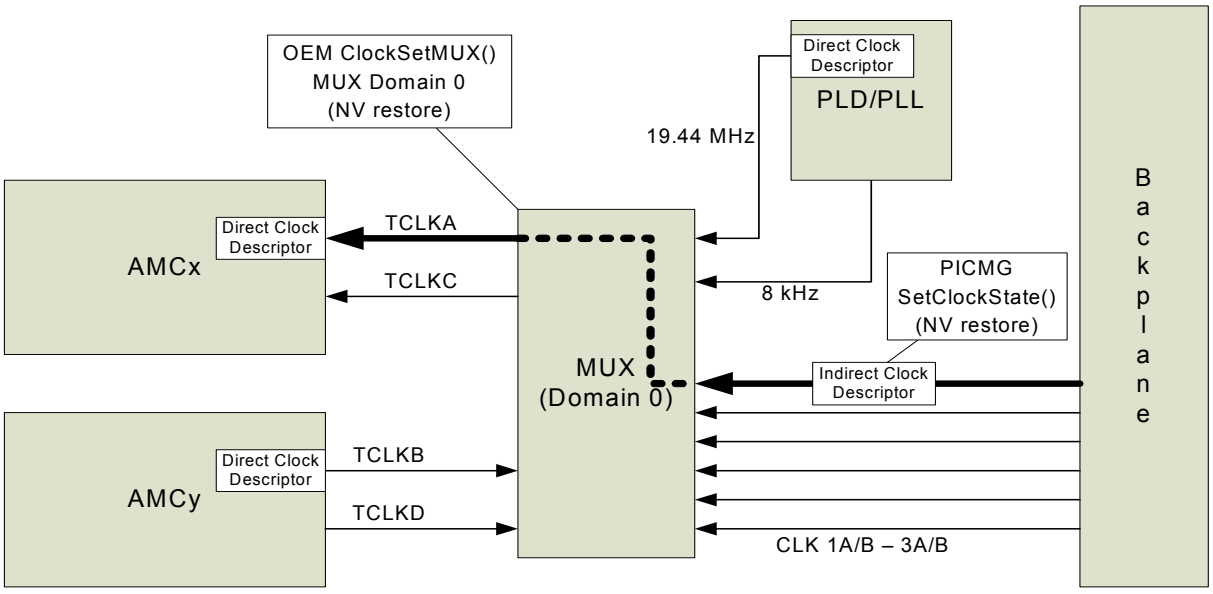
- AMC B1 TCLKA is sourced by AMC B2 (TCLKB)

Figure 4-2: AMC TCLKA sourced by AMC TCLKB



- AMC B1 TCLKA is sourced by backplane (shortcut to PLL)

Figure 4-3: AMC TCLKA sourced by backplane



All AmcSetClockState() commands will be sent during the activation phase of the modules and after the match finding process in case of a match. For a list of OEM commands and additional information, see chapter 4.3.2 OEM Commands.

The MUX (domain 0) selection is stored in NV-memory and is restored after powerup.

The MUX (domain 0) selection affects the clock ekeying match finder.

Note...

The settings of the indirect clock configuration is stored in NV-memory and is restored after powerup.

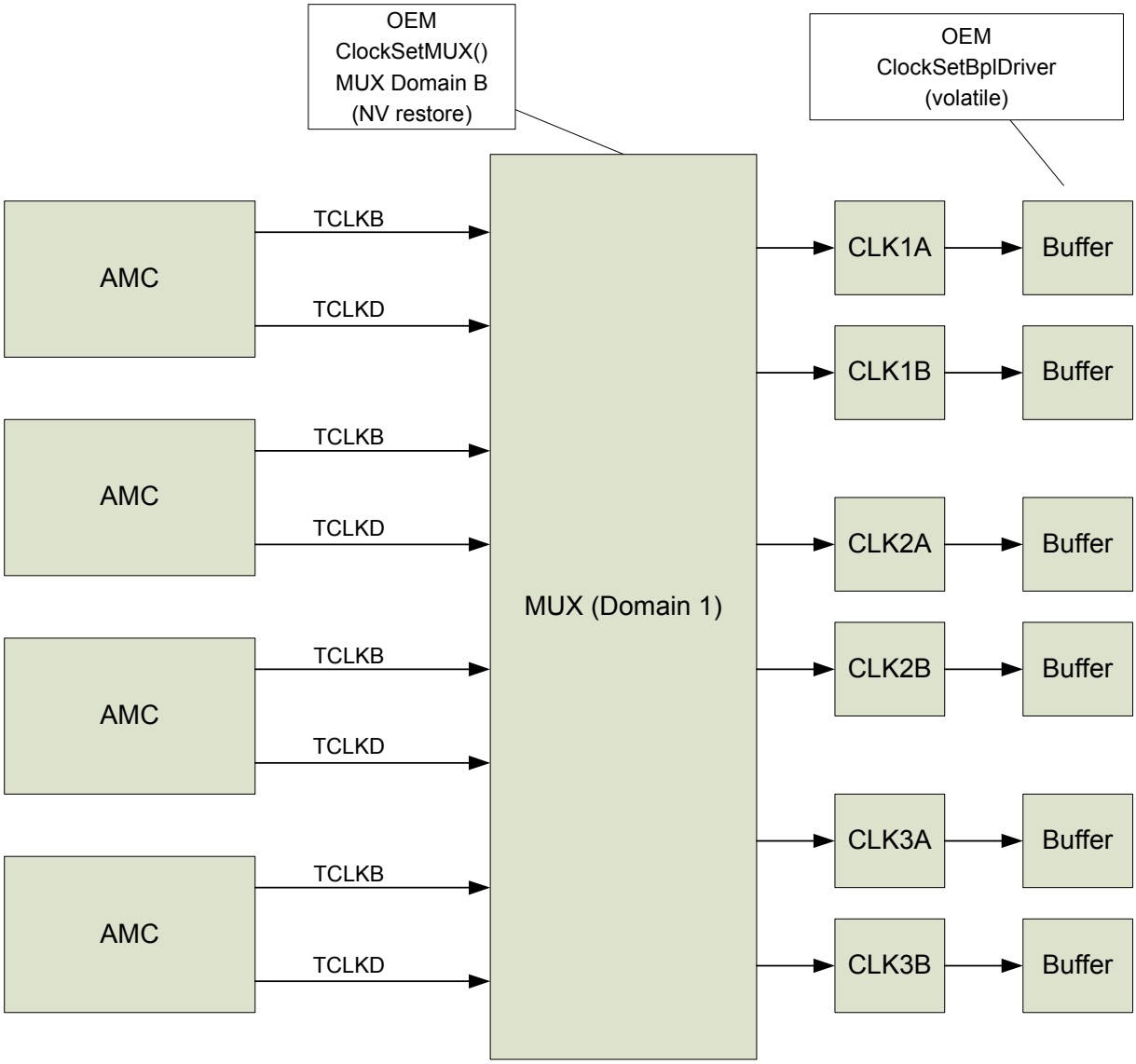
4.5.2 Clock source to backplane from any AMCs TCLK-B/D

The Clock source selection is done by OEM mechanism with automatic NV restore.

Enabling the clock buffer to the backplane is done via an OEM command (ClockSetBpldriver).

The MUX (domain 1) selection is stored in NV-memory and is restored after powerup.

Figure 4-4: Clock source from AMC to backplane

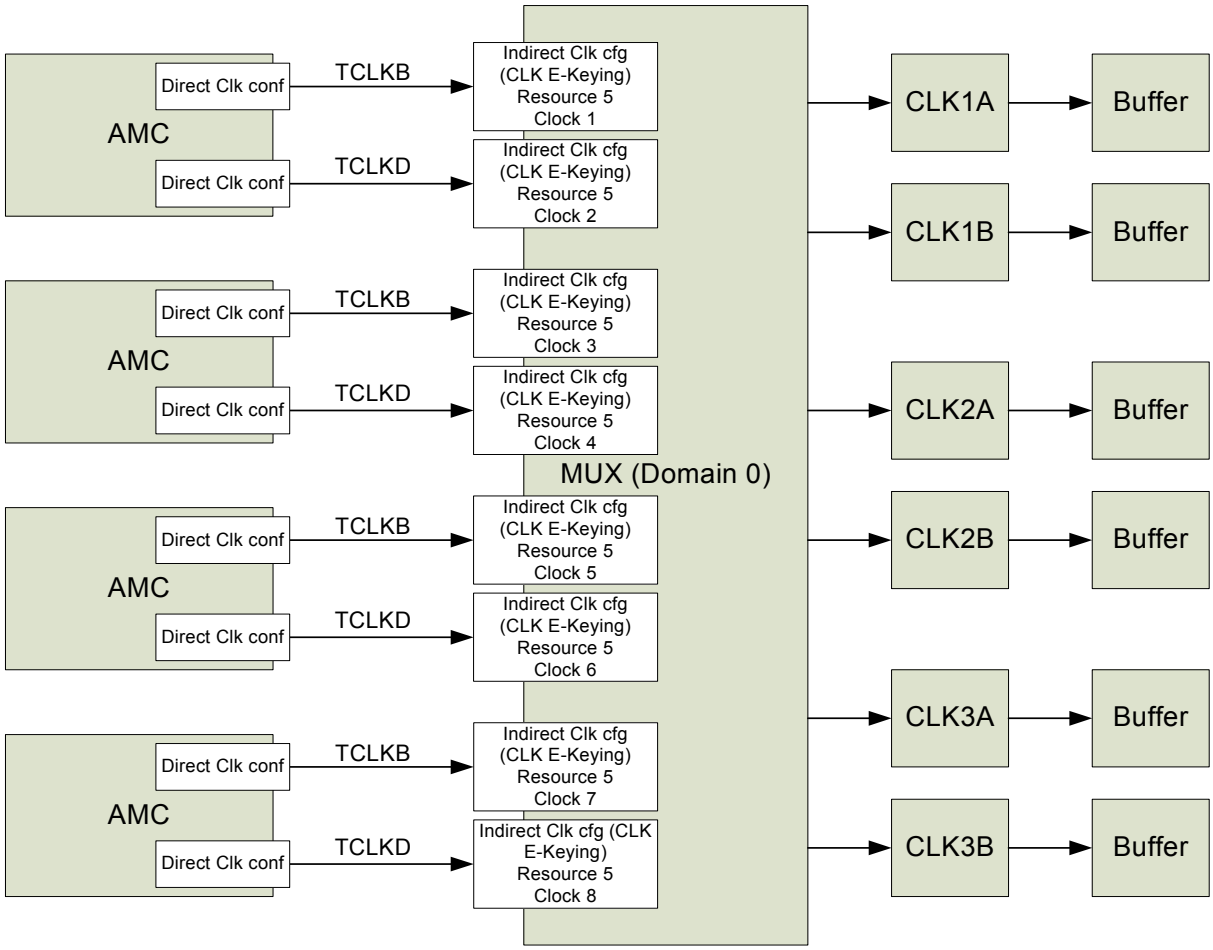


4.5.2.1 Clock ekeying

Endpoint for the clock match finder has to be set in indirect clock configuration. This setting is required for the match finder to enable the clock source on AMC.

The settings of the indirect clock configuration is stored in NV-memory and is restored after powerup.

Figure 4-5: Clock ekeying



4.5.3 Examples

4.5.3.1 Example 1

Configure clock from AMC B1 TCLKB (8kHz) to be driven to backplane CLK3A.

Configure clock from AMC B2 TCLKB (8kHz) to be driven to backplane CLK3B.

1. Configure MUX (domain 1) for AMC B1

```
(Ethernet Fabric) #set board clock mux-bpl clk3a amcb1 tclkb
```

2. Set indirect clock descriptor (necessary for clock ekeying match finder)

```
(Ethernet Fabric) #set board clock receiver amcb1 tclkb enable sonet stratum3E 8kHz
```

3. Configure MUX (domain 1) for AMC B2

```
(Ethernet Fabric) #set board clock mux-bpl clk3b amcb2 tclkb
```

4. Set indirect clock descriptor (necessary for clock ekeying match finder)

```
(Ethernet Fabric) #set board clock receiver amcb2 tclkb enable sonet stratum3E 8kHz
```

5. Enable driver to backplane clock 3A and clock 3B

```
(Ethernet Fabric) #set board clock bpl clk3a enable
(Ethernet Fabric) #set board clock bpl clk3b enable
```

Note: The settings for the backplane driver are not automatically restored after power up.

```
(Ethernet Fabric) #show boardinfo clock amc
AMC clock    Source/Target     State     Family     Accuracy       Frequency
-----------  ----------------- --------- ---------- -------------- -----------
amcb1 tclka  from: pll         disable
amcb1 tclkb  to  : bpl         enable    sonet(1)   stratum3E(50)  8kHz
amcb1 tclkc  from: pll         disable
amcb1 tclkd  to  : bpl         disable
amcb2 tclka  from: pll         disable
amcb2 tclkb  to  : bpl         enable    sonet(1)   stratum3E(50)  8kHz
amcb2 tclkc  from: pll         disable
amcb2 tclkd  to  : bpl         disable
amcb3 tclka  from: pll         disable
amcb3 tclkb  to  : bpl         disable
amcb3 tclkc  from: pll         disable
amcb3 tclkd  to  : bpl         disable
amcb4 tclka  from: pll         disable
amcb4 tclkb  to  : bpl         disable
amcb4 tclkc  from: pll         disable
amcb4 tclkd  to  : bpl         disable


(Ethernet Fabric) #show boardinfo clock bpl
BPL clock  Driver    Source
---------  --------  -----------
clk1a      disabled  amcb1 tclkb
clk1b      disabled  amcb1 tclkb
clk2a      disabled  amcb1 tclkb
clk2b      disabled  amcb1 tclkb
clk3a      enabled   amcb1 tclkb
clk3b      enabled   amcb2 tclkb
```

4.5.3.2 Example 2

Configure clock TCLKC (8kHz) to AMCB2 sourced by backplane CLK1A (PLL bypass).

1. Configure MUX (domain 0)

```
(Ethernet Fabric) #set board clock mux-amc amcb2 tclkc bpl clk1a
```

2. Set indirect clock descriptor (necessary for clock ekeying match finder)

```
(Ethernet Fabric) #set board clock source amcb2 tclkc enable sonet stratum3E 8kHz
```

3. Check config

```
(Ethernet Fabric) #show boardinfo clock amc
AMC clock    Source/Target     State     Family     Accuracy       Frequency
-----------  ----------------- --------- ---------- -------------- -----------
amcb1 tclka  from: pll         disable
amcb1 tclkb  to  : bpl         disable
amcb1 tclkc  from: pll         disable
amcb1 tclkd  to  : bpl         disable
amcb2 tclka  from: pll         disable
amcb2 tclkb  to  : bpl         disable
amcb2 tclkc  from: bpl clk1a   enable    sonet(1)   stratum3E(50)  8kHz
amcb2 tclkd  to  : bpl         disable
amcb3 tclka  from: pll         disable
amcb3 tclkb  to  : bpl         disable
amcb3 tclkc  from: pll         disable
amcb3 tclkd  to  : bpl         disable
amcb4 tclka  from: pll         disable
amcb4 tclkb  to  : bpl         disable
amcb4 tclkc  from: pll         disable
amcb4 tclkd  to  : bpl         disable
```

4.6 Carrier Configuration

4.6.1 Switch default settings

For the standard product, 3 different VLANs are configured to separate BI and FI (channel 1 and 2) traffic.

Setup VLANs:

- 4001 for BI channel 2
- 4002 for FI channel 1
- 4003 for BI channel 2

The following shows an output of /mnt/fastpath/startup-config:

```
vlan database
! vlan 1 is BI Channel_1 untagged
vlan 4001
vlan 4002
vlan 4003
vlan name 4001 BI_Channel_2
vlan name 4002 FI_Channel_1
vlan name 4003 FI_Channel_2
exit

configure


! configure all interfaces
! Into their respective VLANs
interface 0/1
description AMC_B1_FI_Port_8
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
```

```
vlan pvid 4002
vlan tagging 4003
exit

interface 0/2
description AMC_B1_FI_Port_9
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/3
description AMC_B1_FI_Port_10
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/4
description AMC_B1_FI_Port_11
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/5
description AMC_B1_BI_Port_0
vlan participation include 4001
vlan tagging 4001
exit

interface 0/6
description AMC_B2_FI_Port_8
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/7
description AMC_B2_FI_Port_9
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/8
description AMC_B2_FI_Port_10
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit
```

```
interface 0/9
description AMC_B2_FI_Port_11
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/10
description AMC_B2_BI_Port_0
vlan participation include 4001
vlan tagging 4001
exit

interface 0/11
description AMC_B3_FI_Port_8
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/12
description AMC_B3_FI_Port_9
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/13
description AMC_B3_FI_Port_10
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/14
description AMC_B3_FI_Port_11
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/15
description AMC_B3_BI_Port_0
vlan participation include 4001
vlan tagging 4001
exit
```

```
interface 0/16
description AMC_B4_FI_Port_8
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/17
description AMC_B4_FI_Port_9
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/18
description AMC_B4_FI_Port_10
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/19
description AMC_B4_FI_Port_11
vlan participation exclude 1
vlan participation include 4002
vlan participation include 4003
vlan pvid 4002
vlan tagging 4003
exit

interface 0/20
description AMC_B4_BI_Port_0
vlan participation include 4001
vlan tagging 4001
exit

interface 0/21
description UC_ETH0
no auto-negotiate
speed 100 full-duplex
vlan participation include 4001
vlan participation include 4002
vlan participation include 4003
vlan tagging 4001
vlan tagging 4002
vlan tagging 4003
exit

interface 0/22
description RTM_Port_0
vlan participation include 4001
vlan participation include 4002
vlan participation include 4003
vlan tagging 4001
vlan tagging 4002
vlan tagging 4003
exit
```

```
interface 0/23
description BI_Channel_1
exit

interface 0/24
description BI_Channel_2
vlan participation exclude 1
vlan participation include 4001
vlan pvid 4001
exit

interface 0/25
description FI_Channel_1
vlan participation exclude 1
vlan participation include 4002
vlan pvid 4002
exit

interface 0/26
description FI_Channel_2
vlan participation exclude 1
vlan participation include 4003
vlan pvid 4003
exit

exit
```

4.6.2 Using SNMP

For the AT8404, Kontron provides several MIBs in addition to the Standard MIBs (see chapter 4.1 Supported RFCs, Standards and MIBs) that allows to use SNMP for configuration of :

- clocking
- IPMI features
- extended Ethernet features
- PCI
- SGA/GA
- Storage

To use the MIBs, you must import the MIBs into the MIB browser. The MIBs are provided on demand and are part of the update package for current releases.

Kontron specific MIBs start with a “kex_”. Here‘s a list of MIBs provided (in this example for release GA 3.2) including its content:

- kex_config
  - ACL Trap Sleep Time
  - Delete Configuration File
  - DHCP-Relay circuit ID interface
  - DHCP Client Identifier

- kex_ipmi
  - Basic IPMI features:
    - Sensor list
    - SEL entries
    - FRU entries
    - FRU-Device information
    - FRU-Control commands
  - Extended IPMI monitoring functions
    - Site table
    - SEL-trap filter
    - SEL-trap
- kex_mgmt
  - Egress COS drop counter
  - Packet Memory Management
  - Protection Port Groups
  - Advertise Speed
  - Update/Startup status
  - LAG multicast hashing
  - VLAN multicast flooding
  - port multicast flooding
  - LAG unicast enhanced hashing
  - Send IGMP reports
  - CPU load
  - Port learning
  - Fast Reload
  - Memory Usage
  - L2 port bridge
- kex_ref
  - basic Kontron Information
- kex_t5307
  - PCIe commands
  - Storage commands
  - PLL configuration commands
  - Clocking commands
- kex_version
  - basic IPMI features supported)
  - support SGA address
  - support PCB version of board
  - support write-protect feature

Of course, SNMP can also be used for updating System Software, IPMI FW and PLD.

4.6.2.1 Configuring SNMP traps

Sending SNMP traps from the AT8404 carrier can be configured either from FASTPATH CLI or using SNMP.

The following example configures an SNMP trap for PLL state changes (for information about IPMI sensor definition, see “OEM sensor description” on page 62.).

- Configure SNMP trap receiver (example: Trap name: testtrap, IP-address: 10.0.0.114)

```
(Ethernet Fabric) configure
(Ethernet Fabric) (Config)#snmptrap testtrap ipaddr 10.0.0.114
```

- Enable the generation of traps (for a PLL status change). Please note, there are other traps that are enabled by default (e.g. Link Up/Down trap)

```
(Ethernet Fabric) (Config)#snmp-server enable traps pll
(Ethernet Fabric) (Config)#exit
```

- Check for correct trap settings

```
(Ethernet Fabric) #show  trapflags

Authentication Flag.......................... Enable
Link Up/Down Flag............................ Enable
Multiple Users Flag.......................... Enable
Spanning Tree Flag........................... Enable
PLL Traps.................................... Enable
ACL Traps.................................... Disable
Captive Portal Flag.......................... Disable
```

For additional information on how to use the CLI commands, refer to the” AT8404 CLI Reference Manual”.

Configuring traps using SNMP (<ip-addr> is the Mgmt IP address of the AT8404 carrier):

- Create new trap server with any name (new table entry)

```
snmpset <args> <ip-addr> agentSnmpTrapReceiverCreate.0 s "testtrap"
```

- Configure the ip address of the trap server and enable it (related to table index = 0):

```
snmpset <args> <ip-addr> agentSnmpTrapReceiverIPAddress.0 a 10.0.0.114
snmpset <args> <ip-addr> agentSnmpTrapReceiverStatus.0 i active
```

- Enable the generation of traps (for a PLL status change)

```
snmpset <args> <ip-addr> pllTrapFlag i enable
```

- For creating and configuring a second trap-server(table index =1)

```
snmpset <args> <ip-addr> agentSnmpTrapReceiverCreate.0 s "testtrap2"
snmpset <args> <ip-addr> agentSnmpTrapReceiverIPAddress.1 a 10.0.0.115
snmpset <args> <ip-addr> agentSnmpTrapReceiverStatus.1 i active
```

<args> for using all MIBs in the given directory with SNMPv2:

```
-v 2c -c private -M /usr/share/snmp/mibs:/home/rhoyler/proj/SNMP/FP5MIBS -m +ALL
```

4.6.3 Using the “current-settings” file

The current-settings file is used to do the default configuration of the carrier with respect to:

- network interface configration
- watchdog configuration
- SSH configuration
- IPMI over LAN configuration
- DHCP configuration

Using the file to change any default configuration must be taken very carefully to avoid misconfigurations.

To check and edit the /mnt/os/current-settings file you must either be logged in with a serial connection or you must be logged in using telnet port 2323. To use the telnet connection you must first enable telnet port 2323 access (see 4.6.3.2 Enabling SSH to access the Carrier).

The following output shows an example /mnt/os/current-settings file. The comments in the file provide information about default settings and possible setting changes that can be made and the effects the changes might have.

```
##
## Configuration Settings for T5307
## This is a template file
##
## set to yes to start BCM shell instead of normal
## startup
## Note that you should also disable the pOSWD
## and pWD watchdogs in this case
CONFIG_START_BCMSH="no"
# set this to yes to interrupt boot procedure
# prior to FASTPATH startup
# mainly used for debugging
CONFIG_START_MENU="no"
## set to yes to start OS telnetd on port 2323
CONFIG_START_TELNETD="yes"
# note that you need to have SSHD keys
# generated and included in configuration
# for SSHD to work.
# Keys should be stored in
#/etc/ssh/ssh_host_key
#/etc/ssh/ssh_host_rsa_key
#/etc/ssh/ssh_host_dsa_key
#
# You may do this by adding them to /mnt/os/extra-profile
# settings tar.gz file
#
# generate them on Linux using:
#  ssh-keygen -q -t rsa1 -f /etc/ssh/ssh_host_key -C '' -N ''
#  ssh-keygen -q -t rsa -f /etc/ssh/ssh_host_rsa_key -C '' -N ''
#  ssh-keygen -q -t dsa -f /etc/ssh/ssh_host_dsa_key -C '' -N ''
# You may then create an extra-profile with them in it:
#  tar -C / -zcvf /mnt/os/extra-profile /etc/ssh/ssh_host_*
CONFIG_START_SSHD="no"
## set to yes to start NFS portmapper
CONFIG_START_PORTMAP="no"

## Set this to "yes" to start the IPMI over Lan daemon.
## Access parameters may then be adjusted in /etc/ipmi_lan.conf.
##
CONFIG_START_IPMILAN="no"
```

```
##
## Set to "no" to disable all network
## interfaces.
##
## Configuration Settings for T5307
## This is a template file
##

## set to yes to start BCM shell instead of normal
## startup
## Note that you should also disable the pOSWD
## and pWD watchdogs in this case
CONFIG_START_BCMSH="no"
# set this to yes to interrupt boot procedure
# prior to FASTPATH startup
# mainly used for debugging
CONFIG_START_MENU="no"
## set to yes to start OS telnetd on port 2323
CONFIG_START_TELNETD="yes"
# note that you need to have SSHD keys
# generated and included in configuration
# for SSHD to work.
# Keys should be stored in
#/etc/ssh/ssh_host_key
#/etc/ssh/ssh_host_rsa_key
#/etc/ssh/ssh_host_dsa_key
#
# You may do this by adding them to /mnt/os/extra-profile
# settings tar.gz file
#
# generate them on Linux using:
#  ssh-keygen -q -t rsa1 -f /etc/ssh/ssh_host_key -C '' -N ''
#  ssh-keygen -q -t rsa -f /etc/ssh/ssh_host_rsa_key -C '' -N ''
#  ssh-keygen -q -t dsa -f /etc/ssh/ssh_host_dsa_key -C '' -N ''
# You may then create an extra-profile with them in it:
#  tar -C / -zcvf /mnt/os/extra-profile /etc/ssh/ssh_host_*
CONFIG_START_SSHD="no"
## set to yes to start NFS portmapper
CONFIG_START_PORTMAP="no"

## Set this to "yes" to start the IPMI over Lan daemon.
## Access parameters may then be adjusted in /etc/ipmi_lan.conf.
##
CONFIG_START_IPMILAN="no"

##
## Set to "no" to disable all network
## interfaces.
## Set to yes, to enable network configuration
## If set to no, no network interfaces will be configured
##
CONFIG_NETWORK_ENABLE="yes"

## T5307 default VLANs:
## eth0: RTM, VLAN 1, untagged, no IP address, managed by FASTPATH
## eth1: BI, VLAN 1, untagged, DHCP
## Default: no network interfaces

#CONFIG_NETWORK="ETH1 ETH1_4000 ETH1_4001 ETH1_4002 ETH1_4003"
CONFIG_NETWORK="ETH1"

CONFIG_ETH1_DEV="eth1"
```

```
CONFIG_ETH1_IP="dhcp"
CONFIG_ETH1_NETMASK=""
CONFIG_ETH1_BROADCAST=""
CONFIG_ETH1_VLAN_ID=""
CONFIG_ETH1_VCONFIG=""
CONFIG_ETH1_IFCONFIG=""

CONFIG_ETH1_4001_DEV="eth1.4001"
CONFIG_ETH1_4001_IP="dhcp"
CONFIG_ETH1_4001_NETMASK=""
CONFIG_ETH1_4001_BROADCAST=""
CONFIG_ETH1_4001_VLAN_ID="4001"
CONFIG_ETH1_4001_VCONFIG=""
CONFIG_ETH1_4001_IFCONFIG=""

CONFIG_ETH1_4002_DEV="eth1.4002"
CONFIG_ETH1_4002_IP="dhcp"
CONFIG_ETH1_4002_NETMASK=""
CONFIG_ETH1_4002_BROADCAST=""
CONFIG_ETH1_4002_VLAN_ID="4002"
CONFIG_ETH1_4002_VCONFIG=""
CONFIG_ETH1_4002_IFCONFIG=""

CONFIG_ETH1_4003_DEV="eth1.4003"
CONFIG_ETH1_4003_IP="dhcp"
CONFIG_ETH1_4003_NETMASK=""
CONFIG_ETH1_4003_BROADCAST=""
CONFIG_ETH1_4003_VLAN_ID="4003"
CONFIG_ETH1_4003_IFCONFIG=""

## set to DEBUG, TRACE, MINOR, MAJOR, CRITICAL
## for MCL_LOG generated messages
CONFIG_MCL_LOG_LEVEL="MINOR"
## set to yes to get MCL_LOG output on console as well
## otherwise it only goes to syslog
CONFIG_MCL_LOG_DEBUG_CONSOLE="yes"

# set to yes if FASTPATH shall drive pWD watchdog
# Otherwise, custom application may use pWD watchdog
# if this is yes, reload/reboot will do a graceful reboot
# otherwise, the fpmux/switchdrvr will just exit
# on reload/reset command
CONFIG_FASTPATH_WATCHDOG="yes"
# timeout in seconds for watchdog pWD
CONFIG_FASTPATH_WATCHDOG_TIMEOUT="5"
# update interval in seconds for watchdog pWD
CONFIG_FASTPATH_WATCHDOG_HEARTBEAT="1"

## if set to yes, pWD is enabled
CONFIG_WATCHDOG_PWD="yes"
## if set to yes, pOSWD is enabled
CONFIG_WATCHDOG_POSWD="yes"
## if set to YES include DHCP client ID in udhcpc queries
CONFIG_UDHCPC_CLIENTID="yes"
## this command is "eval"ed to get the client ID
## it must return a CLIENTID= string on stdout
CONFIG_UDHCPC_CLIENTID_COMMAND="/opt/kontron/bin/fru-query --dhcp-clientid"
## set to yes to enable script execution from UDHCPC
CONFIG_UDHCPC_SCRIPTEXEC="yes"
```

4.6.3.1 Enabling Telnet access for port 2323 (linux)

This setting allows to access the Carrier Linux shell by using telnet port 2323.

```
[...]
## set to yes to start OS telnetd on port 2323
CONFIG_START_TELNETD="yes"
[...]
```

4.6.3.2 Enabling SSH to access the Carrier

An SSH connection can be established to the Linux shell using the service port.

To use SSH, the keys must be generated and copied to the carrier in an extra-profile.tar.gz file and the feature must be enabled in the “current-settings” file.

```
[...]
# note that you need to have SSHD keys
# generated and included in configuration
# for SSHD to work.
# Keys should be stored in
#/etc/ssh/ssh_host_key
#/etc/ssh/ssh_host_rsa_key
#/etc/ssh/ssh_host_dsa_key
#
# You may do this by adding them to /mnt/os/extra-profile
# settings tar.gz file
#
# generate them on Linux using:
#  ssh-keygen -q -t rsa1 -f /etc/ssh/ssh_host_key -C '' -N ''
#  ssh-keygen -q -t rsa -f /etc/ssh/ssh_host_rsa_key -C '' -N ''
#  ssh-keygen -q -t dsa -f /etc/ssh/ssh_host_dsa_key -C '' -N ''
# You may then create an extra-profile with them in it:
#  tar -C / -zcvf /mnt/os/extra-profile /etc/ssh/ssh_host_*
CONFIG_START_SSHD="yes"
[...]
```

Chapter 5

Thermal Considerations

5. Thermal Considerations

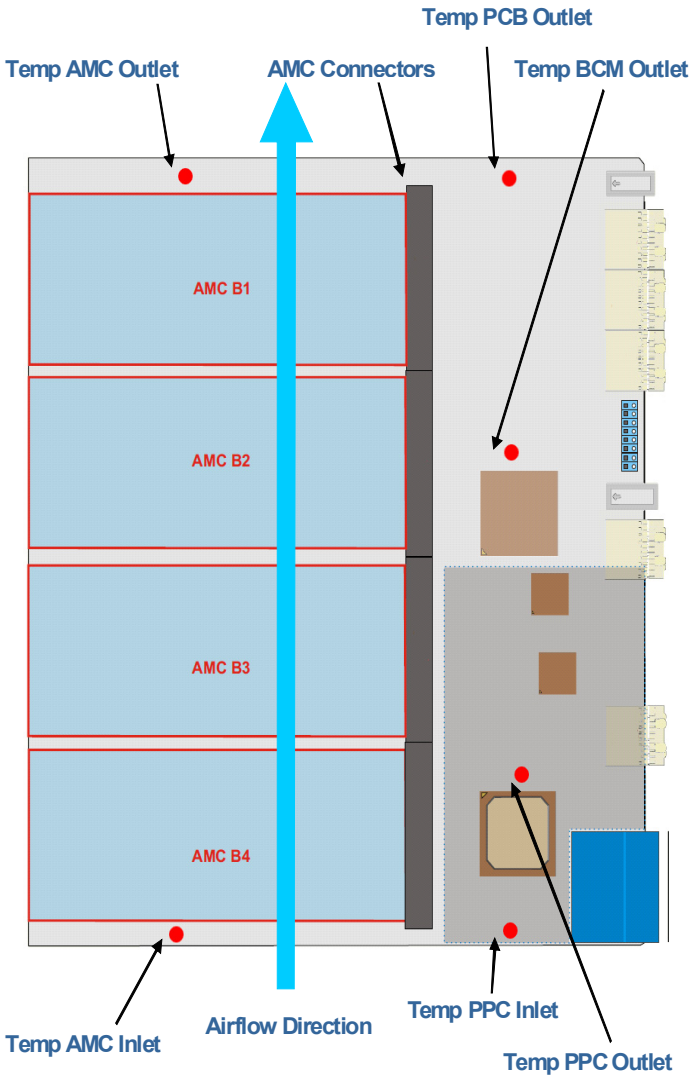
The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing AT8404 applications.

5.1 Thermal Monitoring

To ensure optimal operation and long-term reliability of the AT8404, all onboard components must remain within the maximum temperature specifications. The most critical components on the AT8404 are the Unit Computer and the Ethernet Switch. Additional sensors keep track of the inlet and outlet temperatures of the AMC area and the rear part of the board.

Operating the AT8404 or the AMCs in the AT8404 above the maximum operating limits may result in permanent damage to the board. To ensure functionality at the maximum temperature, the IPMC supports temperature monitoring features. Although temperature sensing information is made available to the IPMC, the AT8404 itself does not provide any active means of temperature regulation.

Figure 5-1: Temperature Sensor Locations (AT8404 Top View)



The following table shows the temperature thresholds of all sensors.

Table 5-1: Temperatur sensor thresholds

SENSOR Number / ID string	Lower Non-Recoverable	Lower critical	Lower non critical	Upper non critical	Upper critical	Upper Non-Recoverable
Temp PPC Inlet	-	- 40°C	0°C	+ 55°C	+ 70°C	+ 80°C
Temp PPC Outlet	-	- 40°C	0°C	+ 70°C	+ 85°C	+ 95°C
Temp AMC Inlet	-	- 40°C	0°C	+ 55°C	+ 70°C	+ 80°C
Temp AMC Outlet	-	- 40°C	0°C	+ 70°C	+ 85°C	+ 95°C
Temp PCB Outlet	-	- 40°C	0°C	+ 70°C	+ 85°C	+ 95°C
Temp BCM Outlet	-	- 40°C	0°C	+ 75°C	+ 90°C	+ 100°C

Temperature values are measured with an accuracy of 1°C.

5.2 Thermal Regulation

When developing applications using the AT8404, the system integrator must be aware of the overall system thermal requirements. A system chassis must be provided which satisfies these requirements.

Measurements proofed that operation in worst case conditions (maximum ambient temperature and power consumption including AMCs) is possible while all temperatures of on-board components stay below their critical thresholds. Note that the AMCs operated in the AT8404 have their own thermal and airflow requirements which have to be observed.

WARNING

As Kontron assumes no responsibility for any damage to the AT8404 or other equipment resulting from overheating any of the components, it is highly recommended that system integrators as well as end users confirm that the operational environment of the AT8404 complies with the thermal considerations set forth in this document.

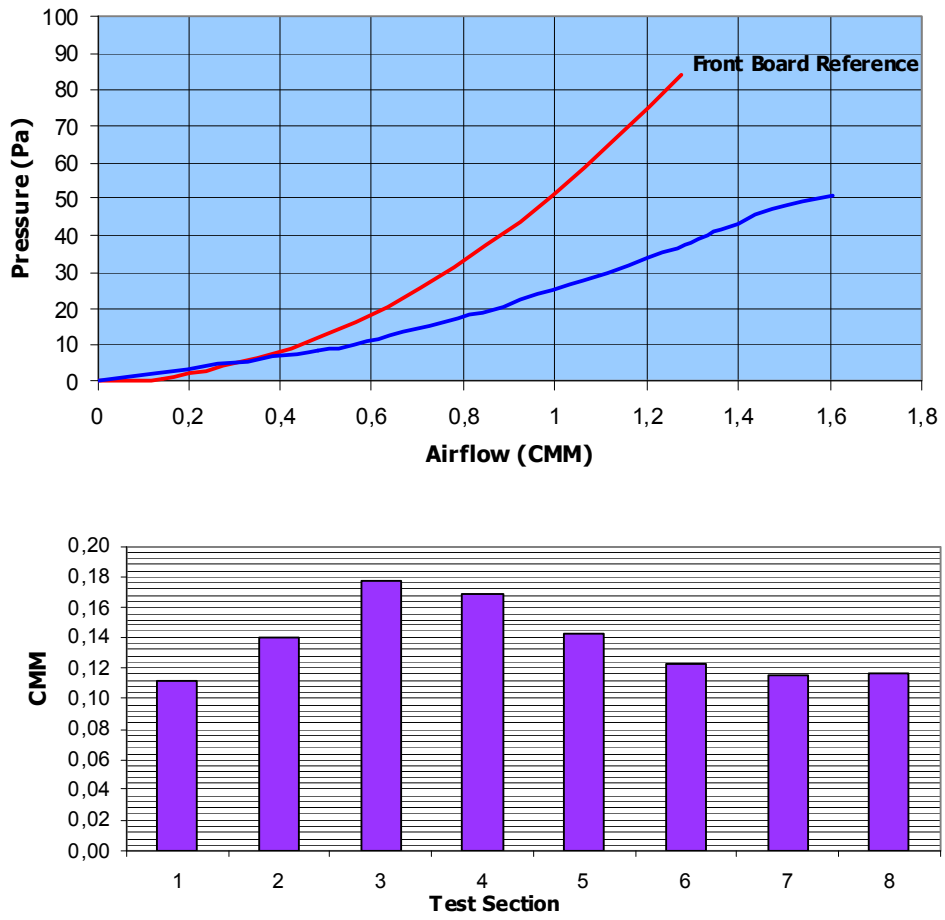
5.3 Airflow

In order to allow system integrators to optimize environmental conditions for the AMCs operated in the AT8404, airfow measurements according to CP-TA Interoperability Compliance Document (AdvancedTCA Book 1.1) were performed.

Two measurements were done with different AMC configurations. For each configuration, the pressure drop between inlet and outlet is measured (upper graph). The red curve represents an ATCA reference board as defined by the CP-TA. Another measurement shows the airflow distribution from the front panel to the back-plane connectors, separated into 8 sections. Sections 1 to 5 represent the AMC area between the front panel and the AMC connectors, while sections 6 to 8 represent the component area of the Carrier between the AMC connectors and the backplane connectors.

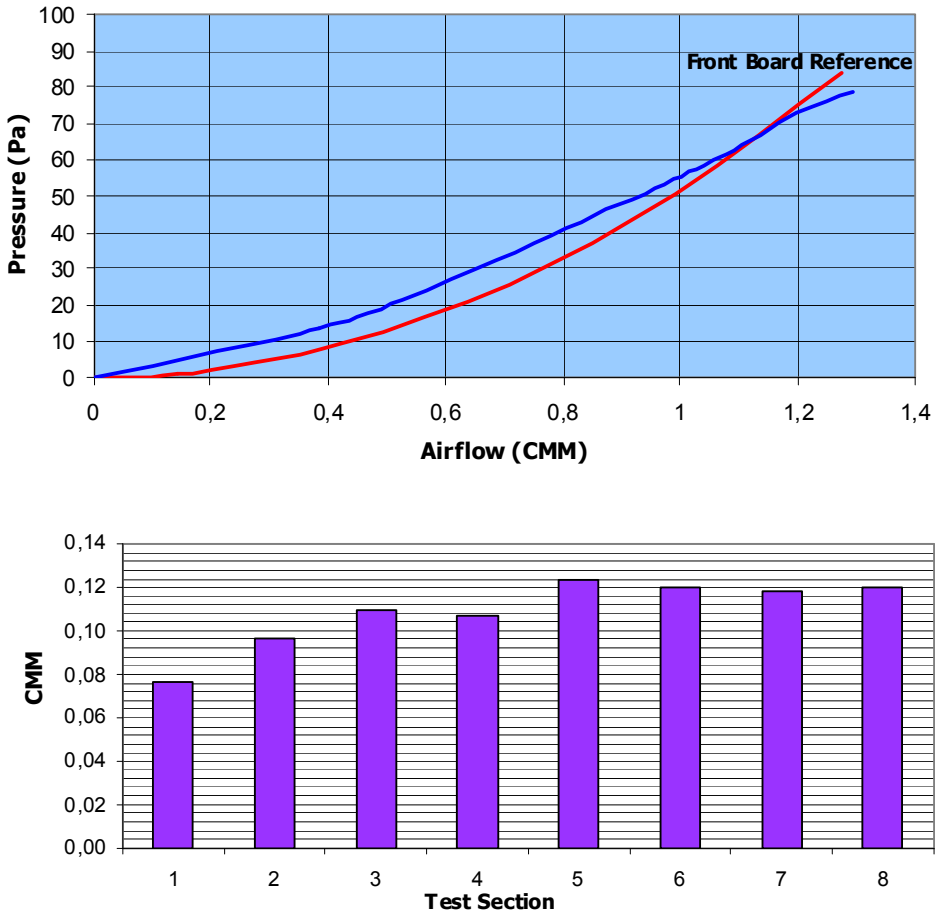
In configuration A, all four AMC slots are populated with blank fillers. These modules represent empty PCBs with front plate mechanics. This corresponds to the lowest possible air impedance.

Figure 5-2: Configuration A - Airflow Measurement



In configuration B, all four AMC slots are populated with air blocker modules. The air blockers simulate the maximum component envelope which is allowed on an AMC. This corresponds to the highest possible air impedance.

Figure 5-3: Configuration B - Airflow Measurement



The airflow through the AT8404 component area behind the AMC connectors is well balanced due to the impedance given by the power mezzanine. This prevents excessive air bypass when the AMC area is loaded with high impedance AMCs.

Partially stuffed AT8404 or AT8404 with low profile AMCs should use blank fillers or other means providing sufficient flow resistance to get close to the CP-TA impedance reference curve.

Appendix A

Getting Help

A. Getting Help

If, at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

North America	EMEA
Tel.: (450) 437-5682	Tel.: +49 (0) 8341 803 333
Fax: (450) 437-8053	Fax: +49 (0) 8341 803 339

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at:

North America: support@ca.kontron.com

EMEA: support-kom@kontron.com

Or at the following address:

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
4555 Ambroise-Lafortune	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7H 0A4 Canada	Germany

A.1 Returning Defective Merchandise

Before returning any merchandise please do one of the following:

- Call
  - Call our Technical Support department in North America at (450) 437-5682 or in EMEA at +49 (0) 8341 803 333. Make sure you have the following on hand: our Invoice #, your Purchase Order # and the Serial Number of the defective unit.
  - Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.
  - The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.
  - Make sure you receive an RMA # from our Technical Support before returning any merchandise.

- Fax
  - Send us a fax at: North America (450) 437-0304, EMEA +49 (0) 8341 803 339. In the fax, you must include your name, your company name, your address, your city, your postal/zip code, your phone number and your e-mail. You must also include the serial number of the defective product and a description of the problem.

- E-mail
  - Send us an e-mail at: RMA@ca.kontron.com in North America or at: orderprocessing@kontron-modular.com in EMEA. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the serial number of the defective product and a description of the problem.

A.2 When Returning a Unit

- In the box, you must include the name and telephone number of a person, in case further explanations are required. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**
- Ensure that the unit is properly packed. Pack it in a rigid cardboard box.
- Clearly write or mark the RMA number on the outside of the package you are returning.
- Ship prepaid. We take care of insuring incoming units.

North America	EMEA
Kontron Canada, Inc.	Kontron Modular Computers GmbH
4555 Ambroise-Lafortune	Sudetenstrasse 7
Boisbriand, Québec	87600 Kaufbeuren
J7H 0A4 Canada	Germany

Appendix B

Glossary

B. Glossary

Acronyms	Descriptions
ACPI	Advanced Configuration & Power Interface
AdvancedMC	(Same as AMC). Advanced Mezzanine Card.
AMC	(Same as AdvancedMC). Advanced Mezzanine Card.
AMC.0	Advanced Mezzanine Card Base Specification.
AMC.1	PCI Express and Advanced Switching on AdvancedMC. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
AMC.2	Ethernet Advanced Mezzanine Card Specification. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
AMC.3	Advanced Mezzanine Card Specification for Storage. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0).
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
ARP	Address Resolution Protocol
ASCII	American Standard Code for Information Interchange. ASCII codes represent text in computers, communications equipment, and other devices that work with text.
ATCA	Advanced Telecommunications Computing Architecture
BI	Base Interface. Backplane connectivity defined by the ATCA.
BMC	Base Management Controller
CLI	Command-Line Interface
CLK1	AdvancedTCA bused resource Synch clock group 1
CLK1A	AdvancedTCA bused resource Synch clock group 1, bus A
CLK1B	AdvancedTCA bused resource Synch clock group 1, bus A
CLK2	AdvancedTCA bused resource Synch clock group 2
CLK2A	AdvancedTCA bused resource Synch clock group 2, bus A
CLK2B	AdvancedTCA bused resource Synch clock group 2, bus B
CLK3	AdvancedTCA bused resource Synch clock group 3
CLK3A	AdvancedTCA bused resource Synch clock group 3 , bus A
CLK3B	AdvancedTCA bused resource Synch clock group 3 , bus B
CPLD	Complex Programmable Logic Device
CP-TA	Communications Platforms Trade Association
CRC	Cyclic Redundancy Check
CTS	Clear To Send
DDR2	(Same as DDR-II). DDR2 SDRAM or Double-Data-Rate two (2) Synchronous Dynamic Random Access Memory.
DHCP	Dynamic Host Configuration Protocol
DIMM	Dual In-line Memory Module
DIN	Deutsches Institut für Normung. German Institute for Standardization.
DMA	Direct Memory Access

Acronyms	Descriptions
DMI	Desktop Management Interface
DRAM	Dynamic Random Access Memory
DTC	Data Transfer Controller
DTR	Data Terminal Ready
DTS	Digital Thermal Sensor in IA32 processors.
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EISA	Extended Industry Standard Architecture. Superset of ISA, 32-bit bus architecture.
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
ESI	Enterprise South bridge Interface. Interface to the I/O legacy bridge component of the Intel ICHx.
ETH	Same as Ethernet.
ETSI	European Telecommunications Standards Institute
FI	Fabric Interface. Backplane connectivity defined by the ATCA.
FPGA	Field-Programmable Gate Array
FRU	Field Replaceable Unit. Any entity that can be replaced by a user in the field. Not all FRUs are hot swappable
FTP	File Transfer Protocol
FW	FirmWare
GARP	Generic Attribute Registration Protocol
Gb	Gigabit
GB	(Same as GByte) GigaByte.
GByte	(Same as GB) GigaByte.
GbE	Gigabit Ethernet
GHz	GigaHertz
GMRP	GARP Multicast Registration Protocol
GND	GrouND
GPIO	General Purpose Input Output
GUID	Globally Unique Identifier
GVRP	GARP VLAN Registration Protocol
HPM	PICMG Hardware Platform Management specification family
HPM.1	Hardware Platform Management IPM Controller Firmware Upgrade Specification
HW	HardWare
I2C	Inter Integrated Circuit bus
IO	(Same as I/O). Input Output
IOL	IPMI-Over-LAN
IP	Internet Protocolww.kontron.com
IPM	Intelligent Platform Management
IPMB	Intelligent Platform Management Bus

Acronyms	Descriptions
IPMB-0	Intelligent Platform Management Bus Channel 0, the logical aggregation of IPMB-A and IPMB-B.
IPMB-A	Intelligent Platform Management Bus A
IPMB-B	Intelligent Platform Management Bus B
IPMB-L	Intelligent Platform Management Bus Local
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
IPMIFWU	Intelligent Platform Management Interface FirmWare Update
IPv6	Internet Protocol version 6
IRQ	Interrupt ReQuest
ISO	International Organization for Standardization
ITU	International Telecommunication Union
ITU-T	ITU Telecommunication standardization sector. ITU is International Telecommunication Union.
JTAG	Joint Test Action Group
KB	KiloByte
KHz	KiloHertz
LAN	Local Area Network
LBC	Local Bus Controller (On PowerQuicc III CPU)
LED	Light-Emitting Diode
LSB	Least Significant Byte
LUN	Logical Unit Number
MAC	Media Access Controller address of a computer networking device.
MB	MegaByte
MC	Management Controller
MCH	Memory Controller Hub
MDI	Medium Dependent Interface. MDI port or uplink port.
MHz	MegaHertz
MMC	Module Management Controller. MMCs are linked to the IPMC.
MMIO	Memory-Mapped IOw.kontron.com
MTBF	Mean Time Between Failures
NAND	Type of Flash Memory, used for mass storage.
NDA	Non-Disclosure Agreement
NEBS	Network Equipment-Building System
OEM	Original Equipment Manufacturer
OOS	Out Of Service
OS	Operating System
OSI	Open Source Initiative
PCB	Printed Circuit Board
PCIe	(Same as PCI-E). PCI-Express. Next generation I/O standard
PCI-E	(Same as PCIe). PCI-Express. Next generation I/O standard.

Acronyms	Descriptions
PHY	PHYsical layer. Generic electronics term referring to a special electronic integrated circuit or functional block of a circuit that takes care of encoding and decoding between a pure digital domain (on-off) and a modulation in the analog domain.
PICMG	PCI Industrial Computer Manufacturers Group
PICMG®	PCI Industrial Computer Manufacturers Group
PLD	Programmable Logic Device
PLL	Phase Lock Loop
PNE	Platform for Network Equipment. A Carrier Grade Linux (4.0) platform.
POR	Power-On Reset
POST	Power-On Self-Test
RAM	Random Access Memory
RHEL	Red Hat Enterprise Linux
RoHS	Restriction of the Use of Certain Hazardous Substances
ROM	Read Only Memory. Also refers to option ROM or expansion ROM code used during POST to provide services for specific controllers, such as boot capabilities.
RS-232	(Same as RS232). Recommended Standard 232.
RS232	(Same as RS-232). Recommended Standard 232.
RTC	Real Time Clock
RTM	Rear Transition Module
RTS	Request To Send
SCL	Serial CLock
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SEEPROM	Serial EEPROM
SEL	System Event Log
SERDES	SERializer/DESerializer. Pair of functional blocks commonly used in high speed communications. These blocks convert data between serial data and parallel interfaces in each direction.
SSGMII	Serial Gigabit Media Independent Interface. Standard interface used to connect a Gigabit Ethernet MAC-block to a PHY.
ShMC	Shelf Management Controller
SMB	(Same as SMBus/SMBUS). System Management Bus.
SOL	Serial Over LAN
SONET	Synchronous Optical NETworking
SPI	Serial Peripheral Interface
SSH	Secure SHell. A network protocol that allows data to be exchanged over a secure channel between two computers.
TCLKA	Telecom CLocK A. AMC Clock Interface.
TCLKB	Telecom CLocK B. AMC Clock Interface.
TCLKC	Telecom CLocK C. AMC Clock Interface.
TCLKD	Telecom CLocK D. AMC Clock Interface.
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter

Acronyms	Descriptions
USB	Universal Serial Bus
VLAN	Virtual Local Area Network
WD	WatchDog
WDT	WatchDog Timer