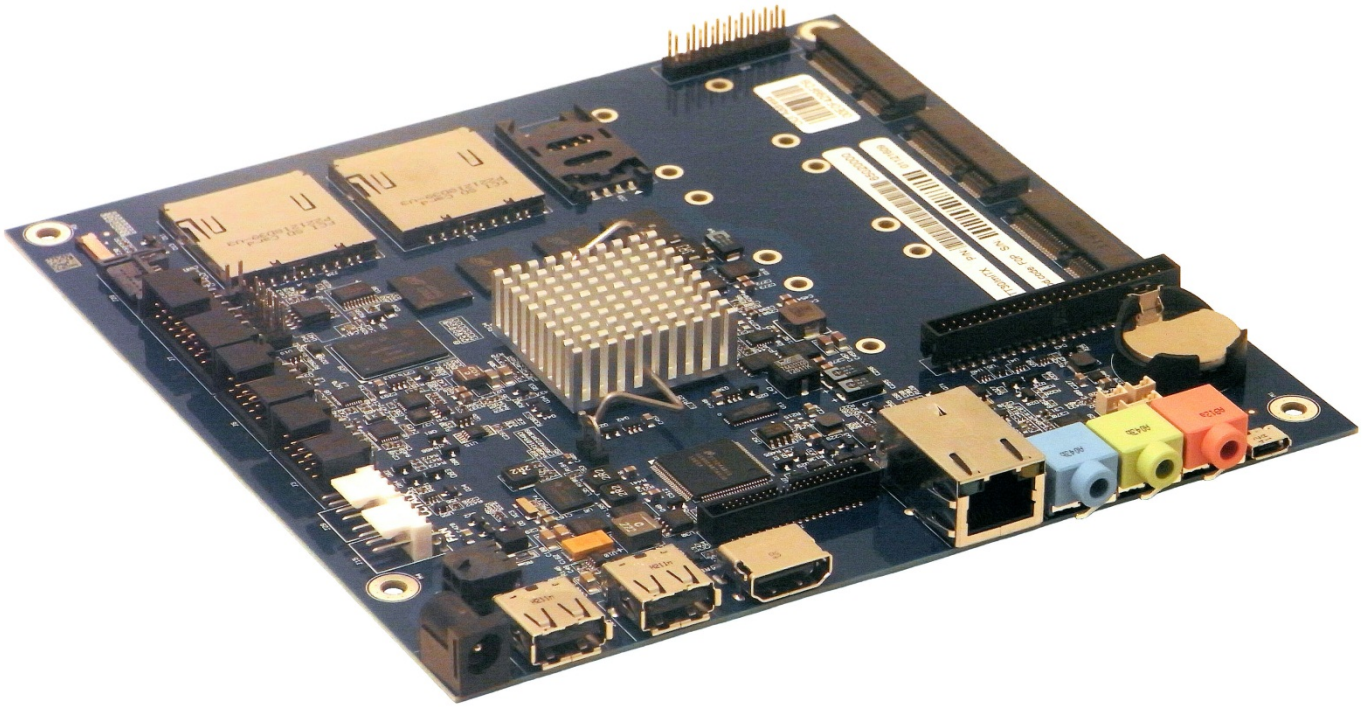
kontron

» Kontron User's Guide «



KTT30/mITX

KTD-N0857-B

The pulse of innovation

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Document Revision History

Revision	Date	By	Comment
B	28-10-2013	MLA	Fan Connector description corrected. Modem card connector description corrected. Front Panel cable kit corrected. Added cable kit info. J37 moved and chapter 4 modified.
A	9-4-2013	MLA	Digital Serial Interface information completely removed.
0	17-12-2012	MHU/MLA	Preliminary version

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- CPU Board
  1. Type.
  2. Part Number (find PN on label)
  3. Serial Number if available (find SN on label)
- Configuration
  1. CPU Type and Clock speed
  2. DRAM Type and Size.
  3. BIOS Revision (find the version info in the BIOS Setup).
  4. BIOS Settings different than *Default* Settings (refer to the BIOS Setup section).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-Rom, LCD Panels etc.

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2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.

1 Introduction

This manual describes the KTT30/mITX board made by KONTRON Technology A/S. This board will also be denoted KTT30 within this Users Guide.

The KTT30 board is based on the NVIDIA® Tegra® 3 Mobile Processor. See the chapter 'Specifications' for more specific details.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

2 Installation Procedure

2.1 Installing the Board

To get the board running follow these steps.

1. **Turn off the PSU (Power Supply Unit)**

Warning: Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power connectors unconnected while configuring the board. Otherwise components (RAM, LAN controller, SPI flash or others) might get damaged.

2. **Connecting Interfaces**
   Insert all external cables for a storage media, a keyboard or others. A serial connection to a desktop PC must be established in order to be able to change Setup settings.

3. **Connect and turn on PSU**
   Connect the PSU to the board and turn it on.

4. **Power Button**
   The PWRBTN pins must be shortened to start the board; this is done by pin 10 (PWRBTN+) and pin 12 (PWRBTN-) on the FRONTPNL connector J7 (see chapter 'Power Supply').

5. **Mounting the board to chassis**
   When fixing the Motherboard on a chassis it is recommended using screws with integrated washer and having diameter of approx. 7mm.

Warning: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.
Do not use washers with teeth as they can damage the PCB and may cause short circuits.

2.2 Requirements IEC60950

Users of KTT30 should take care when designing chassis interface connectors in order to fulfil the IEC60950 standard.

When an interface or connector has a VCC (or other power) pin which is directly connected to a power plane like the VCC plane:
To protect the external power lines of the peripheral devices the customer has to take care about:

- That the wires have suitable rating to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC60950.

Lithium battery precautions

CAUTION! Danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instructions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.
ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie. Remplacement seulement par le même ou un type équivalent recommandé par le producteur. L'évacuation des batteries usagées conformément à des indications du fabricant.	**PRECAUCION!** Peligro de explosión si la batería se sustituye incorrectamente. Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante. Disponga las baterías usadas según las instrucciones del fabricante.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL!** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING! Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS!** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan lalteval-mistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

3 Specifications

3.1 Functional Specifications

System on Chip (SoC): NVIDIA® Tegra® 3

- Quad Cortex-A9 multi-processing ARM® cores up to 1.3 GHz core frequency
- ARMv7 instruction set
- 32 kB data and 32 kB instruction L1 cache per core
- Shared 1 MB L2 cache
- DDR3 memory interface up to DDR3L-1600 with maximum size of 2 GB
- SPI™ flash controller
- Three USB ports (EHCI) with one client interface
- Audio-Video Processor (AVP, GeForce® GPU) with a dual display controller
- Two integrated audio controllers (PCM and Inter-IC Sound, called IIS or I^2S)
- One Secure Digital / MultiMedia Card (SD/MMC) controller with four instances
- Three PCI Express® ports (only single lane configuration)
- One S-ATA® 2.0 port
- Some pins are useable as GPIOs (max. 18 x 3.3V) or as special function pins (e.g. keyboard)
- Five UARTs with 16450/550 compatible mode (only two UARTs available)

Onchip SPI™ Flash Controller

- Supports FIFO and DMA mode access
- Maximum transfer rate of 35 Mbps

Onchip Universal Serial Bus (USB)

- All ports are capable to handle USB 2.0 (EHCI)
- One port alternatively supports USB client functionality
- Supports USB 1.1 low and full speed devices without a companion USB 1.1 host controller

Onchip Graphics Processing Unit (GPU)

- Ultra low power GPU up to 520 MHz internal clock and 12 cores
- Two independent display controllers support 2D/3D graphics rendering
- 1080p Video Encode Processor to deliver full HD video streams
- OpenGL® ES 2.0 support
- HDMI® V1.4a interface (max. 1920x1080 pixels)
- Low Voltage Differential Signaling (LVDS) flatpanel interface supports 18/24 bit color depth with a maximal resolution of 1920x1200 pixels
- Full hardware acceleration of video decode standards (extract): H.264, MPEG4 and VC1

Onchip Audio Subsystem

- Codec interface realize the Inter-IC Sound (I^2S) specification
- The audio codec supports a maximal resolution of 24 bit with 96 kHz sample rate
- Three audio jacks for Line-in, Line-out and Microphone-in
- S/PDIF input and output as well as a Headphone interface

Onchip SD/MMC Controller

- Two ports up to 4 bit data bus width (available on connectors) and one onboard port with 8 bit data width (16 GByte Sandisk NAND flash, bootable)
- Supports FIFO and DMA mode access
- Supports SDMEM/SDIO specification V3.0 up to 50/25 MHz interface speed
- Supports MMC specification V4.4 up to 52 MHz interface speed
- Supports CE-ATA® Digital Protocol specification V1.1 up to 52 MHz interface speed
- Supports e.MMC devices

Onchip PCI Express® Controller

- Three ports with maximum data rate of 2.5 GT/s, one port is used for the onboard LAN controller
- All ports only support one lane (PCIe x1)
- One miniPCI Express® connector (mPCIe signals, no mSATA or USB signals)
- One miniPCI Express® connector (mPCIe or mSATA signals, no USB signals - switchable per software)

Onchip S-ATA® Controller

- Supports S-ATA® specification V2.0 and AHCI V1.3

Onchip Serial Ports (UARTs)

- One RS232C compatible port with CTS and RTS status lines also useable as ccTalk interface
- One RS232C compatible port with all status lines

Gigabit LAN (PCI Express® connection): Intel® 82574L

- Full duplex operation at 10/100/1000 Mbps
- Fully compliant with IEEE® 802.3, IEEE® 802.3u and IEEE® 802.3ab

Temperature Monitoring (I^2C^{TM} connection): ON Semiconductor® ADT7461A

- One onchip thermal sensor and one remote temperature sensor (from SoC)

Motion Processing Unit (I^2C^{TM} connection): InvenSense® MPU-3050™

- Embedded tri-axis gyroscope
- Digital Motion Processor™ (DMP) accelerator engine with a second I^2C^{TM} port for third party accelerometers

Digital Accelerometer (I^2C^{TM} connection): Kionix® KXTF9-4100

- Tri-axis ±2g, ±4g or ±8g accelerometer

Additional Features

- Serial Atmel® touch screen interface (I^2C^{TM})
- Up to 18 GPIOs on a Feature connector
- USB modem card interface with SIM card socket
- One SPI™ interface (3.3V) on a pin header
- An optional 4-wire processor fan

Operating System Support

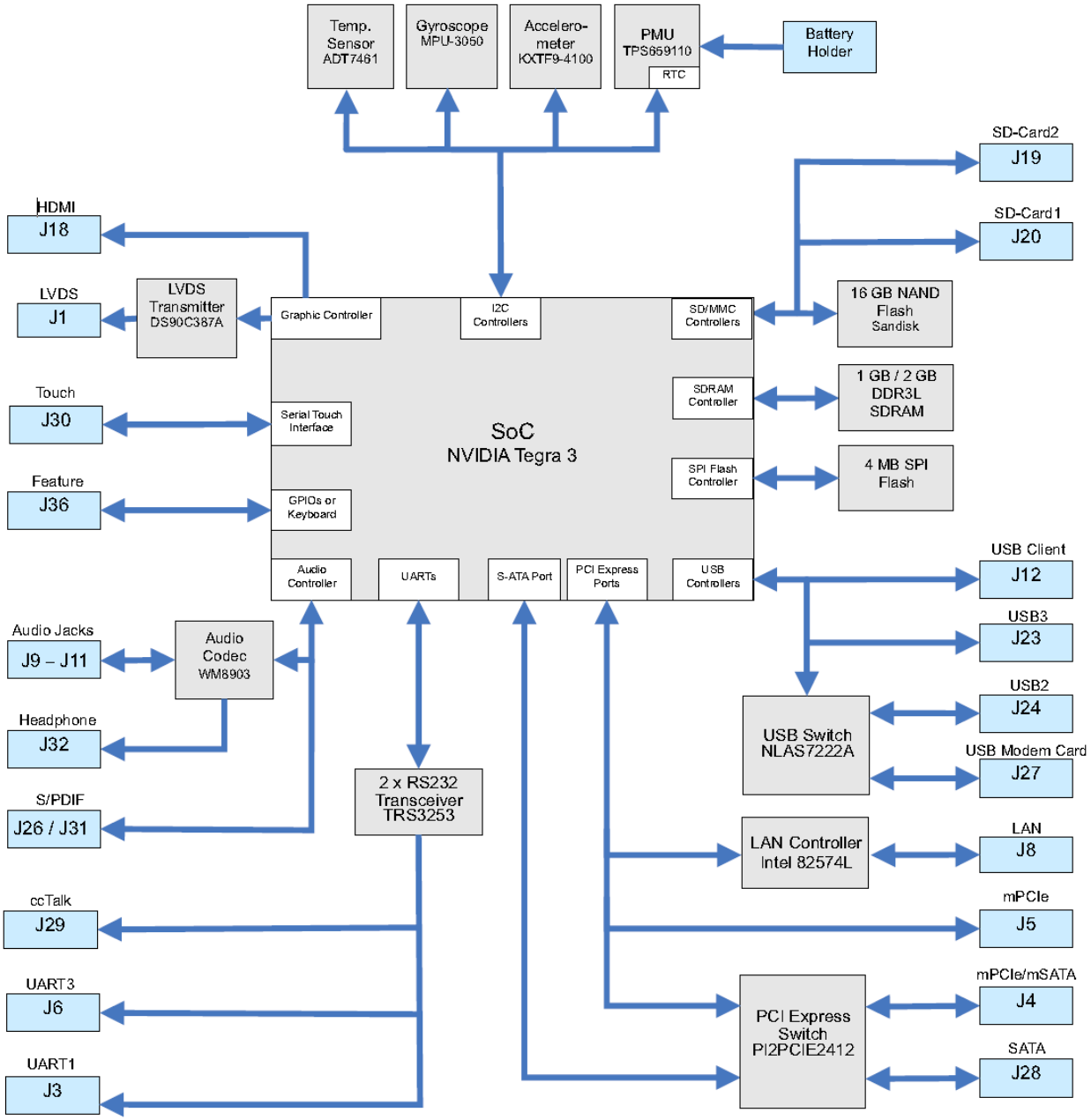
- Linux® (kernel version 3.1)
- Android® (kernel version 4.0)
- Windows® Embedded Compact 7

Battery

- Exchangeable 3.0V Lithium battery for the Real-Time-Clock (RTC)
- Manufacturer Panasonic® (part number CR2032L/BN, CR2032N/BN or CR2032L/BE)

CAUTION!
Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

3.2 KTT30 Block Diagram



3.3 Mechanical Specifications

Dimensions

- miniITX™ form factor 170.2 x 170.2 mm ±0.2 mm (with all connectors 174 x 170.2 mm)
- Height approx. 17.5 mm

3.4 Electrical Specifications

Supply Voltage

- +5V ±10% DC

Supply Current (Linux®)

The power consumption test uses a tool to stress the CPU (100% load) and at the same time another tool to generate a high graphic throughput. The boards were tested with a HDMI®/DVI® monitor, USB keyboard & mouse and the onboard SanDisk® 16 GByte embedded flash drive as boot device.

Full Load		Idle		Deep Sleep	
[A]	[W]	[A]	[W]	[A]	[W]
tbd.	**tbd.**	**tbd.**	**tbd.**	**tbd.**	**tbd.**

3.5 Environmental Specifications

Temperature

Operating:

- Ambient temperature: 0 to +60°C [1)]

Non operating (storage):

- Ambient temperature: -20 to +70°C [2)]

Note: *1) It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.*
2) Lower limit of storage temperature is defined by specification restriction of the onboard Lithium battery. A board with battery has been verified for storage temperature down to -40°C by KONTRON.

Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

Electromagnetic Compatibility (ESD/EMI)

All peripheral interfaces intended for connection to external equipment are ESD/EMI protected.

- EN 61000-4-2:2000 ESD Immunity
- EN55022:1998 class B Generic Emission Standard

Theoretical MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is 'method 1 case 1'. In that particular method the components are assumed to be operating at a 50% stress level in a 40°C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50°C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40°C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) cause lower MTBF values.

- System MTBF (hours): tbd.

Note: *Fans usually shipped with KONTRON Technology A/S products have 50.000-hour typical operating life. The above estimation assumes no fan but a passive heat sinking arrangement. Estimated RTC battery life (as opposed to battery failures) is not included in the MTBF calculation. The RTC battery lifetime has to be considered separately. Battery life depends on both temperature and operating conditions. When the KONTRON unit has external power; the only battery drain is from leakage paths.*

Restriction of Hazardous Substances (RoHS)

All boards in the KTT30 family are RoHS compliant.

4 Debug/Design Tools

In order to change software features, to repair a corrupted bootloader or for service purpose, the two connectors UART3 (J3) Serial port and USB Client (J12) are used.

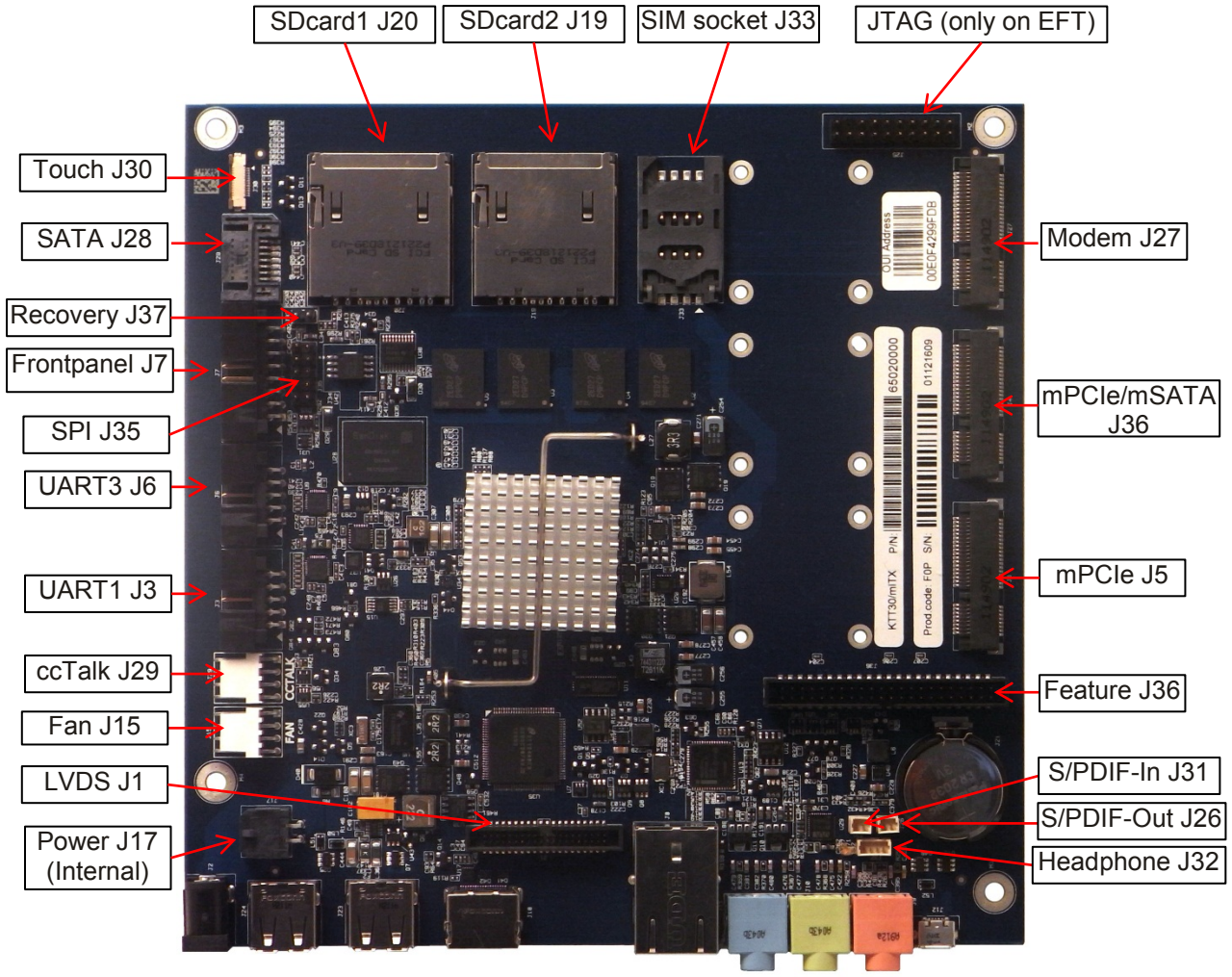
If the board does not boot up or in the case of custom firmware usage (for example the replacement of the KONTRON bootloader) you can overwrite the content of the SPI™ flash. The following parts are necessary:

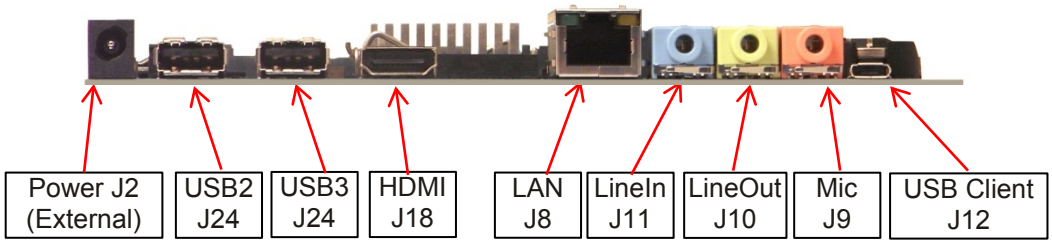
- A desktop PC with a Windows® or Linux® operating system
- A special NVIDIA® USB driver (only Windows®)
- One standard USB cable (Type A plug to micro-B plug)
- Two pushbuttons or one pushbutton and one jumper or something similar
- An actual bootloader image file

For the next step you should create a link from the KTT30 client port to a desktop PC with the standard USB cable. Make sure that you have the power cable plugged-in. Then connect the pushbuttons or a push-button/jumper combination to the pin header J37 (button or jumper) and the Front Panel Header J7 (button).

To set the board into recovery mode, first the pushbutton J37 (if you use two buttons) and then the pushbutton J7 must be pressed until the LEDs go on.
Install the special USB driver on the desktop PC (if not already done). Open the device manager to control the driver activity. After some seconds you must see the entry **USB Client Port Driver (CPD)**. The last step includes the download of the bootloader image file with NVIDIAs® NVFLASH tool. For further details see the 'KTT30/mITX Software Guide' chapter 'NVFLASH Download Tool'.

5 Connectors Location





6 Connector Signal Definitions

The following sections provide pin definitions and detailed description of all onboard connectors.
The connector definitions follow the following notation:

Column Name	Description
Pin	Shows the pin numbers in the connector.
Signal	The mnemonic name of the signal at the current pin. The notation "#" states that the signal is active low.
Type	AI: Analogue Input AO: Analogue Output I: Digital Input IO: Digital Input / Output IOD: Input / Open Drain output O: Digital Output DSO: Differential Signaling Output with complementary signals on two paired wires DSI: Differential Signaling Input with complementary signals on two paired wires DSIO: Differential Signaling Input / Output (combined DSO and DSI) PWR: PoWeR supply or ground reference pins NC: Pin Not Connected Additional notations: -5.0 +5.0V signal voltage level, e.g. I-5.0 -3.3 +3.3V signal voltage level, e.g. O-3.3 -1.8 +1.8V signal voltage level, e.g. IO-1.8
Ioh/Iol	Ioh: Typical current in mA flowing out of an output pin through a grounded load while the output voltage has high level. Iol: Typical current in mA flowing into an output pin from a VCC connected load while the output voltage has low level.

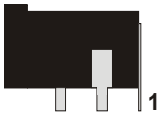
The abbreviation **tbd** is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

7 Rear IO Connectors

7.1 DC Power Connector

The KTT30/mITX board has a power input voltage range from +4.5V to +5.5V. All other voltages are generated onboard (e.g. +3.3V / +1.8V system voltage).

The power supply is supplied via the connector J2 (3 pins, DC power jacket 2.1mm).

Header	Pin	Signal	Description
	1	**VCC5** 1)	Power supply +5V
	2	**GND**	Ground
	3	**GND**	Ground

Alternative through the internal Power connector J17 (4 pin Micro-Fit). Notice that the +5V power lines on J2 and on J17 are connected on the board.

Note: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

7.2 USB Connectors (Standard USB2.0)

The USB interface comes with three USB ports which follow the EHCI specification (USB 2.0 compliant). You can expand the amount of USB connections by adding external hubs. Two ports are available on a standard connector and one (client) port on a micro USB connector. All ports support USB 1.1 low and full speed devices without a companion USB 1.1 host controller.

Two USB ports are available through the standard USB connectors J23 and J24.

Header	Pin	Signal	Description	Type
	1	**VCC5** 1)	Power +5V	PWR
	2	**USB-**	USB port (negative)	DSIO-3.3
	3	**USB+**	USB port (positive)	DSIO-3.3
	4	**GND**	Ground	PWR

Notes: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

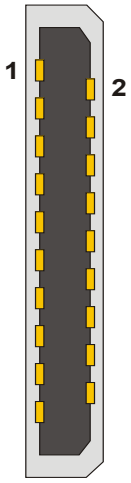
The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 500mA. Do not supply external USB devices with higher power dissipation through these pins

7.3 HDMI® Connector

Graphics Processing Unit

The graphics accelerator supports a HDMI® interface with Full HD resolution, a variety of LVDS LCD panels with double clock, color depths of 18/24 bit and resolutions up to 1920 x 1200 pixels.

The HDMI® interface is available through the standard 19 pin Type A HDMI® connector J18.

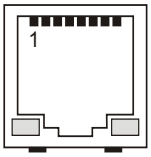
Header	Pin	Signal	Description	Type
	1	**TMDS2+**	TMDS data 2 (positive)	DSO-3.3
	2	**GND**	Ground	PWR
	3	**TMDS2-**	TMDS data 2 (negative)	DSO-3.3
	4	**TMDS1+**	TMDS data 1 (positive)	DSO-3.3
	5	**GND**	Ground	PWR
	6	**TMDS1-**	TMDS data 1 (negative)	DSO-3.3
	7	**TMDS0+**	TMDS data 0 (positive)	DSO-3.3
	8	**GND**	Ground	PWR
	9	**TMDS0-**	TMDS data 0 (negative)	DSO-3.3
	10	**TMDS_CLK+**	TMDS clock (positive)	DSO-3.3
	11	**GND**	Ground	PWR
	12	**TMDS_CLK-**	TMDS clock (negative)	DSO-3.3
	13	**CEC**	Consumer Electronics Control	IO-5.0
	14	**N.C.**	Not connected	NC
	15	**DDC_CLK**	DDC clock	IO-5.0
	16	**DDC_DATA**	DDC data	IO-5.0
	17	**GND**	Ground	PWR
	18	**VCC5** [1)]	Power +5V	PWR
	19	**TMDS_HPD**	Hotplug detect	I-5.0

Note: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

7.4 LAN Connector

The KTT30 uses an Intel® 82574 Gigabit PCI Express® LAN controller which supports 10/100/1000 Base-T interfaces. The controller auto-negotiates the management of a 10, 100 or 1000 Mbps connection. Additionally you can boot up the board via a network connection from a PXE server.

The LAN interface is available through the standard RJ45 connector J8 (8 pins).

Header	Pin	Signal	Description	Type
	1	**TXD+ / MDI01+**	10/100 transmit / 1000 pair 1 (positive)	DSO / DSIO
	2	**TXD- / MDI01-**	10/100 transmit / 1000 pair 1 (negative)	DSO / DSIO
	3	**RXD+ / MDIO2+**	10/100 receive / 1000 pair 2 (positive)	DSI / DSIO
	4	**MDIO3+**	1000 pair 3 (positive)	DSIO
	5	**MDIO3-**	1000 pair 3 (negative)	DSIO
	6	**RXD- / MDIO2-**	10/100 receive / 1000 pair 2 (negative)	DSI / DSIO
	7	**MDIO4+**	1000 pair 4 (positive)	DSIO
	8	**MDIO4-**	1000 pair 4 (negative)	DSIO

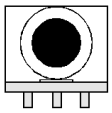
7.5 Audio Interface

The SoC supports an Inter-IC Sound (I^2S) codec with 24 bit resolution and 96 kHz sample rate (the maximum rate of 96 kHz only unidirectional). The analogue-to-digital part of the codec uses 24 bit, 128x oversampled sigma-delta ADCs. The digital-to-analogue part contains two 24 bit sigma-delta DACs. The interface includes LINE OUT, LINE IN, MICROPHONE IN and a digital S/PDIF output.

Parameter	Values	Units
Output resolution (LINE OUT, S/PDIF)	16/20/24	bit
Output sample rate (LINE OUT, S/PDIF)	44.1/48/96	kHz
Output signal-to-noise ratio (LINE OUT)	96	dB
Input resolution (LINE IN)	16/20/24	bit
Input sample rate (LINE IN)	44.1/48/96	kHz
Input signal-to-noise ratio (LINE IN)	92	dB

7.6 Analog Connectors

The analog audio interface uses three TRS (Tip, Ring, Sleeve) connectors J9 to J11 (3 pins).

Header	Pin	J11 BLUE	J10 LIME	J9 PINK	Type
	Tip	**LINEIN-L**	**LINEOUT-L**	**MIC-L**	IA resp. OA (J10)
	Ring	**LINEIN-R**	**LINEOUT-R**	**MIC-R**	IA resp. OA (J10)
	Sleeve	**GND**	**GND**	**GND**	PWR

7.7 Micro USB Connector

The connector J12 (5 pins) provides the USB Client functionality (default setting).

You need the client functionality for changing the bootloader or update a corrupted bootloader. Together with the recovery pin (see chapter “Debug/Design Tools”) and dedicated software on a desktop computer as well as a standard USB cable the upload.

Header	Pin	Signal	Description	Type
	1	**VCC5** 1)	Power +5V	PWR
	2	**USB-**	USB port (negative)	DSIO-3.3
	3	**USB+**	USB port (positive)	DSIO-3.3
	4	**ID**	Host / slave detection (grounded or opened)	I
	5	**GND**	Ground	PWR

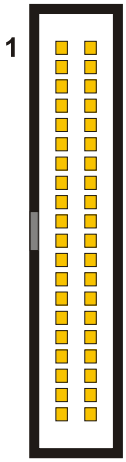
Notes: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 500mA. Do not supply external USB devices with higher power dissipation through these pins

8 Pin Connectors

8.1 LVDS Flat Panel Connector

The J1 connector (40 pins) provides the LVDS interface for flat panels on the top side of the board.

Header	Pin	Signal	Description	Type
	1 - 5	**VCC5** [1)]	Power +5V	PWR
	6	**GND**	Ground	PWR
	7	**VCC5** [1)]	Power +5V	PWR
	8	**GND**	Ground	PWR
	9 - 10	**LCDVCC** [1)]	Panel power +3.3V or +5V	PWR
	11	**DDC_CLK**	DDC clock	IO-3.3
	12	**DDC_DATA**	DDC data	IO-3.3
	13	**BKLTADJ**	Brightness control	PWM-3.3
	14	**VCCENABLE**	Panel power enable	O-3.3
	15	**BKLTON**	Backlight on/off	O-3.3
	16	**GND**	Ground	PWR
	17	**LVDSA0-**	First channel data 0 output (negative)	DSO-3.3
	18	**LVDSA0+**	First channel data 0 output (positive)	DSO-3.3
	19	**LVDSA1-**	First channel data 1 output (negative)	DSO-3.3
	20	**LVDSA1+**	First channel data 1 output (positive)	DSO-3.3
	21	**LVDSA2-**	First channel data 2 output (negative)	DSO-3.3
	22	**LVDSA2+**	First channel data 2 output (positive)	DSO-3.3
	23	**LVDSAC-**	First channel clock output (negative)	DSO-3.3
	24	**LVDSAC+**	First channel clock output (positive)	DSO-3.3
	25	**LVDSA3-**	First channel data 3 output (negative)	DSO-3.3
	26	**LVDSA3+**	First channel data 3 output (positive)	DSO-3.3
	27 - 28	**GND**	Ground	PWR
	29	**LVDSB0-**	Second channel data 0 output (negative)	DSO-3.3
	30	**LVDSB0+**	Second channel data 0 output (positive)	DSO-3.3
	31	**LVDSB1-**	Second channel data 1 output (negative)	DSO-3.3
	32	**LVDSB1+**	Second channel data 1 output (positive)	DSO-3.3
	33	**LVDSB2-**	Second channel data 2 output (negative)	DSO-3.3
	34	**LVDSB2+**	Second channel data 2 output (positive)	DSO-3.3
	35	**LVDSBC-**	Second channel clock output (negative)	DSO-3.3
	36	**LVDSBC+**	Second channel clock output (positive)	DSO-3.3
	37	**LVDSB3-**	Second channel data 3 output (negative)	DSO-3.3
	38	**LVDSB3+**	Second channel data 3 output (positive)	DSO-3.3
	39 - 40	**GND**	Ground	PWR

Note: The backlight adjust signal uses the Pulse Width Modulation (PWM) technique. A proto- type cable with open ends is shippable from KONTRON (part number 821515).

Note: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

Warning: *Check the U-Boot Setup for correct settings for your panel – not doing so might cause permanent damage to your panel.*

Connecting a Flat Panel

❶ Check if you have the correct panel cable. Inspect the cable for damages.

❷ Switch on the power supply and activate/save the desired settings with help of the U-Boot bootloader (for further details see the 'Software Guide' chapter 'U-Boot Setup'). Switch off the power supply.

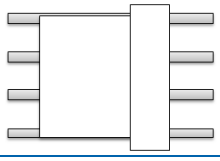
❸ Connect an external power supply for the correct backlight voltage (except the power supply complies with the backlight voltage).

❹ Connect the cable to the flat panel connector J1 on the KTT30 and connect the other end to your display.

❺ Switch on the power supply. If you only see a blank screen contact your distributor for technical support.

8.2 Fan Connector

For an optional fan use the connector J15 (4 pins). The interface only supports +5V fans and operates with a PWM output (Control) which allows the control of fan speed.

Header	Pin	Signal	Description	Type
1 	1	**Control**	PWM output	0-5.0
	2	**Sence**	Tacho signal (open drain)	I
	3	**VCC5** [1)]	Power +5V	PWR
	4	**GND**	Ground	PWR

Note: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

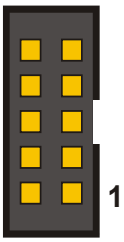
Warning: Do not mix the Fan Connector and the ccTalk connector. If mounting Fan into ccTalk connector Fan might be damaged.

8.3 COM ports (RS232)

Two serial ports provide asynchronous serial communication with RS-232 interfaces. They are 16450/16550 UART compatible and support 16-byte FIFO buffers for transfer rates from 50 Baud to 115.2 kBaud. UARTC/UART3 can be configured as a standard serial or as a ccTalk interface. With a solder jumper it is possible to activate the ccTalk interface, often used in automatic payment equipment.
Connector assignment:

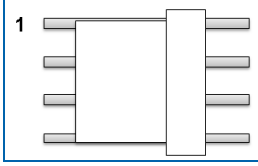
J3 → **UARTA**/UART1
J6 → **UARTC**/UART3

The serial ports are available through the connectors J3 and J6 (10 pins).

Header	Pin	Signal	J3	J6	Description	Type
	1	**DCD#**	✔		Data carrier detect	I
	2	**DSR#**	✔		Data set ready	I
	3	**RXD**	✔	✔	Receive serial data	I
	4	**RTS#**	✔	✔	Request to send	O
	5	**TXD**	✔	✔	Transmit serial data	O
	6	**CTS#**	✔	✔	Clear to send	I
	7	**DTR#**	✔		Data terminal ready	O
	8	**RI#**	✔		Ring indicator	I
	9	**GND**	✔	✔	Ground	PWR
	10	**VCC5** 1) 2)	✔	✔	Power +5V	PWR

8.4 ccTalk Connector

The ccTalk interface uses the fan connector J29 (4 pins).

Header	Pin	Signal	Description	Type
	1	**VCC5** 1)	Power +5V	PWR
	2	**N.C.**	Not connected	NC
	3	**GND**	Ground	PWR
	4	**DATA**	Serial data line (RXD/TXD)	IO

Notes: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.
2) The +5V supply voltage is protected with a common 1.5A resetable fuse.

Warning: Do not mix the ccTalk Connector with the Fan Connector. If mounting ccTalk device into Fan Connector then ccTalk device and or mother board might be damaged.

8.5 Serial Console

Most operating systems have a defined serial console. The KTT30/mITX board uses the first serial port (UARTA/ UART1) on connector J3 for this purpose. Normally the serial console needs only three signal lines (TXD, RXD and GND). The serial port is assigned to the environment variables **stdin**, **stdout** and **stderr**. If you use U-Boot as bootloader you can interact with U-Boot via a USB keyboard and a standard terminal program on a desktop computer. The following overview shows the default serial settings:

- Baudrate 115 kBaud
- Data bits 8
- Stop bits 1
- Parity No

8.6 Digital Connectors (S/PDIF)

The digital audio interface is available through the connectors J26 and J31 (2 pins).

Header	Pin	J26	J31	Type
	1	**SPDIF_OUT**	**SPDIF_IN**	O resp. I (J31)-3.3
	2	**GND**	**GND**	PWR

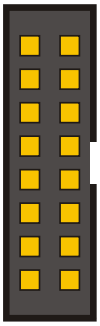
8.7 Headphone Connector

The headphone interface is available through the connector J32 (4 pins).

Header	Pin	Signal	Type
	1	**GND**	PWR
	2	**HPOUT-L**	AO
	3	**GND**	PWR
	4	**HPOUT-R**	AO

8.8 Front Panel Header (FRONTPNL)

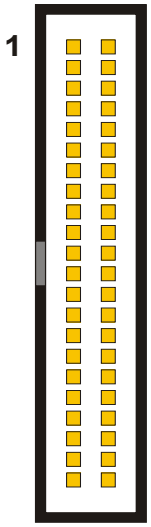
The power button and other power signals are available through the pin header J7 (16 pins).

Header	Pin	Signal	Description	Type	Ioh/Iol
 1	1	**GND**	Ground	PWR	
	2	**GND**	Ground	PWR	
	3	**BKLTADJ_DWN**	Backlight brightness down	I-1.8	
	4	**BKLTADJ_UP**	Backlight brightness up	I-1.8	
	5	**VCC5** 1)	Power supply +5V	PWR	
	6	**VCC5** 1)	Power supply +5V	PWR	
	7	**SATA_LED+**	S-ATA® LED	O-3.3	
	8	**DEEP_SLEEP**	Indicates deep sleep mode	O-5.0	
	9	**GND**	Ground	PWR	
	10	**PWR_BTN+** 2)	Power button (positive)	I-5.0	
	11	**RESET_IN**	Board reset input	I	
	12	**PWR_BTN-**	Power button (negative) = GND	PWR	
	13	**VCC3** 1)	Power supply +3.3V	PWR	
	14	**GND**	Ground	PWR	
	15	**GND**	Ground	PWR	
	16	**GND**	Ground	PWR	

Notes: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.
2) The label PWR_BTN (power button) is identical with NVIDIAs® 'ONKEY' button.

8.9 Feature Connector

The General Purpose I/O 's and a few other signals are available through the Feature connector J36.

Header	Pin	Signal	Description	Type	Ioh/Iol
	1	**CASE_OPEN#**	Case opened detection	I	
	2	**N.C.**	Not connected	NC	
	3	**CORE_PWR_ON**	T30 core rail enabled	O-5.0	
	4	**N.C.**	Not connected	NC	
	5	**DEEP_SLEEP**	Indicates deep sleep mode	O-5.0	
	6	**EXT_BAT**	External battery input	PWR	
	7 - 8	**N.C.**	Not connected	NC	
	9	**VCC3** 1)	Power +3.3V	PWR	
	10	**VCC5** 1)	Power +5V	PWR	
	11	**GPIO0**	General purpose I/O 0	IO-3.3	
	12	**GPIO1**	General purpose I/O 1	IO-3.3	
	13	**GPIO2**	General purpose I/O 2	IO-3.3	
	14	**GPIO3**	General purpose I/O 3	IO-3.3	
	15	**GPIO4**	General purpose I/O 4	IO-3.3	
	16	**GPIO5**	General purpose I/O 5	IO-3.3	
	17	**GPIO6**	General purpose I/O 6	IO-3.3	
	18	**GPIO7**	General purpose I/O 7	IO-3.3	
	19 - 20	**GND**	Ground	PWR	
	21	**GPIO8**	General purpose I/O 8	IO-3.3	
	22	**GPIO9**	General purpose I/O 9	IO-3.3	
	23	**GPIO10**	General purpose I/O 10	IO-3.3	
	24	**GPIO11**	General purpose I/O 11	IO-3.3	
	25	**GPIO12**	General purpose I/O 12	IO-3.3	
	26	**GPIO13**	General purpose I/O 13	IO-3.3	
	27	**GPIO14**	General purpose I/O 14	IO-3.3	
	28	**GPIO15**	General purpose I/O 15	IO-3.3	
	29	**GPIO16**	General purpose I/O 16	IO-3.3	
	30	**GPIO17**	General purpose I/O 17	IO-3.3	
	31 - 32	**GND**	Ground	PWR	
	33 - 37	**N.C.**	Not connected	NC	
	38	**GND**	Ground	PWR	
	39 - 40	**N.C.**	Not connected	NC	
	41 - 43	**GND**	Ground	PWR	
	44	**CPU_PWR_ON**	T30 CPU rail enabled	O-5.0	

Note: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

The General Purpose I/O's and a few other signals are available through the Feature connector J36.

Signal	Description
CASE_OPEN#	This signal is used to detect if the system case has been opened.
CORE_PWR_ON	This signal is an active high indication that the T30 CORE rail has been enabled. The signal is buffered for LED usage.
DEEP_SLEEP	This signal is an active high indication that the system has entered the deep sleep mode. The signal is buffered for LED usage.
EXT_BAT	EXTernal BATtery option for connecting the plus pin or terminal of an external primary cell battery (2.5 to 4.0V). The minus pin or terminal should be connected to a GND pin. The external battery is protected against charging and can be used with or without the onboard battery installed.
CPU_PWR_ON	This signal is an active high indication that the T30 CPU rail has been enabled. The signal is buffered for LED usage.

The three signals for LED usage assume the following states during power management:

Signal	ACTIVE	SUSPEND	DEEP SLEEP
CORE_PWR_ON	High	High	Low
CPU_PWR_ON	High	Low	Low
DEEP_SLEEP	Low	Low	High

General Purpose I/O Interface

The General Purpose I/O interface is a subset of a multifunction part from NVIDIAs® Tegra® 3 SoC. All I/O pins have additional functionalities which can be changed by software.

The I/O signals are decoupled to 3.3V voltage level by voltage level translators. With one I/O line (NVIDIA® label: Q.00) you can enable or disable all voltage level translators:

Active state **high** level
Tri-state **low** level

Electrical Specifications

Digital Input	Min.	Typ.	Max.	Units
Input LOW voltage			+1.1	V
Input HIGH voltage	+2.2	3.3	+3.8	V
Input rate (Linux)			tbd.	kHz

Digital Outputr	Min.	Typ.	Max.	Units
Output LOW voltage			+0.4	V
Output HIGH voltage	+2.9		+3.3	V
Continuous output current per pin			8	mA
Switching rate (Linux)			tbd.	kHz

Multifunction Overview

The following table informs about the dependencies.

I/O Pin	NVIDIA® Label	Second Function
GPI00	Q.01	Keyboard column 1
GPI01	Q.02	Keyboard column 2
GPI02	Q.03	Keyboard column 3
GPI03	Q.04	Keyboard column 4
GPI04	Q.05	Keyboard column 5
GPI05	Q.06	Keyboard column 6
GPI06	Q.07	Keyboard column 7
GPI07	R.00	Keyboard row 0
GPI08	R.01	Keyboard row 1
GPI09	R.02	Keyboard row 2
GPI010	R.03	Keyboard row 3
GPI011	R.04	Keyboard row 4
GPI012	R.05	Keyboard row 5
GPI013	S.01	Keyboard row 9
GPI014	S.02	Keyboard row 10
GPI015	S.03	Keyboard row 11
GPI016	S.04	Keyboard row 12
GPI017	S.05	Keyboard row 13

8.10 DC Power Connector Internal

The KTT30/mITX board has a power input voltage range from +4.5V to +5.5V. The power supply is connected via the connector J17 (4 pin Micro-Fit) or alternatively the external Power connector J2 (3 pins, DC power jacket 2.1mm). Notice that the +5V power lines on J2 and on J17 are connected on the board.

Header	Pin	Signal	Description
 1	1	VCC5 1)	Power supply +5V
	2	GND	Ground
	3	GND	Ground
	4	VCC5 1)	Power supply +5V

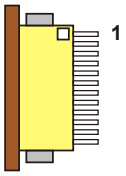
Warning: *Do not overload the onboard system voltage +3.3V resp. 1.8V (SD™ card socket, digital I/O connector). The maximum current should not exceed 250mA.*

Note: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

8.11 Touch Interface

By default the touch screen interface supports an I^2C^{TM} connection. Alternative a stuffing option allows the usage of a standard SPI^{TM} port. The complete interface is 3.3V compatible.

The touch screen interface is available through the connector J30 (12 pins).

Header	Pin	Signal	Description	Type
	1	**AVCC3** 1)	Analog power +3.3V	PWR
	2	**AVCC3** 1)	Analog power +3.3V	PWR
	3	**AVCC3** 1)	Analog power +3.3V	PWR
	4	**VCC3** 1)	Digital power +3.3V	PWR
	5	**SPI_CLK**	SPI^{TM} clock (alternative)	O-3.3
	6	**SPI_CS#**	SPI^{TM} slave select (alternative)	O-3.3
	7	**TS_IRQ#**	Interrupt (optional)	I-3.3
	8	**I2C_SDA** **SPI_MOSI**	I^2C^{TM} data SPI^{TM} master output (alternative)	IO-3.3 O-3.3
	9	**I2C_SCL** **SPI_MISO**	I^2C^{TM} clock SPI^{TM} master input (alternative)	IO-3.3 I-3.3
	10	**TS_RST#**	Reset (optional)	O-3.3
	11	**GND**	Ground	PWR
	12	**VCC1** 1)	Digital power +1.8V	PWR

Note: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

8.12 SPI™ Interface

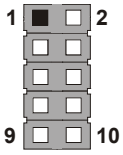
The KTT30 provides one synchronous full duplex Serial Peripheral Interface Bus (SPI™) for customer requirements. All four SPI™ signals are 5V tolerant.

Two things should be considered:

1. An onboard SPI™ flash coexists on the same interface lines. You must disable this component with a 3.3V power connection to the ADDIN signal (e.g. a short circuit jumper between pin 2 and 4).

2. The four SPI™ lines are protected with an additional bus driver and the ISOLATE# signal controls the output enable pin. For normal operation this signal should be high.

The SPI™ interface is available on connector J35 (pin header, 10 pins).

Header	Pin	Signal	Description	Type
	1	**SPI_CLK**	SPI™ clock	O-3.3
	2	**VCC3** 1)	Power +3.3V	PWR
	3	**SPI_CS#**	SPI™ slave select	O-3.3
	4	**ADDIN**	Disable onboard SPI flash	I-3.3
	5	**RSVD**	Reserved (10k pullup to 3.3V)	PWR
	6	**N.C.**	Not connected	NC
	7	**SPI_MOSI**	SPI™ master output	O-3.3
	8	**ISOLATE#**	Disable the SPI interface	I-3.3
	9	**SPI_MISO**	SPI™ master input	I-3.3
	10	**GND**	Ground	PWR

CAUTION!
If you permanently disable the onboard SPI™ flash then you disable the standard boot device which contains the U-Boot bootloader. In this case please contact your local Distributor or Field Application Engineer (FAE).

Note: *1) To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

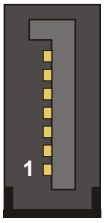
9 Standard Slot Connectors

9.1 SATA Connector

Only one S-ATA® 2.0 port is available. Serial-ATA® connections boost the data rate theoretically up to 300 MB/sec. In addition it changes the parallel interface requiring 40 separate wires to a serial interface requiring only 6 wires. The controller supports the Advanced Host Controller Interface (AHCI).

Note that SATA connector shares the internal SATA port with mSATA connector. If mSATA card is plugged in, then hardware automatically switches from the SATA connector to the mSATA card socket.

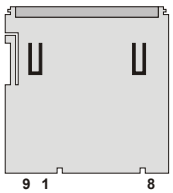
The S-ATA® interface is available through the standard L-type connector J28 (7 pins).

Header	Pin	Signal	Description	Type
	1	**GND**	Ground	PWR
	2	**TX+**	Transmit (positive)	DSO
	3	**TX-**	Transmit (negative)	DSO
	4	**GND**	Ground	PWR
	5	**RX-**	Receive (negative)	DSI
	6	**RX+**	Receive (positive)	DSI
	7	**GND**	Ground	PWR

9.2 Secure Digital and Multimedia Card

The SD/MMC interface uses two standard SD™ card sockets as well as an onboard SanDisk® 16 GByte embedded flash drive with an e.MMC interface. The controller supports the SD™ specification revision 3.0 (implies the SDSC, SDHC and SDXC families) and the MMC specification revision 4.4. The data bus width accounts 4 bits for the standard sockets and 8 bits for the flash drive, the SD™ card transfer rate can be up to 50 MHz and MMC rate up to 52 MHz. The onboard SanDisk® 16 GByte embedded flash drive is bootable.

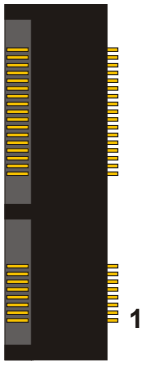
The SD™ card sockets are named J19 and J20 (9 pins).

Header	Pin	Signal	Description	Type
	1	**CD / DATA3**	Card detect / Data bit 3	IO-3.3
	2	**CMD**	Command line	IO-3.3
	3	**GND**	Ground	PWR
	4	**VCC3** [1)]	Power +3.3V	PWR
	5	**CLK**	Clock	O-3.3
	6	**GND**	Ground	PWR
	7	**DATA0**	Data bit 0	IO-3.3
	8	**DATA1**	Data bit 1	IO-3.3
	9	**DATA2**	Data bit 2	IO-3.3

9.3 Mini PCI Express® Connector

NVIDIAs® Tegra® 3 supports the PCI Express® specification 1.1 with 2.5 GT/s (GigaTransfers/s - identical with Gigabits/s by one lane). Two ports with one lane are provided for free usage. The first port has no additional features, the second port allows the switching between mini PCI Express® and mini S-ATA®.

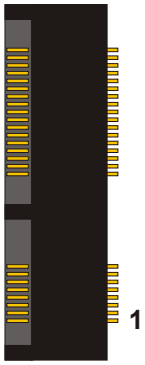
The pure mini PCI Express® port is available through the connector J5 (52 pins).



Header	Pin	Signal	Description	Type	Pin	Signal	Description	Type
	1	**WAKE#**	Wake event	I-3.3	2	**VCC3** 1)	Power +3.3V	PWR
	3	**N.C.**	Not connected	NC	4	**GND**	Ground	PWR
	5	**N.C.**	Not connected	NC	6	**VCC1** 1)	Power +1.5V	PWR
	7	**CLKREQ#**	PCIe® clock request	I-3.3	8	**N.C.**	Not connected	NC
	9	**GND**	Ground	PWR	10	**N.C.**	Not connected	NC
	11	**PE_CLK-**	PCIe® clock (neg.)	DSO	12	**N.C.**	Not connected	NC
	13	**PE_CLK+**	PCIe® clock (pos.)	DSO	14	**N.C.**	Not connected	NC
	15	**GND**	Ground	PWR	16	**N.C.**	Not connected	NC
	17	**N.C.**	Not connected	NC	18	**GND**	Ground	PWR
	19	**N.C.**	Not connected	NC	20	**W_DISABLE#**	Wireless disable	O-3.3
	21	**GND**	Ground	PWR	22	**PE_RST#**	PCIe® reset	O-3.3
	23	**PE_RX-**	PCIe® receive (neg.)	DSI	24	**VCC3** 1)	Power +3.3V	PWR
	25	**PE_RX+**	PCIe® receive (pos.)	DSI	26	**GND**	Ground	PWR
	27	**GND**	Ground	PWR	28	**VCC1** 1)	Power +1.5V	PWR
	29	**GND**	Ground	PWR	30	**I2C_CLK**	I2C™ clock	O-3.3
	31	**PE_TX-**	PCIe® transmit (neg.)	DSO	32	**I2C_DATA**	I2C™ data	IO-3.3
	33	**PE_TX+**	PCIe® transmit (pos.)	DSO	34	**GND**	Ground	PWR
	35	**GND**	Ground	PWR	36	**N.C.**	Not connected	NC
	37	**GND**	Ground	PWR	38	**N.C.**	Not connected	NC
	39	**VCC3** 1)	Power +3.3V	PWR	40	**GND**	Ground	PWR
	41	**VCC3** 1)	Power +3.3V	PWR	42	**N.C.**	Not connected	NC
	43	**GND**	Ground	PWR	44	**N.C.**	Not connected	NC
	45	**N.C.**	Not connected	NC	46	**N.C.**	Not connected	NC
	47	**N.C.**	Not connected	NC	48	**VCC1** 1)	Power +1.5V	PWR
	49	**N.C.**	Not connected	NC	50	**GND**	Ground	PWR
	51	**N.C.**	Not connected	NC	52	**VCC3** 1)	Power +3.3V	PWR

9.4 m PCIe / mSATA Connector

The mPCIe / mSATA port is available through the connector J4 (52 pins).

Header	Pin	Signal	Description	Type	Pin	Signal	Description	Type
 1	1	**WAKE#**	Wake event	I-3.3	2	**VCC3** [1)]	Power +3.3V	PWR
	3	**N.C.**	Not connected	NC	4	**GND**	Ground	PWR
	5	**N.C.**	Not connected	NC	6	**VCC1** [1)]	Power +1.5V	PWR
	7	**CLKREQ#**	PCIe® clock request	I-3.3	8	**N.C.**	Not connected	NC
	9	**GND**	Ground	PWR	10	**N.C.**	Not connected	NC
	11	**PE_CLK-**	PCIe® clock (neg.)	DSO	12	**N.C.**	Not connected	NC
	13	**PE_CLK+**	PCIe® clock (pos.)	DSO	14	**N.C.**	Not connected	NC
	15	**GND**	Ground	PWR	16	**N.C.**	Not connected	NC
	17	**N.C.**	Not connected	NC	18	**GND**	Ground	PWR
	19	**N.C.**	Not connected	NC	20	**W_DISABLE#**	Wireless disable	O-3.3
	21	**GND**	Ground	PWR	22	**PE_RST#**	PCIe® reset	O-3.3
	23	**PE_RX-** **SATA_RX+**	PCIe® receive (neg.) S-ATA® receive (pos.)	DSI	24	**VCC3** [1)]	Power +3.3V	PWR
	25	**PE_RX+** **SATA_RX-**	PCIe® receive (pos.) S-ATA® receive (neg.)	DSI	26	**GND**	Ground	PWR
	27	**GND**	Ground	PWR	28	**VCC1** [1)]	Power +1.5V	PWR
	29	**GND**	Ground	PWR	30	**I2C_CLK**	I2C™ clock	IO-3.3
	31	**PE_TX-** **SATA_TX-**	PCIe® transmit (neg.) S-ATA® transmit (neg.)	DSO	32	**I2C_DATA**	I2C™ data	IO-3.3
	33	**PE_TX+** **SATA_TX+**	PCIe® transmit (pos.) S-ATA® transmit (pos.)	DSO	34	**GND**	Ground	PWR
	35	**GND**	Ground	PWR	36	**N.C.**	Not connected	NC
	37	**GND**	Ground	PWR	38	**N.C.**	Not connected	NC
	39	**VCC3** [1)]	Power +3.3V	PWR	40	**GND**	Ground	PWR
	41	**VCC3** [1)]	Power +3.3V	PWR	42	**N.C.**	Not connected	NC
	43	**GND**	Ground	PWR	44	**N.C.**	Not connected	NC
	45	**N.C.**	Not connected	NC	46	**N.C.**	Not connected	NC
	47	**N.C.**	Not connected	NC	48	**VCC1** [1)]	Power +1.5V	PWR
	49	**N.C.**	Not connected	NC	50	**GND**	Ground	PWR
	51	**SEL_SATA#**	S-ATA® identification	I-1.8	52	**VCC3** [1)]	Power +3.3V	PWR

Note that SATA connector shares the internal SATA port with mSATA connector. If mSATA card is plugged in, then hardware automatically switches from the SATA connector to the mSATA card socket.

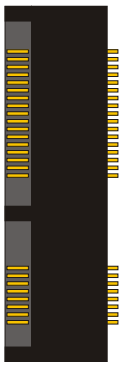
9.5 Modem Card Connector

The second host port (named USB2) can also be configured as a miniPCI Express® USB modem interface. With an USB 2.0 switch the host port supports either the standard connector J24 or the USB modem interface on connector J27. One I/O line (NVIDIA® label: L.05) enables the switching between the interfaces:

Standard connector J24 **low** level

Modem card connector J27 **high** level

The modem card interface is available through the connector J27 (52 pins).

Header	Pin	Signal	Description	Type	Pin	Signal	Description	Type
	1	**WAKE#**	Wake event	I-3.3	2	**VCC3** [1)]	Power +3.3V	PWR
	3	**N.C.**	Not connected	NC	4	**GND**	Ground	PWR
	5	**N.C.**	Not connected	NC	6	**VCC1** [1)]	Power +1.5V	PWR
	7	**N.C.**	Not connected	NC	8	**USIM_VCC**	USIM power	PWR
	9	**GND**	Ground	PWR	10	**USIM_IO**	USIM data	IO
	11	**N.C.**	Not connected	NC	12	**USIM_CLK**	USIM clock	O
	13	**N.C.**	Not connected	NC	14	**USIM_RST**	USIM reset	O
	15	**GND**	Ground	PWR	16	**USIM_VPP**	USIM progr. volt.	PWR
	17	**USIM_USB-**	USIM USB (neg.)	DSIO	18	**GND**	Ground	PWR
	19	**USIM_USB+**	USIM USB (pos.)	DSIO	20	**W_DISABLE#**	Wireless disable	O-3.3
	21	**GND**	Ground	PWR	22	**PE_RST#**	PCIe® reset	O-3.3
	23	**N.C.**	Not connected	NC	24	**VCC3** [1)]	Power +3.3V	PWR
	25	**N.C.**	Not connected	NC	26	**GND**	Ground	PWR
	27	**GND**	Ground	PWR	28	**VCC1** [1)]	Power +1.5V	PWR
	29	**GND**	Ground	PWR	30	**I2C_CLK**	I2C™ clock	O-3.3
	31	**N.C.**	Not connected	NC	32	**I2C_DATA**	I2C™ data	IO-3.3
	33	**N.C.**	Not connected	NC	34	**GND**	Ground	PWR
	35	**GND**	Ground	PWR	36	**USB-**	USB port (neg.)	DSIO
	37	**GND**	Ground	PWR	38	**USB+**	USB port (pos.)	DSIO
	39	**VCC3** [1)]	Power +3.3V	PWR	40	**GND**	Ground	PWR
	41	**VCC3** [1)]	Power +3.3V	PWR	42	**N.C.**	Not connected	NC
	43	**GND**	Ground	PWR	44	**N.C.**	Not connected	NC
	45	**MODEM_CLK**	Modem clock	O	46	**N.C.**	Not connected	NC
	47	**MODEM_DIN**	Modem data in	O	48	**VCC1** [1)]	Power +1.5V	PWR
	49	**MODEM_DOUT**	Modem data out	I	50	**GND**	Ground	PWR
	51	**MODEM_CS**	Modem chip sel.	O	52	**VCC3** [1)]	Power +3.3V	PWR

Appendix A: System Resources

A.1 Memory Area

All registers of the Tegra® 3 processor are memory-mapped. Do not write to the register range if you have no knowledge about the register function.

Memory Range	Used for	Available	Comment
00000000h - 3FFFFFFFh	PCI Express® memory	No	Reserved for operating systems
40000000h - 4003FFFFh	Internal RAM (IRAM)	No	Normally do not access the IRAM
50000000h - 7FFFFFFFh	Processor registers	No	
80000000h - FFEFFFFFh	External SDRAM	Yes	Read- and writeable

Appendix B: Mating Connectors

The Mating connectors / Cables are connectors or cable kits which are fitting the On-board connector.

Connector		Onboard Connectors		Mating Connectors	
		Manufacturer	P/N	Manufacturer	P/N
Power (External)	J2	Kycon	KLDHCX-0202-A-LT		
Power (Internal)	J17	Molex	0430450402	MOLEX	43025-0400
				Kontron	KT 1052-5080 (cable kit)
LVDS	J1	SAMTEC	SHF-120-01-F-D-SM-K-TR	Don Connex	A32-40-C-G-B-1
		Hon Kon Technology	HB12-220-VFS-20R	Kontron	KT 910000005
		WIESON TECHNOLOGIES	G2124-03200101-00	Kontron	KT 821515 (cable kit)
		DON CONNEX	C44-40BSBC1-G	Kontron	KT 821155 (cable kit)
Fan	J15	MOLEX	22-05-3041	MOLEX	22-01-2045
		FOXCONN	HF1804E-K		
ccTalk	J29	MOLEX	22-05-3041	MOLEX	22-01-2045
		FOXCONN	HF1804E-K		
UART1/UART3	J3/J6	PINREX	511-90-10GB00	Molex	90635-1103
		FOXCONN	HL8605V	Kontron	KT 821016 (cable kit)
				Kontron	KT 821017 (cable kit)
Frontpanel	J7	PINREX	511-90-16GB00	Molex	90635-1243
		FOXCONN	HL8608V	Kontron	KT 1055-5493 (cable kit)
Touch	J30	MOLEX	54550-1294		
Feature	J36	PINREX	52C-90-44GB00	Don Connex	A05c-44-B-G-A-1-G
		FOXCONN	HS5422F		
S/PDIF-In	J31	MOLEX	53047-0210	MOLEX	51021-0200
S/PDIF-Out	J26	MOLEX	53047-0210	MOLEX	51021-0200
Headphone	J32	MOLEX	53047-0410	MOLEX	51021-0400

KTT30 Cable kit PN 826604:

PN	Qty.	Description
821017	2	Cable, COM, 2.54mm, 100mm
821515	1	Cable, LVDS Open-End
821035	1	Cable, SATA, 500mm
1052-5885	1	Cable, Feature 44pol 1 to1, 300mm
1055-5493	1	Cable, Front Panel 16pol, Open-End
1052-5080	1	Cable ATX Power for KTT30

Appendix C: Reference Documents

KONTRON Technology A/S can't guarantee the availability of internet addresses.

Document	Internet Address
NVIDIA® Development	http://developer.nvidia.com/tools/Development
Linux® for Tegra®	http://developer.nvidia.com/linux-tegra
Digital Visual Interface (DVI®)	http://www.ddwg.org
Open LVDS Display Interface Standard Spec. (Open LDI™)	http://www.national.com/analog/displays/open_ldi
IEEE 802.3® Specification (Ethernet)	http://standards.ieee.org/getieee802
Universal Serial Bus Specification (USB)	http://www.usb.org/developers/docs
PCI Express® Base Specification (PCI Express®)	http://www.pcisig.com/specifications
High Speed Serialized AT Attachment (S-ATA) ®	http://www.sata-io.org/developers
SD Specification (SD Card)	http://www.sdcard.org/developers/tech/sdio/sdio_spec

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