» Kontron User's Guide «

KTA75/Flex

KTD-N0876-C

» Table of Contents «

Document Revision History

Rev.	Date	By	Comment
C	04/2016	GSZ	New memory SKU
B			EXT_BAT max. 3.47 V.
A	Nov 28th 2013	MLA	First release.
0	Mar 21st 2013	MLA	Preliminary version of KTA75/Flex.

Copyright Notice

Trademark Acknowledgement

Brand and product names are trademarks or registered trademarks of their respective owners.

Disclaimer

KONTRON Technology A/S reserves the right to make changes without notice to any product, including circuits and/or software described or contained in this manual in order to improve design and/or performance.
Specifications listed in this manual are subject to change without notice. KONTRON Technology assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright or mask work rights to these products and makes no representations or warranties that these products are free from patent, copyright or mask work right infringement unless otherwise specified. Applications that are described in this manual are for illustration purposes only. KONTRON Technology A/S makes no representation or warranty that such application will be suitable for the specified use without further testing or modification.

Life Support Policy

KONTRON Technology's PRODUCTS ARE NOT FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT EXPRESS WRITTEN APPROVAL OF THE GENERAL MANAGER OF KONTRON Technology A/S.

As used herein:
Life support devices or systems are devices or systems which (a) are intended for surgical implant into body or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labelling can be reasonably expected to result in significant injury to the user.
A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

KONTRON Technology Technical Support

If you have questions about installing or using your KONTRON Technology Product, then check this User's Manual first – you will find answers to most questions here. To obtain support please contact your local Kontron Sales Partner or Kontron Field Application Engineer (FAE).

Before Contacting Support: Please be prepared to provide as much information as possible:

- CPU Board
    1. Type and P/N (Part Number), find label like:

        KTA75/Flex P/N: |||| |||||||||||||| | ||| 66110000

    2. S/N (Serial Number), find label like:

        Prod.code:A4Q S/N: ||| |||||||||||| | ||| 01111336

- Configuration (if relevant)
    1. CPU Type and Clock speed
    2. DRAM Type and Size.
    3. BIOS Revision (find the version info in the BIOS Setup Menu).
    4. BIOS Settings different than *Default* Settings.

- System (if relevant)
    1. OS (Operating System) Make and Version.
    2. Driver Version numbers: Graphics, Network, and Audio etc.
    3. Attached Hardware: Harddisks, CD-Rom, Display Panels etc.

If the Kontron Technology product seems to be defect and you want to return it for repair, please follow the guide lines from the following page:

http://kontron.com/services/rma-information/kontron-technology-a-s/

Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:

    A. Accident, misuse, neglect, fire, water, lightning or other acts of nature, unauthorized product modification or failure to follow instructions supplied with the product.

    B. Repair or attempted repair by anyone not authorized by KONTRON Technology.

    C. Causes external to the product, such as electric power fluctuations or failure.

    D. Normal wear and tear.

    E. Any other causes which does not relate to a product defect.

2. Removal, installation and set-up service charges.

Exclusion of damages:

KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:

1. DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCON- VENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.

2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.

3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.

1   Introduction

This manual describes the KTA75/Flex board made by KONTRON Technology A/S. The board will also be denoted KTA75 within this Users Guide.

The KTA75 is designed to support the below listed APU variants (uPGA 722pin processors) and AMD A75 Fusion Controller Hub (FCH) A75 on a Flex form factor.

APU variants	AMD PN	Processor data
R-464L	RE464LDEC44HJE	2.3 GHz – Quad Core – 35W
R-460H	RE460HDEC44HJE	1.9 GHz – Quad Core – 35W
R-272F	RE272FDEC23HJE	2.7 GHz – Dual Core – 35W
R-268D	RE268DDEC23HJE	2.5 GHz – Dual Core – 35W
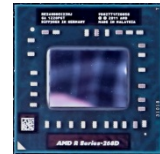
See the chapter *System Specifications* for more specific details.The 4 versions have the same type of active CPU cooler (the cooler is by default not premounted, but can be ordered with this obtion).

Use of this Users Guide implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KTA75 board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the *Installation Procedure* stated in the following chapter before switching-on the power.

All configuration and setup of the CPU board is either done automatically or manually by the user via the BIOS setup menus. Only exceptions are the *Clear CMOS jumper* and the *Always On jumper*.

Note: Sufficient cooling must be applied to the CPU in order to remove the effect as listed in above table (Thermal Guideline). The sufficient cooling is also depending on the maximum (worst-case) ambient operating temperature and the actual load of processor.

The Kontron PN 1044-9447 is "Active Cooler for KTQM67/KTQM77" capable of being used for processors (fully loaded) having Thermal Guideline up to 45W @ 60ºC ambient temperature. MTBF is 70.000 hours @ 40ºC.

The Kontron PN 1052-6345 "Cooler Active KTQM67 35W 33mm longlife" is capable of being used for processors (fully loaded) having Thermal Guideline up to 35W @ 60ºC ambient temperature. It support 1U and has long life (MTBF is 200.000 hours @ 60ºC).
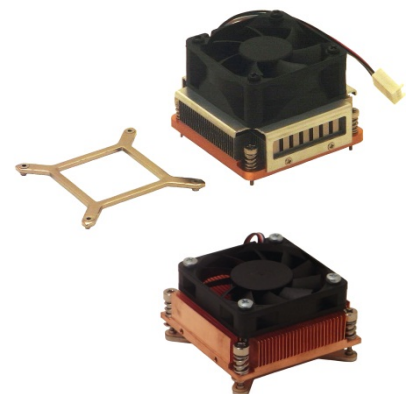
Latest revision of this manual, datasheet, BIOS, drivers, BSP's (Board Support Packages), Mechanical drawings (2D and 3D) can be downloaded from here:
http://kontron.com/products/boards+and+mezzanines/embedded+motherboards/miniitx+motherboards/kta70mmitx.html

2　Installation Procedure

2.1　Installing the Board

To get the board running, follow these steps. If the board shipped from KONTRON has already components like CPU and RAM mounted, then relevant steps below can be skipped.

1. **Turn off the PSU (Power Supply Unit)**

   ⚠️ **Warning**: Turn off PSU (Power Supply Unit) befor configuring the board and do not hot plug power supply, otherwise components (RAM, LAN cards etc.) might get damaged.

2. **Install the CPU into the socket**

   Make sure the lock is in the unlocked position.
   Insert the CPU, pay attention to the mark.
   By use of suitable screwdriver turn the lock to the locked position.

   Lock
   (Shown in unlocked position)

   Mark

3. **Insert the DDR3 DIMM 240pin module(s)**
   Be careful to push it in the slot(s) before locking the tabs.

4. **Connecting Interfaces and PSU**
   Insert all external cables for hard disk, keyboard etc. A display/monitor must be connected in order to be able to change BIOS settings. Connect a standard ATX/BTX PSU to the board by the inserting power cables into 24-pin ATX and the 4-pin ATX+12V PWR plugs connectors.

5. **Power Button**
   Turn on mains power to the PSU. If board doesn't boot, then PWRBTN_IN must be toggled; this is done by shorting pins 16 (PWRBTN_IN) and pin 18 (GND) on the FRONTPNL connector (see Connector description), by use of a "normally open" switch etc.

6. **BIOS Setup**
   Enter the BIOS setup by pressing the <Del> key during boot up. Enter Exit Menu and Load Optimal Defaults. Refer to the "BIOS Configuration / Setup" section of this manual for details on BIOS setup.

   Note: To clear all BIOS settings, including Password protection, activate "Clear CMOS" Jumper for ≈10 sec (without power connected).

7. **Mounting the board to chassis**

   ⚠️ **Warning**: When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the Motherboard on a chassis it is recommended using screws with integrated washer and a diameter of ≈7mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

2.2   Requirements IEC60950

Take care when designing chassis interface connectors in order to fulfil the IEC60950 standard.

When an interface or connector has a VCC (or other power) pin which is directly connected to a power plane like the VCC plane:
To protect the external power lines of the peripheral devices the customer has to ensure:
- Wires have suitable rating to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC60950.

Lithium battery precautions

CAUTION! Danger of explosion if battery is incorrectly re- placed. Replace only with same or equivalent type recommended by manufacturer. Dispose of used batteries according to the manufacturer's instruc- tions.	**VORSICHT!** Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Anga- ben des Herstellers.
ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie. Remplacement seulement par le même ou un type équivalent recommandé par le producteur. L'évacuation des batteries usagées conformément à des indications du fabricant.	**PRECAUCION!** Peligro de explosión si la batería se sustituye incorrectamente. Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante. Disponga las baterías usadas según las instrucciones del fabricante.
ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.	**ADVARSEL!** Eksplosjonsfare ved feilaktig skifte av batteri. Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten. Brukte batterier kasseres i henhold til fabrikantens instruksjoner.
VARNING! Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.	**VAROITUS!** Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

2.3 System Memory support

Notes: Kontron offers the following memory modules:
Please notice that not all speeds are supported by all CPU's.

NEW SKU 04/2016*	SKU Name**	OLD SKU before 04/2016
1060-2470	DDR3-1066 DIMM 1GB	1028-6891
1060-2474	DDR3-1066 DIMM 2GB	1030-5747
1060-2472	DDR3-1333 DIMM 1GB	1030-5722
1060-2480	DDR3-1333 DIMM 4GB	1050-3141
1060-2488	DDR3-1600 DIMM 8GB	1052-5601

*SKU changes were caused by administrative issues only, no hardware changes.
**Named are always the min. requirements, the shipped memory can fulfill a higher performance level

3 System Specifications

3.1 Component main data

The table below summarizes the features of the KTA75/Flex embedded motherboards.

Form factor	Flex: 190,5 x 228,6 mm / 7,5 x 9,0"
Processor	AMD eTrinity FP2 processor: • Quad-Core 2.3 GHZ with R-464L APU 35W • Quad Core 1.9 GHz with R-460H APU 35W • Dual Core 2.7 GHz with R-272F APU 35W • Dual Core 2.5 GHz with R-268D APU 35W • Compatible with Existing 32-Bit x86 and 64-bit AMD64 Code Base • AMD64 64-bit ISA • High Performance Floating-Point Unit • SSE 4.1 & 4.2, AVX 1.0 &1.1, AES, XOP, FMA4 • Secure advanced Virtualization Features • 64-bit DDR3 SDRAM Controller (1333MT/s,666MHz): PC3-10600 / (1600MT/s,800MHz): PC3-12800 • Compliant with JEDEC DDR3 1.5V and LV-DDR3 1.35V/1.25V SDRAM specification. Note:LV-DDR3 modules not validated • PCIe® Technology • Integrated Memory Controller • Integrated Graphics AMD Radeon™ HD 7000G Series graphics. • Dedicated graphics memory controller • 2D Acceleration Features • Open GL 4.2 & 2.0 • DirectX® 11 compliant 3D Acceleration Features • Adaptive Anti Aliasing, Shader Model 5 • Motion Video Acceleration Features • Dedicated hardware (UVD 3) for H.264 • VC-1, DivX and MPEG2 decode • HDCP (High-bandwidth Digital Content Protection) supported on DisplayPort. • Display Port 1.2 • Support DVI/HDMI via passive adapter.
Companion Device	AMD A75 (Hudson)Fusion Controller Hub • Unified Media Interface (UMI) (5.0 GT/s) • PCI Express® 2.0 Controller • PCI Host Bus Controller • USB Controllers with up to 14 USB ports • SMBus Controller • SATA Controller with RAID 0,1,10 support • High Definition Audio • Real Time Clock (RTC) • Integrated Clock controller • ACPI 3.0 compliant

Memory	Memory controller is integrated in the AMD eTrinity FS1r2 uPGA 722pin processor. Features are: • Compliant with JEDEC DDR3 1.5V and *(LV-DDR3 1.35V / 1.25 SDRAM, not verified)* specifications • Supports DDR3 UDIMM 240pin Using up to 8GB DRAM technology • DDR3 1333/1600MT/s (PC3-10600/PC3-12800) • From 1GB to 2x 8GB maximum (16GB in total) Notes: Less than 4GB displayed in System Properties using 32bit OS (Shared Video Memory/PCI resources is subtracted) ECC not supported
Flash (BIOS)	32Mbit SPI Flash for dual System BIOS.
Security	Intel® Integrated TPM 1.2 support Infineon TPM SLB9635TT1.2 (FW 3.17)
IT8516E Embedded Controller	KT Feature Connector. 15 Multiplexed (GPIO, DAC, ADC, PWM & TIMER) Possible 152 GPIO expansion. Software Watchdog.
Audio Codec	Audio, 7.1 Channel High Definition Audio Codec using the VIA VT1708S codec
Seriel ATA	6x SATA port J9 – J13 & J39, SATA 3.0 1x mSATA J39 (mechanically sharing space with mPCIe slot J38), SATA 3.0 • RAID 0,1,10 support
Frontpanel	2xUSB, HDD-LED, SYSRST#, SUSLED, PWRBTN#, AUDIO Line/MIC output.
PCI	2x PCI slots (PCI Local Bus Specification revision 2.3 32bit/33MHz)
PCIe	1x PCI Express x16 Slot 1x PCI Express x4 Slot (in mechanically x16 slot) 1x mPCIe Slot J38 1x mPCIe/mSATA J43 (mechanically sharing between mSATA and mPCIe). The mSATA interface will be selected when a mSATA card are inserted into the mPCIe socket (J43)
DisplayPort	3x DisplayPort connector (in REAR-IO area) DP1 J44 DP2 J3 DP0 J4 Optionally Add-On card with 1x DisplayPort
LVDS	Optionally Add-On card (TBD)
Audio Jack	3x Audiojacks stack J40 (in REAR-IO area) Blue Line-In Green Speaker Pink Mic
Audio	Audio Pin header J41 Line-out Line-in Surround output: SIDE, LFE, CEN, BACK and FRONT Microphone: MIC1 SPDIF-OUT (electrical Interface only)

LAN	Two RJ45 connectors J8 (in REAR-IO area) • 2x 10/100/1000Mbits/s LAN (ETH1/ETH2) using Intel® Pearsonville xGB PCI Express Ethernet controller (WGI211ATSLJXZ). • PXE Netboot supported. • Wake On LAN (WOL) supported

USB	14x USB ports (10x USB2.0 & 4x USB2.0/USB3.0):
	   2x USB2.0 in Frontpanel Connector J5
	   2x USB2.0 in USB Internal USB Connector J16
	   4x USB2.0, USB stack J20 (in REAR-IO area)
	   2x USB 2.0/USB3.0, Right USB stack J14 (in REAR-IO area)
	   2x USB 2.0/USB3.0, left USB stack J15 (in REAR-IO area)
	   1x USB 2.0 in mPCIe socket J38
	   1x USB 2.0 in mSATA/mPCIe socket J43

Serial port	2x RS232 pin header (+12V, -12V supply generated by driver circuit)
	   COM1 2x 5 Pin row J23
	   COM2 2x 5 Pin row J22

LPC	LPC connector J29
FAN	CPUFAN 4 pin row J25 12V PWM SYSFAN 4 pin row J24 12V PWM
PS2 Kbd/Mse	1x 6 Pin row Keyboard / Mouse PS2 cable kit interface J27
Power Plug	ATX12V: 1x 4 pole connector J19 (core power) and 1x 24 pole connector J17 ATX/BTX
Battery	Exchangeable 3.0V Lithium battery for on-board Real Time Clock and CMOS RAM. Manufacturer Panasonic / Part-number CR-2032L/BN, CR2032N/BN or CR-2032L/BE. Approximate 6 years retention. Current draw is 4 µA when PSU is disconnected and 0 µA in S0 – S5. CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.
Speaker	On-board Speaker Piezo On-board speaker (Electromagnetic Sound Generator like Hycom HY-05LF)
BIOS	AMI EFI SPI Connector J21 (for BIOS Recovery) Clear CMOS J34 Always On J37
OS (planned)	Windows 7 (32 and 64bit) Windows 8 (32 and 64bit) Windows XP (32 bit) DOS Windows Embedded 7

Environmental	Operating: 0°C – 60°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. 10% - 90% relative humidity (non-condensing) Storage: -20°C – 70°C; lower limit of storage temperature is defined by specification restriction of on-board CR2032 battery. Board with battery has been verified for storage temperature down to -40°C by Kontron. 5% - 95% relative humidity (non-condensing) Electro Static Discharge (ESD) / Radiated Emissions (EMI): All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard. Safety: EN 60950-1: 2006/ A11:2009/ A1:2010/A12:2011 IEC 60950-1(ed.2) CSA C22.2 No. 60950-1 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252 (E194252-A21-CB-1) Theoretical MTBF: 314.614 / 153.436 hours @ 40°C / 60°C Restriction of Hazardous Substances (RoHS): All boards in the KTA75 family are RoHS/RoHS-II compliant. Capacitor utilization: No Tantalum capacitors on board Only Japanese brand Solid capacitors rated for 100 °C used on board

3.2　KTA75/Flex Block Diagram

2x UDIMM DDR3 Dual Channel 1067/1333

3x DP (DisplayPort 1.2)

eTrinity APU Processor 722pin uPGA

PCIe x16 (x16slot) Graphics

4x USB3.0/USB2.0 10x USB2.0

VIA Audio Codec

SPI BIOS Flash

2x Fan (CPU/System)

A75 FCH

1x PCIe x4 (x16 slot) 1x mPCIe w. USB2.0 1x mPCIe/mSATA w. USB2.0 2x PCI 32bit/33MHz

2x 10/100/Gbe Intel Pearsonville I211AT

5x SATA3.0, RAID0/1/10 1x SATA or mSATA (shared) (mSATA shared w. mPCIe)

TPM (Infineon)

2x COM (RS232)

6-pin PS/2 Keyboard/Mouse

Embedded Controller ITE8516

Feature connector: SMBus/I2C GPIO/DAC/ADC/PWM GPIO expansion (up to 152) Intruder

3.3   Power Consumption

On the following pages the power consumption of the KTA75 Board is measured under:

1- DOS, idle, mean
2- Windows 7, Running 3DMARK 2005 & BiT 6, mean
3- S1, mean
4- S3, mean
5- S4, mean

The following items were used in the test setup:

1. **Low Power Setup:**
   Standard system configuration equipped with PCI card, internal graphics, 2x SATA HDD, AMD R-460H @ 1.9GHz CPU, 1x DIMM (1GB Modules), CRT Monitor, Keyboard & Mouse. 1x 1-4GB USB Stick.

   High Power Setup:
   Standard system configuration equipped with PCI, PCIex1, PCIex16, miniPCIe WLAN or mSATA HDD, 4x SATA HDD, AMD R-460H @ 1.9GHz CPU, 2x DIMM (2+2GB Modules), CRT Monitor, Keyboard & Mouse, 4x 4-8GB USB Sticks

2. 12V active cooler (BOX)
3. USB Keyboard/Mouse Genius
4. DELL 2407WFPg
5. 3.5" HDD WD
6. ATX Eurocase 450W
7. Tektronix TDS5104B
8. Tektronix TCPA300
9. Tektronix TCP312
10. Fluke 289
11. ATX Switcher
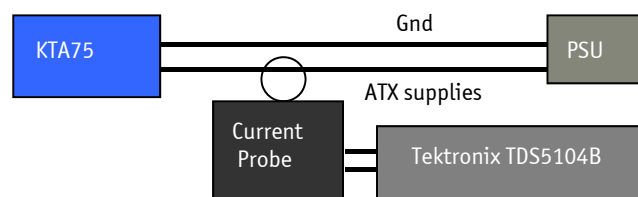
   Note: The Power consumption of Monitor and HDDs is not included.

Warning: Hot Plugging power supply is not supported. Hot plugging might damage the board.

Low Power Setup results:

DOS Idle, Mean, No external load		
Supply	**Current draw**	**Power consumption**
+12V	0.2545A	3.054W
+12V P4	1.4245A	17.094W
+5V	0.6717A	3.3585W
+3V3	0.6496A	2.14368W
-12V	32.17mA	0.38604W
5VSB	0.5mA	0.0025W
Total		26.0387W

Windows 7, mean 3DMARK2005 (first scene) & BiT 6		
Supply	**Current draw**	**Power consumption**
+12V	0.2545A	3.054W
+12V P4	1.8234A	21.8808W
+5V	0.8842A	4.421W
+3V3	0.4789A	1.58037W
-12V	32.12mA	0.38544W
5VSB	0.5mA	0.0025W
Total		31.3241W

S3 Mode, Mean, No external load		
Supply	**Current draw**	**Power consumption**
+12V	0	0W
+12V P4	0	0W
+5V	0	0W
+3V3	0	0W
-12V	0	0W
5VSB	114.11mA	0.57055W
Total		0.57055W

S4 Mode, Mean, No external load		
Supply	**Current draw**	**Power consumption**
+12V	0	0W
+12V P4	0	0W
+5V	0	0W
+3V3	0	0W
-12V	0	0W
5VSB	96.52mA	0.4826W
Total		0.4826W

High Power Setup results:

DOS Idle, Mean, No external load		
Supply	**Current draw**	**Power consumption**
+12V	0.6898A	8.2776W
+12V P4	1.5452A	18.5424W
+5V	1.0571A	5.2855W
+3V3	1.1882A	3.92106W
-12V	32.23mA	0.38676W
5VSB	0.5mA	0.0025W
Total		36.41582W

Windows 7, mean 3DMARK2005 (first scene) & BiT 6		
Supply	**Current draw**	**Power consumption**
+12V	0.6905A	8.286W
+12V P4	2.0547A	24.6564W
+5V	1.4275A	7.1375W
+3V3	1.1967A	3.94911W
-12V	32.43mA	0.38916W
5VSB	0.5mA	0.0025W
Total		44.42067W

S3 Mode, Mean, No external load		
Supply	**Current draw**	**Power consumption**
+12V	0	0W
+12V P4	0	0W
+5V	0	0W
+3V3	0	0W
-12V	0	0W
5VSB	265.73mA	1.32865W
Total		1.32865W

S4 Mode, Mean, No external load		
Supply	**Current draw**	**Power consumption**
+12V	0	0W
+12V P4	0	0W
+5V	0	0W
+3V3	0	0W
-12V	0	0W
5VSB	256.37mA	1.28185W
Total		1.28185W

3.4   USB ports overview

The KTA75 board contains two pairs of EHCI (Enhanced Host Controller Interface) and OHCI (Open Host Controller Interface) in order to support up to 10 USB1.1/USB2.0 devices and further more two xHCI (Extensible Host Controller Interface) to support up to 4 USB3.0 devices.

The OHCI controllers support USB1.1, Full-Speed (12Mbps) and Low-Speed (1.5Mbps).

The EHCI controllers support USB2.0, High-Speed (480Mbps).

The xHCI controllers support USB3.0, USB2.0 and USB 1.1, Super-Speed (5.0Gbps), High-Speed (480Mbps), Full-Speed (12Mbps) and Low-Speed (1.5Mbps)

Legacy Keyboard/Mouse and wakeup from sleep states are supported. Over-current detection on all USB ports except USB2.

USB #	USB standard	Connector location	HCI	Note
USB0 USB1	USB2.0 /USB1.1	Frontpanel (J5)	OHCI1/EHCI1	
USB2	USB2.0 /USB1.1	mPCIe (J38)	OHCI1/EHCI1	No over current detection
USB3	USB2.0 /USB1.1	mSATA/mPCIe (J43)	OHCI1/EHCI1	No over current detection
USB4	USB2.0 /USB1.1	Pin row (J16)	OHCI1/EHCI1	
USB5	USB2.0 /USB1.1	Pin row (J16)	OHCI2/EHCI2	
USB6 USB7 USB8 USB9	USB2.0 /USB1.1	USB quad stack (J20) Rear IO	OHCI2/EHCI2	
USB10 USB11	USB3.0/USB2.0/USB1.1	USB3.0 dual stack (J15) Left - Rear IO	xHCI1	
USB12 USB13	USB3.0/USB2.0/USB1.1	USB3.0 dual stack (J14) Right - Rear IO	xHCI2	

Notes: *In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.*

The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 1000mA.

Do not supply external USB devices with higher power dissipation through these pinsTo protect the external power lines of peripheral devices make sure that
   - the wires have the right diameter to withstand the maximum available current.
   - to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

For USB2.0 cabling it is required to use only HiSpeed USB cable, specified in USB2.0 standard:
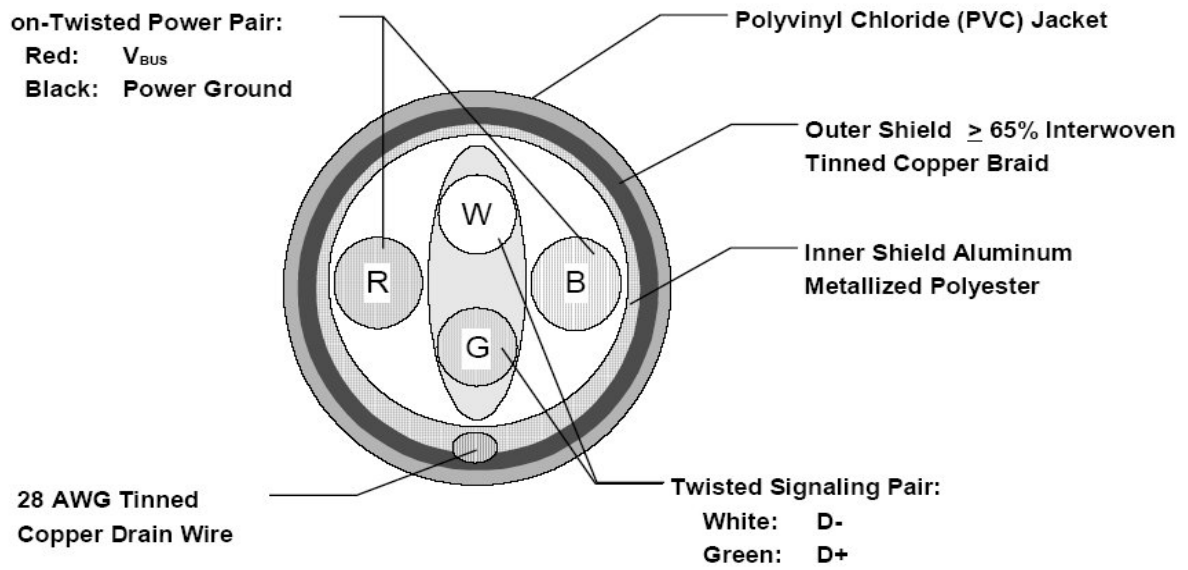
For USB3.0 cabling it is required to use only HiSpeed USB cable, specified in USB3.0 standard:
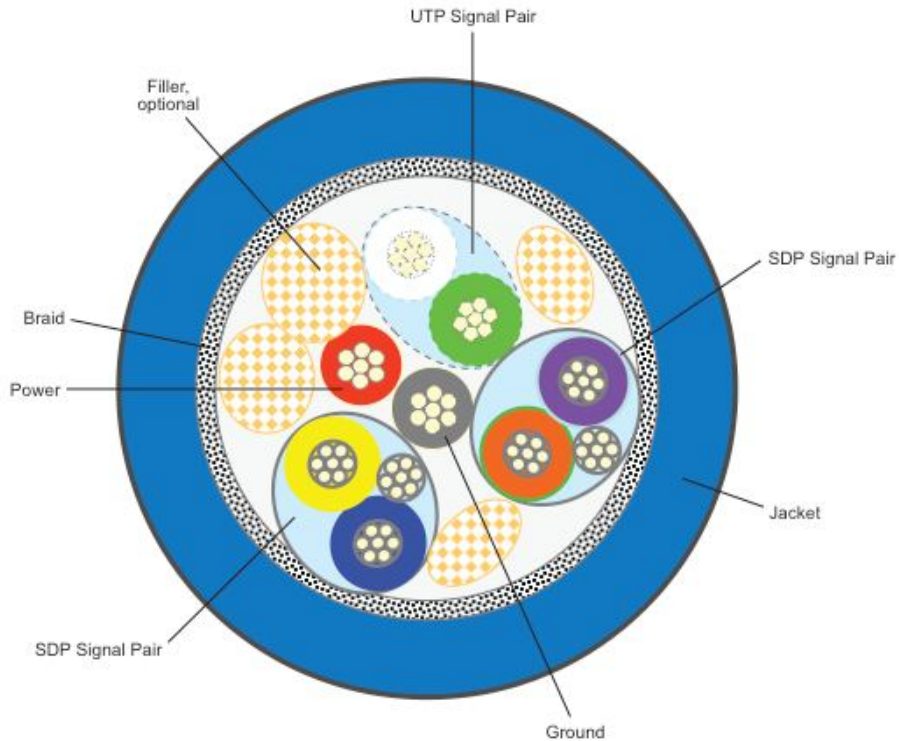
4   Connectors Locations

4.1   KTA75/Flex Topview

Power J17
ATX-BTX

mSATA/mPCIe J43

mPCIe J38

CPUFan J25

SysFan J24

UDIMM J1

UDIMM J2

Frontpanel J5

KBD/MSE J27

Power J19
ATX-core power

SATA4 SATA2 SATA0
SATA5 SATA3 SATA1

Feature J26

LPC J29

COM1 J23

COM2 J22

PCIex4 J6
(x16 slot)

PCIex16 J7
(x16 slot)

PCI 32b J18

PCI 32b J28

SPI J21

AlwaysOn J37

ClearCMOS J34

NC J36

USB4/5 J16   Audio J41
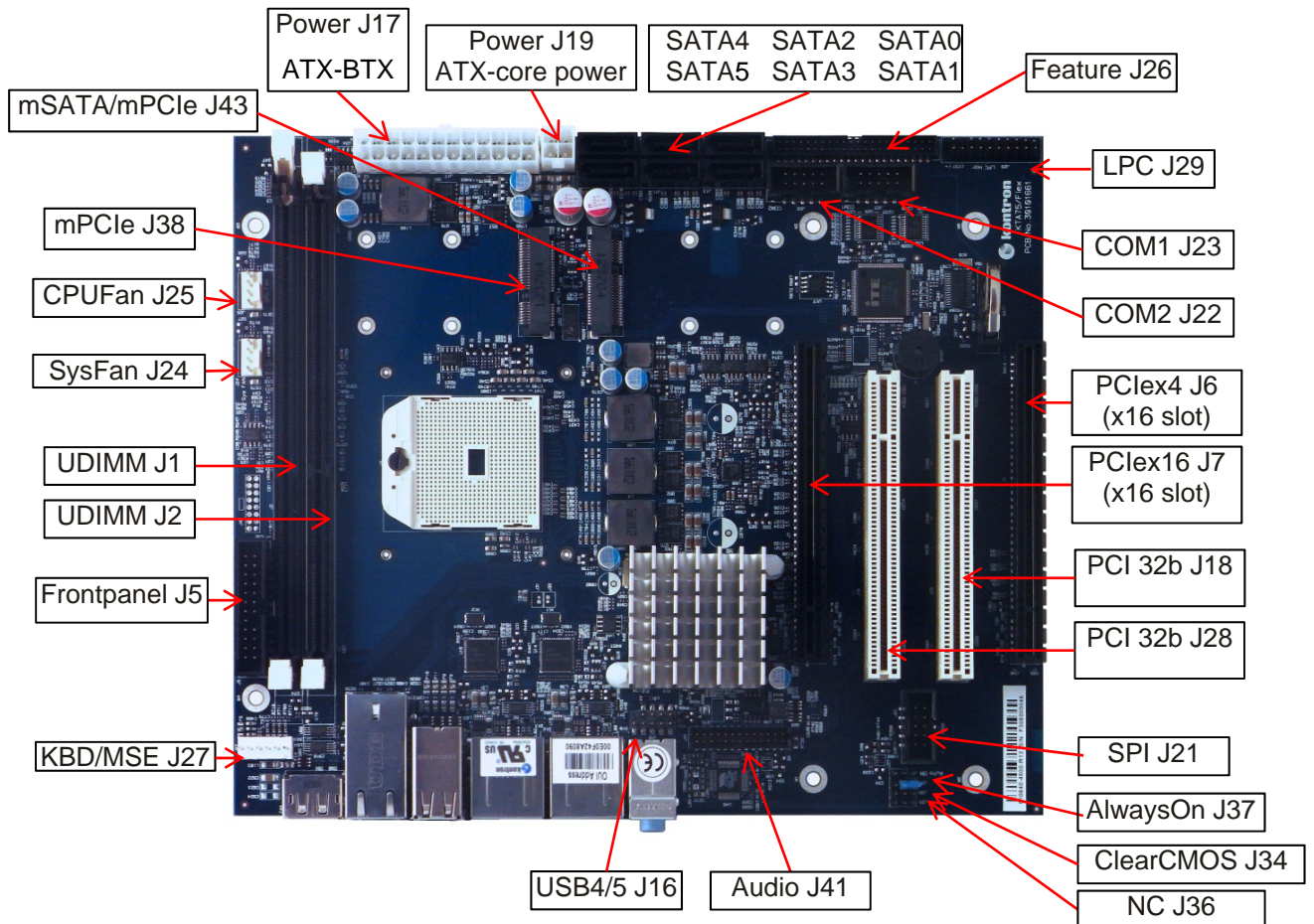
Note: SATA5 and mSATA (J43) is shared.

DP1 J44

ETH1
ETH2
J8

USB6
USB7
USB8
USB9
J20

USB12 J14
USB13 J14
DP0 J4

USB10 J15
USB11 J15
DP2 J3

LineIn
LineOut
Mic
J40
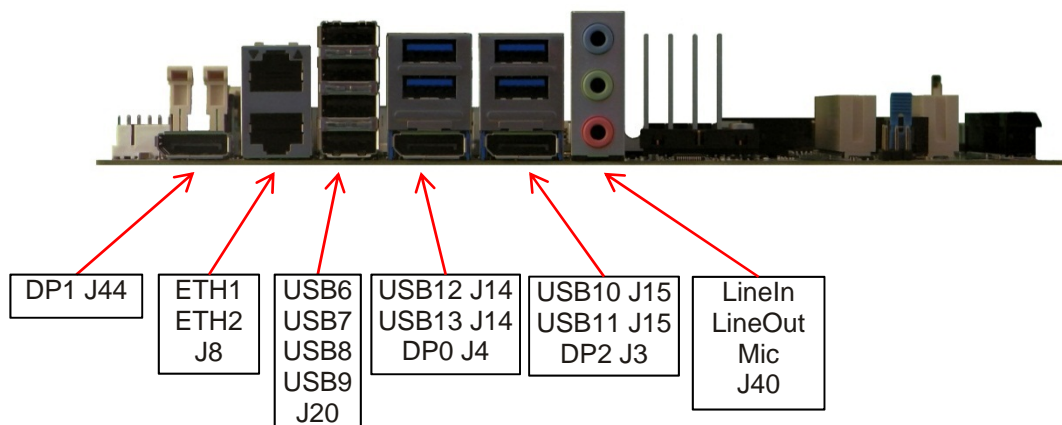
5   Connector Signal Definitions

The following sections provide pin definitions and detailed description of all onboard connectors.
The connector definitions follow the following notation:

Column Name	Description
Pin	Shows the pin numbers in the connector.
Signal	The mnemonic name of the signal at the current pin. The notation "#" states that the signal is active low.

Type	AI: Analogue Input
	AO: Analogue Output
	I: Digital Input
	IO: Digital Input / Output
	IOD: Input / Open Drain output
	O: Digital Output
	DSO: Differential Signaling Output with complementary signals on two paired wires
	DSI: Differential Signaling Input with complementary signals on two paired wires
	DSIO: Differential Signaling Input / Output (combined DSO and DSI)
	PWR: PoWeR supply or ground reference pins
	NC: Pin Not Connected
	Additional notations:
	          -5.0 +5.0V signal voltage level, e.g. I-5.0
	          -3.3 +3.3V signal voltage level, e.g. O-3.3
	          -1.8 +1.8V signal voltage level, e.g. IO-1.8

Ioh/Iol	Ioh: Typical current in mA flowing out of an output pin through a grounded load while the output voltage has high level. Iol: Typical current in mA flowing into an output pin from a VCC connected load while the output voltage has low level.

The abbreviation tbd is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

6   Rear IO Connectors

6.1   DisplayPort (DP0/DP1/DP2) (J4/J43/J3)

The DP (DisplayPort) connectors are based on standard DP type Foxconn 3VD11203-H7AB-4H or similar.
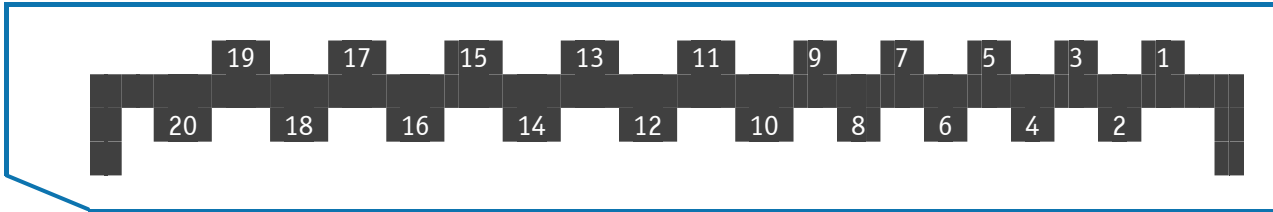
Pin	Signal	Description	Type	Note
1	Lane 0 (p)		LVDS	
2	GND		PWR	
3	Lane 0 (n)		LVDS	
4	Lane 1 (p)		LVDS	
5	GND		PWR	
6	Lane 1 (n)		LVDS	
7	Lane 2 (p)		LVDS	
8	GND		PWR	
9	Lane 2 (n)		LVDS	
10	Lane 3 (p)		LVDS	
11	GND		PWR	
12	Lane 3 (n)		LVDS	
13	Config1	Aux or DDC selection	I	Internally pull down (1Mohm). Aux channel on pin 15/17 selected as default (when NC) DDC channel on pin 15/17, If HDMI adapter used (3.3V)
14	Config2	(Not used)	O	Internally connected to GND
15	Aux Ch (p)	Aux Channel (+) or DDC Clk		AUX (+) channel used by DP DDC Clk used by HDMI
16	GND		PWR	
17	Aux Ch (n)	Aux Channel (-) or DDC Data		AUX (-) channel used by DP DDC Data used by HDMI
18	Hot Plug		I	Internally pull down (100Kohm).
19	Return		PWR	Same as GND
20	3.3V		PWR	Fused by 1.5A resetable PTC fuse, common for DP0 and DP1

Note: **To protect the external power lines of peripheral devices make sure that**
          - the wires have the right diameter to withstand the maximum available current.
          - to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

The 3 DisplayPorts (DP0, DP1 and DP2) can be used in a 3 independent display configuration. By use of DP Adapter Converters it is possible to implement a mix of DP, VGA, HDMI and DVI-D outputs and still support 3 independent displays configuration.

Available DP adapters:

| DP to VGA | DP to HDMI | DP to DVI-D |
| PN 1045-5779 | PN 1045-5781 | PN 1045-5780 |

DP Extention Cable:

In order to prevent mechanical conflicts the above DP adapters can be connected to DP#0, DP#1 and DP#2 via the 1051-7619 Cable DP Extender cable 200mm.

The DP to VGA adapter is an "active" converter, meaning that seen from the graphics controller it looks like a DP. The HDMI and DVI converters are passive converters, meaning that they inform the graphics controller about its type and the graphics controller then replace the DP signals with TMDS signals (used in HDMI and DVI).

The HDMI interface supports the HDMI 1.4a specification including audio codec. Limitations to the resolution apply: 2048x1536 (VGA), 1920x1200 (HDMI and DVI).

Four independent (simultaneously) displays (without using PCIe Graphics cards) is a possible configuration under the following conditions:

1. A DP-PCIe passive card or DP-DVI passive card must be used in the outermost PCIe slot.
2. All DP must be converted to DVI-D or HDMI via passive adapters like above adapters.
3. Two of the panels must have the same timing (as if two panels are of the exact same type).

6.2   USB3.0 Connectors (USB10/USB11/USB12/USB13) (J15/J15/J14/J14)

The USB3.0 connectors are based on standard USB3.0 connectors type Lotes ABA-USB-104-K01 or similar.

Thease 4 USB3.0 ports are controlled by the xHCI controllers supporting USB3.0, USB2.0 and USB 1.1, Super-Speed (5.0Gbps), High-Speed (480Mbps), Full-Speed (12Mbps) and Low-Speed (1.5Mbps)

USB Ports 10 and 11 (mounted on top of the DP#2 port):

Note	Type	Signal	PIN				Signal	Type	Note
	DSIO-3.3		USB10-	USB10+				DSIO-3.3	
1	PWR	5V/SB5V	1	2	3	4	GND	PWR	
	DSIO-3.3	RX10-	5	6	7	8	9 TX10+	DSIO-3.3	
	DSIO-3.3		RX10+		TX10-			DSIO-3.3	
	PWR		GND						
	DSIO-3.3		USB11-	USB11+				DSIO-3.3	
1	PWR	5V/SB5V	1	2	3	4	GND	PWR	
	DSIO-3.3	RX11-	5	6	7	8	9 TX11+	DSIO-3.3	
	DSIO-3.3		RX11+		TX11-			DSIO-3.3	
	PWR		GND						

Signal	Description
USB10+ USB10- RX10+ RX10- TX10+ TX10- USB11+ USB11- RX11+ RX11- TX11+ TX11-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external device. SB5V is supplied during powerdown to allow wakeup on device activity. Protected by current limited power distribution switch,1A for each port.

USB Ports 12 and 13 (mounted on top of the DP#0 port):

Note	Type	Signal	PIN				Signal	Type	Note
	DSIO-3.3		USB12-	USB12+				DSIO-3.3	
1	PWR	5V/SB5V	1	2	3	4	GND	PWR	
	DSIO-3.3	RX12-	5	6	7	8	9 TX12+	DSIO-3.3	
	DSIO-3.3		RX12+		TX12-			DSIO-3.3	
	PWR		GND						
	DSIO-3.3		USB13-	USB13+				DSIO-3.3	
1	PWR	5V/SB5V	1	2	3	4	GND	PWR	
	DSIO-3.3	RX13-	5	6	7	8	9 TX13+	DSIO-3.3	
	IO		RX13+		TX13-			DSIO-3.3	
	PWR		GND						

Signal	Description
USB12+ USB12- RX12+ RX12- TX12+ TX12- USB13+ USB13- RX13+ RX13- TX13+ TX13-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external device. SB5V is supplied during powerdown to allow wakeup on device activity. Protected by current limited power distribution switch,1A for each port.

Notes: **In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.**

The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 1000mA.

Do not supply external USB devices with higher power dissipation through these pinsTo protect the external power lines of peripheral devices make sure that
  - the wires have the right diameter to withstand the maximum available current.
  - to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

6.3   Ethernet Connectors (ETH1/ETH2) (J8)

The KTA75 supports two 10/100/1000Mb Ethernet RJ45 connetors in a stacked dual LAN connector, type Ude RMT-123AGF1F or sililar. Both ports are driven by Intel® Pearsonville WGI211AT PCI Express controller.

Ethernet connector 1 (ETH1) is mounted above Ethernet connector 2 (ETH2).

Signal	PIN	Note
LED1		LED Lights when ETH1 Link, Flashing when activity
MDIO+		
MDIO-		
MDI1+		
MDI2+		
MDI2-		
MDI1-		
MDI3+		
MDI3-		
LED2		LED Lights when ETH2 Link, Flashing when activity
ETH1	8 7 6 5 4 3 2 1	
ETH2	1 2 3 4 5 6 7 8	
MDIO+		
MDIO-		
MDI1+		
MDI2+		
MDI2-		
MDI1-		
MDI3+		
MDI3-		

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

Signal	Description
MDI[0]+ / MDI[0]-	MDI mode: first pair in 1000Base-T (i.e. the BI_DA+/- pair), transmit pair in 10/100Base-T. MDI crossover mode: acts as the BI_DB+/- pair, receive pair in 10/100Base-TX.
MDI[1]+ / MDI[1]-	MDI mode: second pair in 1000Base-T (i.e. the BI_DB+/- pair), receive pair in 10/100Base-T. MDI crossover mode: acts as the BI_DA+/- pair, transmit pair in 10/100Base-T.
MDI[2]+ / MDI[2]-	MDI mode: third pair in 1000Base-T (i.e. the BI_DC+/- pair). MDI crossover mode: acts as the BI_DD+/- pair.
MDI[3]+ / MDI[3]-	MDI mode: fourth pair in 1000Base-T (i.e. the BI_DD+/- pair). MDI crossover mode: acts as the BI_DC+/- pair.

Note: MDI = Media Dependent Interface.

6.4   USB x4 Stack Connector (USB6/USB7/USB8/USB9) (J20)

USB Ports 6, 7, 8 and 9 are mounted in a single stack in the IO Area type Foxconn UB11123-Q8DF-4F or similar. The USB ports are controlled by a single set of OHCI and EHCI controllers (also shared by USB5).

The OHCI controllers support USB1.1, Full-Speed (12Mbps) and Low-Speed (1.5Mbps).
The EHCI controllers support USB2.0, High-Speed (480Mbps).

Note	Type	Signal	PIN				Signal	Type	Note
	PWR	5V/SB5V	1	2	3	4	GND	PWR	
	DSIO-3.3	USB6-					USB6+	DSIO-3.3	
	PWR	5V/SB5V	1	2	3	4	GND	PWR	
	DSIO-3.3	USB7-					USB7+	DSIO-3.3	
	PWR	5V/SB5V	1	2	3	4	GND	PWR	
	DSIO-3.3	USB8-					USB8+	DSIO-3.3	
	PWR	5V/SB5V	1	2	3	4	GND	PWR	
	DSIO-3.3	USB9-					USB9+	DSIO-3.3	

Signal	Description
USB6+ USB6- USB7+ USB7- USB8+ USB8- USB9+ USB9-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by individual resettable 1A fuse.

Notes: *In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.*

The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 1000mA.

Do not supply external USB devices with higher power dissipation through these pinsTo protect the external power lines of peripheral devices make sure that
   - the wires have the right diameter to withstand the maximum available current.
   - to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

6.5   Audio Interface (J40)

The on-board Audio circuit, based on Via VT1708S, implements 7.1+2 Channel High Definition Audio with UAA (Universal Audio Architecture), featuring five 24-bit stereo DACs and three 20-bit stereo ADCs. The Following Audio connector is available in IO Area.

Audio Speakers, Line-in and Microphone are available in the stacked audiojack connector type Lotes ABA-JAK-028-K03

	Signal	Type	Note
TIP	LINE1-L	IA	
RING	LINE1-R	IA	
SLEEVE	GND	PWR	
TIP	FRONT-OUT-L	OA	
RING	FRONT-OUT-R	OA	
SLEEVE	GND	PWR	
TIP	MIC1-L	IA	
RING	MIC1-R	IA	
SLEEVE	GND	PWR	
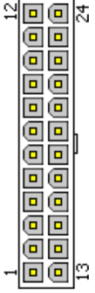
Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
MIC1-L	Microphone 1 - Left	Shared with Audio Header
MIC1-R	Microphone 1 - Right	Shared with Audio Header
LINE1-L	Line 1 signal - Left	Shared with Audio Header
LINE1-R	Line 1 signal - Right	Shared with Audio Header

7   Pin Connectors

7.1   24-pin ATX-BTX Power Connector (J17)

The KTA75 boards are designed to be supplied from a standard ATX (or BTX) power supply. Use of BTX supply is not required for operation, but may be required to drive high-power PCIe cards.

ATX-BTX Power Connector (J17):

Header	Note	Type	Signal	PIN		Signal	Type	Note
		PWR	3V3	12	24	GND	PWR	
		PWR	+12V	11	23	5V	PWR	
		PWR	+12V	10	22	5V	PWR	
		PWR	SB5V	9	21	5V	PWR	
		I	P_OK	8	20	-5V	PWR	1
		PWR	GND	7	19	GND	PWR	
		PWR	5V	6	18	GND	PWR	
		PWR	GND	5	17	GND	PWR	
		PWR	5V	4	16	PSON#	OC	
		PWR	GND	3	15	GND	PWR	
		PWR	3V3	2	14	-12V	PWR	
		PWR	3V3	1	13	3V3	PWR	
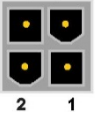
Note 1: -5V supply is not used on-board.

See chapter "Power Consumption" regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification version 2.2).

Signal	Description
P_OK	P_OK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the undervoltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the undervoltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, P_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the *ATX12V Power SupplyDesign Guide*. It is strongly recommended to use an ATX or BTX supply in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised on-board.
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

7.2   4-pin 12V Power Connector (J19)

The KTA75/Flex has an internal power input connector for supplying voltage in the range from +11.4V to +12.6V. The power connector is a 4 pin 12V ATX connector type Lotes ABA-POW-003-K02 or similar.

Header	Pin	Signal	Description
	1	GND	Ground
	2	GND	Ground
	3	12V	Power supply +12V
	4	12V	Power supply +12V

Warning: Hot Plugging power supply is not supported. Hot plugging might damage the board.

Note 1: Use of the 4-pin ATX+12V Power Connector is required for operation of all KTA75 board versions.

Notes: *To protect the external power lines of peripheral devices make sure that*
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.

Alternatively the DC Power External Connector can be used

7.3   Audio Header Connector (J41)

The Audio Header connector is a 26 pin connector type Molex 87832-2620 or similar.

Note	Type	Signal	PIN		Signal	Type	Note
	AO	LFE-OUT	1	2	CEN-OUT	AO	
	PWR	AAGND	3	4	AAGND	PWR	
1	AO	FRONT-OUT-L	5	6	FRONT-OUT-R	AO	1
	PWR	AAGND	7	8	AAGND	PWR	
	AO	REAR-OUT-L	9	10	REAR-OUT-R	AO	
	AO	SIDE-OUT-L	11	12	SIDE-OUT-R	AO	
	PWR	AAGND	13	14	AAGND	PWR	
1	AI	MIC1-L	15	16	MIC1-R	AI	1
	PWR	AAGND	17	18	AAGND	PWR	
1		LINE1-L	19	20	LINE1-R		1
	NC	NC	21	22	AAGND	PWR	
	PWR	GND	23	24	NC	NC	
	O	SPDIF-OUT	25	26	GND	PWR	

Note 1: Shared with Audio Stack connector (in Rear IO area).

Signal	Description
FRONT-OUT-L	Front Speakers (Speaker Out Left).
FRONT-OUT-R	Front Speakers (Speaker Out Right).
REAR-OUT-L	Rear Speakers (Surround Out Left).
REAR-OUT-R	Rear Speakers (Surround Out Right).
SIDE-OUT-L	Side speakers (Surround Out Left)
SIDE-OUT-R	Side speakers (Surround Out Right)
CEN-OUT	Center Speaker (Center Out channel).
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).
NC	No connection
MIC1	MIC Input 1
LINE1	Line 1 signals
F-SPDIF-OUT	S/PDIF Output
AAGND	Audio Analogue ground

Available cable kit:
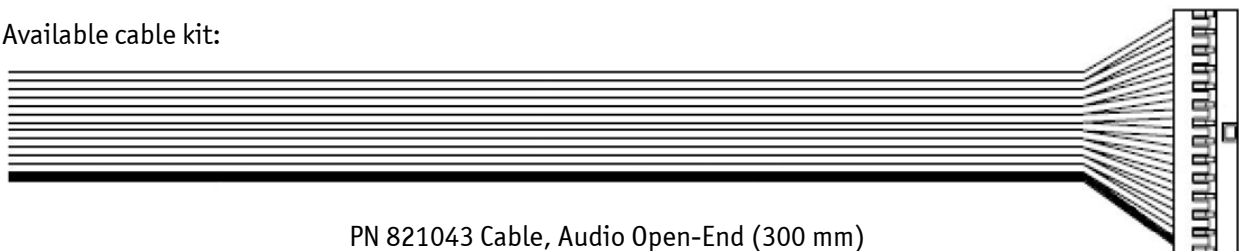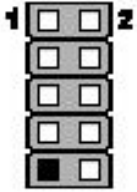
PN 821043 Cable, Audio Open-End (300 mm)

7.4 USB4/5 Connector (J16)

USB Ports 4 and 5 are available via Pin Row connector type Foxconn HS1105F-RNP9 or similar.

The USB4 port is controlled by a set of OHCI and EHCI controllers (also shared by USB0/1/2).
The USB5 port is controlled by a set of OHCI and EHCI controllers (also shared by USB6/7/8/9).

The OHCI controllers support USB1.1, Full-Speed (12Mbps) and Low-Speed (1.5Mbps).
The EHCI controllers support USB2.0, High-Speed (480Mbps).

Header	Pin	Signal	Description	Type
	1	5V/SB5V	5V (always) protected by separate 1A resettable fuse	PWR
	2	5V/SB5V	5V (always) protected by separate 1A resettable fuse	PWR
	3	USB4-	Differential pair 4 -	DSIO-3.3
	4	USB5-	Differential pair 5 -	DSIO-3.3
	5	USB4+	Differential pair 4 +	DSIO-3.3
	6	USB4+	Differential pair 5 +	DSIO-3.3
	7	GND	Ground	PWR
	8	GND	Ground	PWR
	-		(pin not mounted -Used for keying)	
	10	KEY		NC

Notes: **In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.**

The contacts for USB devices are protected and suitable to supply USB devices with a maximum input current of 1000mA.

Do not supply external USB devices with higher power dissipation through these pinsTo protect the external power lines of peripheral devices make sure that
- the wires have the right diameter to withstand the maximum available current.
- to enclosure of the peripheral device fulfills the fire-protecting conditions of IEC/EN 60950.
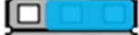
Available cable kit:
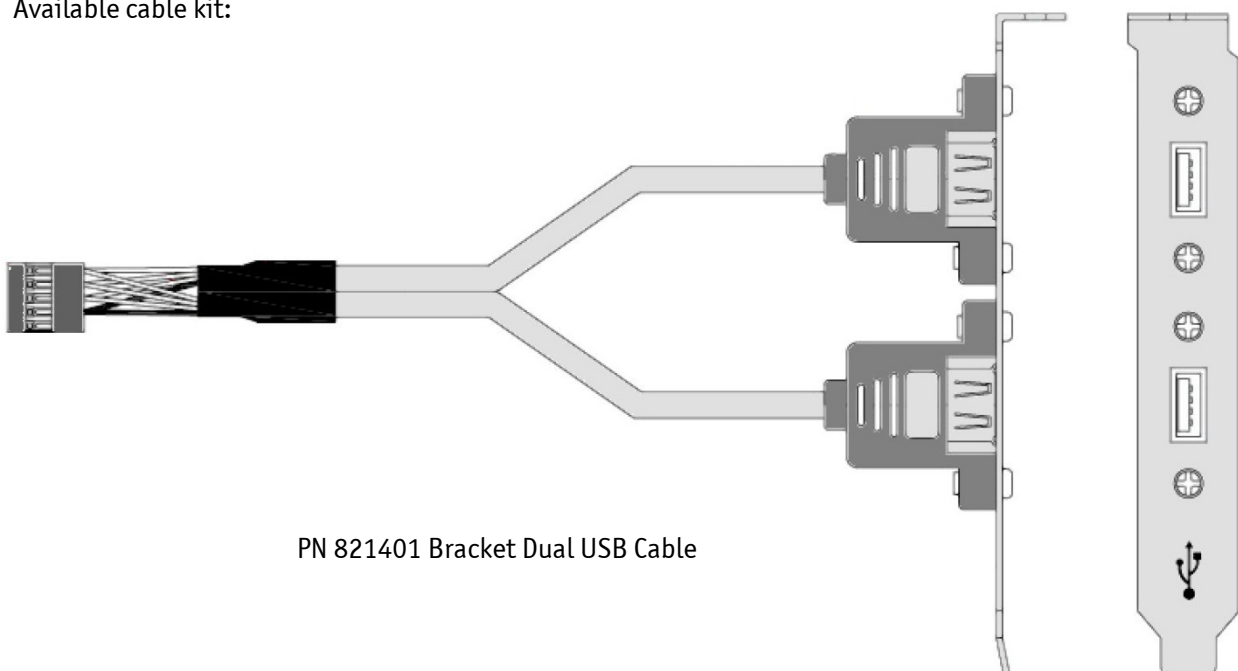
PN 821401 Bracket Dual USB Cable

7.5   Jumper area (J34, J35, J36, J37)

The KTA75 has a jumper area containing pin connectors 2.54mm pitch, for up to four jumpers, but normally only one jumper is used (jumper in the J34 pin 2-3 position, as indicated below).

Function	J#	Jumper in position 1-2	Pin 1 2 3	Jumper in position 2-3
Always On	J37	-		Always On
Clear CMOS	J34	Clear CMOS		Normal (Default)
Audio Short circuit test	J36	Front Right		Front Left
Not mounted	J35	-		-

Always On: is PT not supported.

(None): Not mounted on final version of board. Only mounted on Early Field Test versions of KTA75.

Clear CMOS: is used to erase all customised BIOS settings located in the CMOS RAM storage. If the board has a booting problem or is unstabile, then Clearing CMOS by moving the Jumper from default position to the Clear CMOS position for approx. 10 sec. might solve the problem.

> ⚠️ **Warning**
>
> Don't leave the Clear CMOS jumper in position 1-2, otherwise if power is disconnected, the battery will fully deplete within a few weeks.
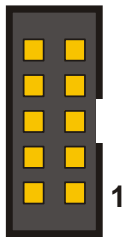
Audio Short Circuit Test: is only used in manufacturing test. No jumper should be installed.

7.6   SPI Connector (J21)

The KTA75 provides one synchronous full duplex SPI (Serial Peripheral Interface) Bus in a 10 pin header connector. The connector is type Pinrex 512-90-10GBE5 or similar.

Two things should be considered:

1.   An onboard SPI^{TM} flash coexists on the same interface lines. You must disable this component with a 3.3V power connection to the ADDIN signal (e.g. a short circuit jumper between pin 2 and 4).

2.   The four SPI^{TM} lines are protected with an additional bus driver and the ISOLATE# signal controls the output enable pin. For normal operation this signal should be high.

Header	Pin	Signal	Description	Type
	1	SPI_CLK	SPI clock	O-3.3
	2	3.3V	Power +3.3V	PWR
	3	SPI_CS#	SPI slave select, active low	O-3.3
	4	ADDIN	Disable onboard SPI flash	I-3.3
	5	RSVD	Reserved (10k pullup to 3.3V)	PWR
	6	N.C.	Not connected	NC
	7	SPI_MOSI	SPI master output, Slave Input	IO-3.3
	8	ISOLATE#	Disable the SPI interface	I-3.3
	9	SPI_MISO	SPI master input, Slave Output	IO-3.3
	10	GND	Ground	PWR

Signal	Further description
SB3V3	3.3V Standby Voltage power line. Normally output power, but when Motherboard is turned off then the on-board SPI Flash can be 3.3V power sourced via this pin.
ISOLATE#	The ISOLATE# input, active low, is normally NC, but must be connected to GND when loading SPI flash. Power Supply to the Motherboard must be turned off when loading SPI flash. The pull up resistor is connected via diode to 5VSB.

7.7   COM1/COM2 (J23/J22)

Two serial ports provide asynchronous serial communication via RS-232 interfaces. The connector is type Pinrex 512-90-10GBE5 or similar.

The pinout of Serial ports COM1 and COM2 is as follows:

Note	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Note
-		I	DCD	1	2	DSR	I	-	
-		I	RxD	3	4	RTS	O		
		O	TxD	5	6	CTS	I	-	
		O	DTR	7	8	RI	I	-	
-		PWR	GND	9	10	5V	PWR	-	1

Note 1: The COM1 and COM4 5V supply is fused with a common 1.1A resettable fuse.

The typical definition of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem etc. is ready to establish a communications link.
RTS	Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.

Available cable kit (DB9 adapter cables):
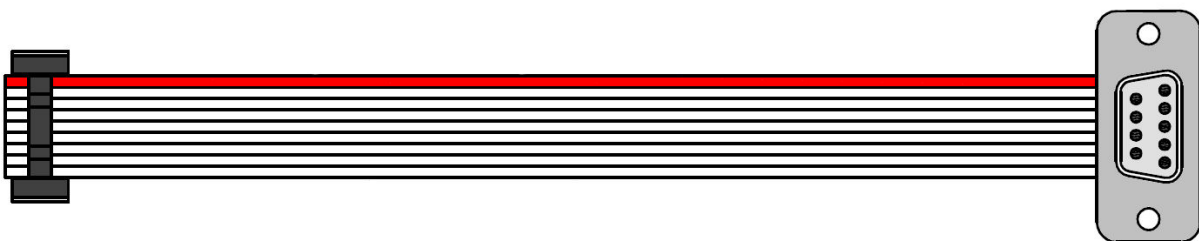
PN 821017 - 100 mm or PN 821016 - 200 mm

7.8 LPC Connector (J29)

The LPC connector is unsupported. The connector is type Foxconn HC11101-P0 or similar.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1	2	GND				
	-	-	PWR	LPC FRAME#	3		KEY				
				LPC RST#	5	6	+5V				
				LPC AD3	7	8	LPC AD2				
				+3V3	9	10	LPC AD1				
				LPC AD0	11	12	GND				
				SMB_CLK	13	14	SMB_DATA				
				SB3V3	15	16	LPC SERIRQ				
				GND	17	18	CLKRUN#				
				SUS_STAT#	19	20	NC				

7.9   Front Panel Connector (J5)

The Front Panel connector is a 24 pin connector type Wieson G2120HT0038-016 or similar.

Note	Pull U/D	Ioh/ Iol	Type	Signal	PIN		Signal	Type	Ioh/ Iol	Pull U/D	Note
	-	-	PWR	USB0_5V	1	2	USB1_5V	PWR	-	-	
	-	-		USB0-	3	4	USB1-		-	-	
	-	-		USB0+	5	6	USB1+		-	-	
	-	-	PWR	GND	7	8	GND	PWR	-	-	
	-	-	NC	NC	9	10	LINE2-L		-	-	
	-	-	PWR	+5V	11	12	+5V	PWR	-	-	
	-	25/25mA	O	SATA_LED#	13	14	SUS_LED	O	7mA	-	
	-	-	PWR	GND	15	16	PWRBTN_IN#	I		1K1	
	4K7	-	I	RSTIN#	17	18	GND	PWR	-	-	
	-	-	PWR	SB3V3	19	20	LINE2-R		-	-	
	-	-	PWR	AGND	21	22	AGND	PWR	-	-	
	-	-	AI	MIC2-L	23	24	MIC2-R	AI	-	-	

Signal	Description
USB0_5V/USB1_5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by independed resettable 1.1A fuse.
USB0+/USB0-	Universal Serial Bus Port 0 Differentials: Bus Data/Address/Command Bus.
USB1+/USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A if using IDC connector or 2A if using crimp terminals .
SATA_LED#	SATA Activity LED (active low signal). 3V3 output when passive.
SUS_LED	Suspend Mode LED (active high signal). Output 3.3V via 470Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for a minimum 16ms, the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
LINE2	Line2 is second stereo Line signals
MIC2	MIC2 is second stereo microphone input.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

Note: In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.
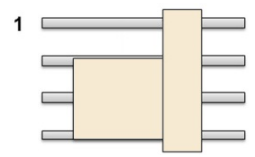
Available cable kit:
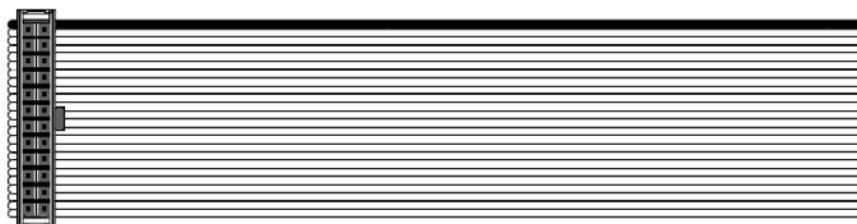
PN 821042 Cable Front Panel Open-End, 300 mm

7.10   CPU/System Fan Connectors (J25, J24)

The CPU Fan connector and the System Fan connector are identical 4 pin type connectors. The type is Tyco 1470947-1 or similar.

Header	Pin	Signal	Description	Type
	1	PWM	PWM output	0-3.3
	2	TACHO	Tacho signal (open drain)	I
	3	12V	Power +12V	PWR
	4	GND	Ground	PWR

Signal	Description
PWM	PWM is output signal used to control the fan speed (only for 4-wire Fans).
Tacho	Tarcho input signal is used to monitor the rotation speed RPM (Rotation Per Minute). Prepared for two pulses per turn.

7.11   Feature Connector (J26)

The Feature Connector is a 44 pin connector, 2 mm pitch, type Foxconn HS5422F or similar.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN		Signal	Type	Ioh/Iol	Pull U/D	Note
2	2M/	-	I	CASE_OPEN#	1	2	SMBC		/4mA	10K/	1
	-	25/25mA	O	S5#	3	4	SMBD		/4mA	10K/	1
	-	25/25mA	O	PWR_OK	5	6	EXT_BAT	PWR	-	-	
4	-		O	FAN3OUT	7	8	FAN3IN	I	-	10K/	4
	-	-	PWR	SB3V3	9	10	SB5V	PWR	-	-	
	-		IOT	GPIO0	11	12	GPIO1	IOT		-	
	-		IOT	GPIO2	13	14	GPIO3	IOT		-	
	-		IOT	GPIO4	15	16	GPIO5	IOT		-	
	-		IOT	GPIO6	17	18	GPIO7	IOT		-	
	-	-	PWR	GND	19	20	GND	PWR	-	-	
	-		I	GPIO8	21	22	GPIO9	I		-	
3	-		NC	GPIO10	23	24	GPIO11	NC		-	3
	-		I	GPIO12	25	26	GPIO13	IOT		-	
	-		IOT	GPIO14	27	28	GPIO15	IOT		-	
	-		IOT	GPIO16	29	30	GPIO17	NC		-	3
	-	-	PWR	GND	31	32	GND	PWR	-	-	
	-	8/8mA	O	EGCLK	33	34	EGCS#	O	8/8mA	-	
	-	8/8mA		EGAD	35	36	TMA0	O			
	-		PWR	+12V	37	38	GND	PWR	-	-	
4	-		O	FAN4OUT	39	40	FAN4IN	I	-	10K/	4
	-	-	PWR	GND	41	42	GND	PWR	-	-	
	-	-	PWR	GND	43	44	S3#	O	25/25mA	-	

Notes: **1**. Pull-up to SB3V3.
2. Pull-up to on-board Battery.
3. Not connected, used for onboard feature.
4. Not supported.

Available cable kit:
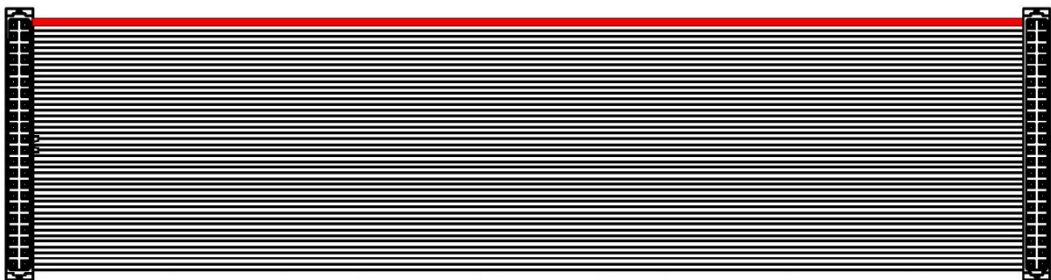
PN 1052-5885 Cable, Feature 44pol 1 to1, 300mm

Signal	Description
CASE_OPEN# *	CASE OPEN, used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not required.
SMBC	SMBus Clock signal
SMBD	SMBus Data signal
S3#	S3 sleep mode, active low output, optionally used to deactivate external system.
S5#	S5 sleep mode, active low output, optionally used to deactivate external system.
PWR_OK	PoWeR OK, signal is high if no power failures are detected. (This is not the same as the P_OK signal generated by ATX PSU).
EXT_BAT *	(EXTernal BATtery) option for connecting + terminal of an external primary cell battery (2.5 - 3.47 V) (– terminal connected to GND). The external battery is protected against charging and can be used with/without the on-board battery installed.
FAN3OUT	Not Supported
FAN3IN	Not Supported
FAN4OUT	Not Supported
FAN4IN	Not Supported
SB3V3	+3.3V StandBy voltage, max. load 1 Amp
SB5V	+5V StandBy voltage
GPIO0..17 *	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KT-API-V2 (Application Programming Interface). GPIO10, GPIO11 and GPIO17 are not supported (not connected).
EGCLK *	Extend GPIO Clock signal
EGAD *	Extend GPIO Address Data signal
EGCS# *	Extend GPIO Chip Select signal, active low
TMA0	Timer Output
+12V	+12V, max. load 1 Amp.

(*) = Not verified.

Available Temperature Sensor cable kit (for System Fan Temperature Cruise, selected in BIOS):

Based on Maxim DS18B20, Accurate to ±0.5ºC over the range of -10ºC to +85ºC
Feature connector 3.3V (Pin 9), GND (Pin 19) and GPIO16 (Pin 29)
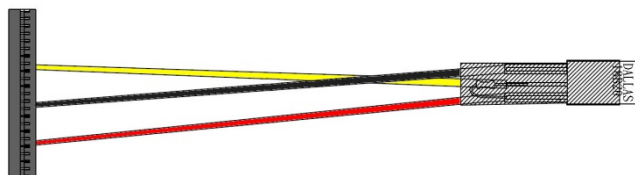
PN1053-4925 Cable Temperature Sensor - 44P, 400 mm

GPIO in more details:

The GPIO's are controlled via the ITE IT8516F Embedded Controller. Each GPIO has 100pF to ground, clamping Diode to 3V3 and has multiplexed functionality. Some pins can be DAC (Digital to Analogue Converter output), PWM (Pulse Width Modulated signal output), ADC (Analogue to Digital Converter input), TMRI (Timer Counter Input), WUI (Wake Up Input), RI (Ring Indicator Input) or some special function.

Signal	IT8516F pin name	Type	Description
GPIO0	DAC0/GPJ0	AO/IOS	
GPIO1	DAC1/GPJ1	AO/IOS	
GPIO2	DAC2/GPJ2	AO/IOS	
GPIO3	DAC3/GPJ3	AO/IOS	
GPIO4	PWM2/GPA2	O8/IOS	
GPIO5	PWM3/GPA3	O8/IOS	
GPIO6	PWM4/GPA4	O8/IOS	
GPIO7	PWM5/GPA5	O8/IOS	
GPIO8	ADC0/GPI0	AI/IS	
GPIO9	ADC1/GPI1	AI/IS	
GPIO10	ADC2/GPI2	AI/IS	Reserved, used for System Temperature
GPIO11	ADC3/GPI3	AI/IS	Reserved, used for +12V monitoring
GPIO12	ADC4/WUI28/GPI4	AI/IS/IS	
GPIO13	RI1#/WUI0/GPD0	IS/IS/IOS	
GPIO14	RI2#/WUI1/GPD1	IS/IS/IOS	
GPIO15	TMRI0/WUI2/GPC4	IS/IS/IOS	
GPIO16	TMRI1/WUI3/GPC6	IS/IS/IOS	Optionally for Cable Temperature sensor
GPIO17	L80HLAT/BA0/WUI24/GPE0	O4/O4/IS/IOS	Reserved, used for Sync

Feature Break-out board:
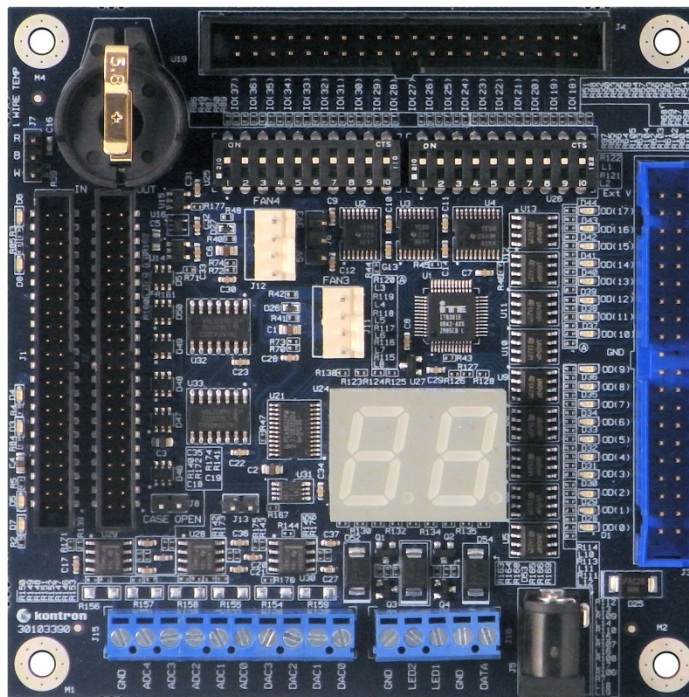
PN 820978 Feature BOB (Break-Out-Board)

7.12 KBD/MSE (J27)

Attachment of a PS/2 keyboard/mouse can be done through the pinrow connector KBDMSE (J27) type Molex 22-23-2061 or similar.

Both interfaces utilize open-drain signalling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resettable fuse.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOD	/14mA	2K7	
2	KBDDAT	IOD	/14mA	2K7	
3	MSCLK	IOD	/14mA	2K7	
4	MSDAT	IOD	/14mA	2K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

Available cable kit:
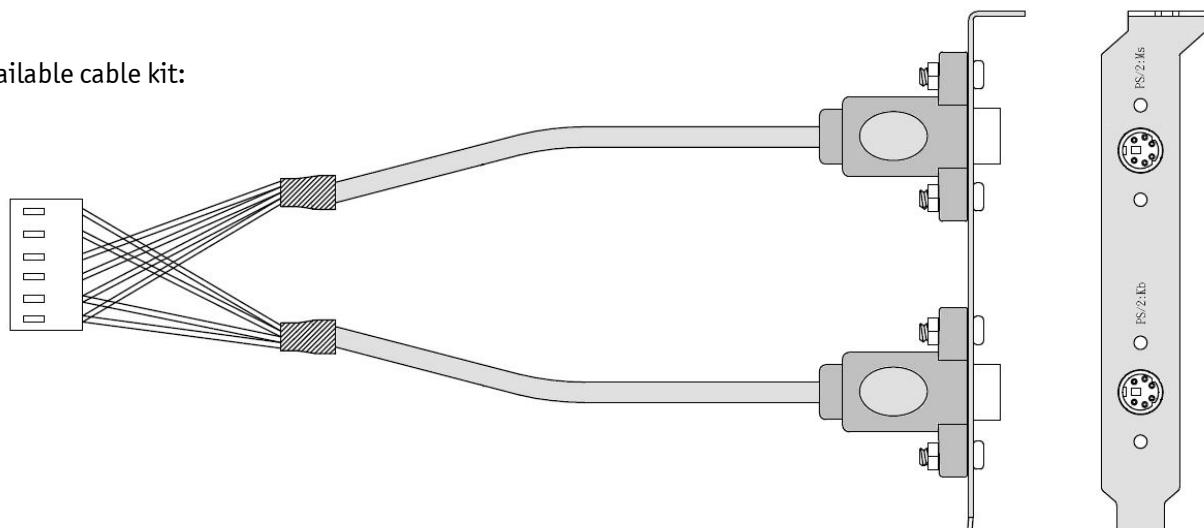
PN 1053-2384 Bracket Cable 6-Pin to PS2-Kbd-Mse

8   Slot Connectors (PCI-Express, miniPCIe, SATA, mSATA)

8.1   PCIex16 (J7)

The PCIex16 (16-lane PCI Express) is available through a PCIe x16 slot and support PCIe 2.0. The slot can be used for external PCI Express cards inclusive graphics card and dedicated TMDS passive card. The slot is located nearest the edge of the board. Maximum theoretical bandwidth using 16 lanes is 8 GB/s.

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	GND via 0 Ohm		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	SCL5-AUX5P		
		GND	B7	A7	SCA5-AUX5N		
		+3V3	B8	A8	NC		
		DP5 HP	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLKP		
		PEG_TXP[0]	B14	A14	PCIE_x16 CLKN		
		PEG_TXN[0]	B15	A15	GND		
		GND	B16	A16	PEG_RXP[0]		
		CLKREQ	B17	A17	PEG_RXN[0]		
		GND	B18	A18	GND		
		PEG_TXP[1]	B19	A19	NC		
		PEG_TXN[1]	B20	A20	GND		
		GND	B21	A21	PEG_RXP[1]		
		GND	B22	A22	PEG_RXN[1]		
		PEG_TXP[2]	B23	A23	GND		
		PEG_TXN[2]	B24	A24	GND		
		GND	B25	A25	PEG_RXP[2]		
		GND	B26	A26	PEG_RXN[2]		
		PEG_TXP[3]	B27	A27	GND		
		PEG_TXN[3]	B28	A28	GND		
		GND	B29	A29	PEG_RXP[3]		
		NC	B30	A30	PEG_RXN[3]		
		CLKREQ	B31	A31	GND		
		GND	B32	A32	NC		
		PEG_TXP[4]	B33	A33	NC		
		PEG_TXN[4]	B34	A34	GND		
		GND	B35	A35	PEG_RXP[4]		

		GND	B35	A35	PEG_RXP[4]		
		GND	B36	A36	PEG_RXN[4]		
		PEG_TXP[5]	B37	A37	GND		
		PEG_TXN[5]	B38	A38	GND		
		GND	B39	A39	PEG_RXP[5]		
		GND	B40	A40	PEG_RXN[5]		
		PEG_TXP[6]	B41	A41	GND		
		PEG_TXN[6]	B42	A42	GND		
		GND	B43	A43	PEG_RXP[6]		
		GND	B44	A44	PEG_RXN[6]		
		PEG_TXP[7]	B45	A45	GND		
		PEG_TXN[7]	B46	A46	GND		
		GND	B47	A47	PEG_RXP[7]		
		CLKREQ	B48	A48	PEG_RXN[7]		
		GND	B49	A49	GND		
		PEG_TXP[8]	B50	A50	NC		
		PEG_TXN[8]	B51	A51	GND		
		GND	B52	A52	PEG_RXP[8]		
		GND	B53	A53	PEG_RXN[8]		
		PEG_TXP[9]	B54	A54	GND		
		PEG_TXN[9]	B55	A55	GND		
		GND	B56	A56	PEG_RXP[9]		
		GND	B57	A57	PEG_RXN[9]		
		PEG_TXP[10]	B58	A58	GND		
		PEG_TXN[10]	B59	A59	GND		
		GND	B60	A60	PEG_RXP[10]		
		GND	B61	A61	PEG_RXN[10]		
		PEG_TXP[11]	B62	A62	GND		
		PEG_TXN[11]	B63	A63	GND		
		GND	B64	A64	PEG_RXP[11]		
		GND	B65	A65	PEG_RXN[11]		
		PEG_TXP[12]	B66	A66	GND		
		PEG_TXN[12]	B67	A67	GND		
		GND	B68	A68	PEG_RXP[12]		
		GND	B69	A69	PEG_RXN[12]		
		PEG_TXP[13]	B70	A70	GND		
		PEG_TXN[13]	B71	A71	GND		
		GND	B72	A72	PEG_RXP[13]		
		GND	B73	A73	PEG_RXN[13]		
		PEG_TXP[14]	B74	A74	GND		
		PEG_TXN[14]	B75	A75	GND		
		GND	B76	A76	PEG_RXP[14]		
		GND	B77	A77	PEG_RXN[14]		
		PEG_TXP[15]	B78	A78	GND		
		PEG_TXN[15]	B79	A79	GND		
		GND	B80	A80	PEG_RXP[15]		
		CLKREQ	B81	A81	PEG_RXN[15]		
		NC	B82	A82	GND		

8.2 PCIex4 (J6)

The PCIex4 (4-lane PCI Express) is available through a PCIe x16 slot and support PCIe 2.0. The slot can be used for external PCI Express cards inclusive graphics card. The slot is located nearest the CPU of the board. Maximum theoretical bandwidth using 4 lanes is 4 GB/s.

Note	Type	Signal	PIN		Signal	Type	Note
		+12V	B1	A1	GND via 0 ohm		
		+12V	B2	A2	+12V		
		+12V	B3	A3	+12V		
		GND	B4	A4	GND		
		SMB_CLK	B5	A5	NC		
		SMB_DATA	B6	A6	NC		
		GND	B7	A7	NC		
		+3V3	B8	A8	NC		
		NC	B9	A9	+3V3		
		SB3V3	B10	A10	+3V3		
		WAKE#	B11	A11	RST#		
		NC	B12	A12	GND		
		GND	B13	A13	PCIE_x16 CLK		
		PEG_TXP[0]	B14	A14	PCIE_x16 CLK#		
		PEG_TXN[0]	B15	A15	GND		
		GND	B16	A16	PEG_RXP[0]		
		CLKREQ	B17	A17	PEG_RXN[0]		
		GND	B18	A18	GND		
		PEG_TXP[1]	B19	A19	NC		
		PEG_TXN[1]	B20	A20	GND		
		GND	B21	A21	PEG_RXP[1]		
		GND	B22	A22	PEG_RXN[1]		
		PEG_TXP[2]	B23	A23	GND		
		PEG_TXN[2]	B24	A24	GND		
		GND	B25	A25	PEG_RXP[2]		
		GND	B26	A26	PEG_RXN[2]		
		PEG_TXP[3]	B27	A27	GND		
		PEG_TXN[3]	B28	A28	GND		
		GND	B29	A29	PEG_RXP[3]		
		NC	B30	A30	PEG_RXN[3]		
		CLKREQ	B31	A31	GND		
		GND	B32	A32	NC		
		NC	B33	A33	NC		
		NC	B34	A34	GND		
		GND	B35	A35	NC		
		GND	B36	A36	NC		
		NC	B37	A37	GND		
		NC	B38	A38	GND		

			B	A			
		GND	B39	A39	NC		
		GND	B40	A40	NC		
		NC	B41	A41	GND		
		NC	B42	A42	GND		
		GND	B43	A43	NC		
		GND	B44	A44	NC		
		NC	B45	A45	GND		
		NC	B46	A46	GND		
		GND	B47	A47	NC		
		CLKREQ	B48	A48	NC		
		GND	B49	A49	GND		
		NC	B50	A50	NC		
		NC	B51	A51	GND		
		GND	B52	A52	NC		
		GND	B53	A53	NC		
		NC	B54	A54	GND		
		NC	B55	A55	GND		
		GND	B56	A56	NC		
		GND	B57	A57	NC		
		NC	B58	A58	GND		
		NC	B59	A59	GND		
		GND	B60	A60	NC		
		GND	B61	A61	NC		
		NC	B62	A62	GND		
		NC	B63	A63	GND		
		GND	B64	A64	NC		
		GND	B65	A65	NC		
		NC	B66	A66	GND		
		NC	B67	A67	GND		
		GND	B68	A68	NC		
		GND	B69	A69	NC		
		NC	B70	A70	GND		
		NC	B71	A71	GND		
		GND	B72	A72	NC		
		GND	B73	A73	NC		
		NC	B74	A74	GND		
		NC	B75	A75	GND		
		GND	B76	A76	NC		
		GND	B77	A77	NC		
		NC	B78	A78	GND		
		NC	B79	A79	GND		
		GND	B80	A80	NC		
		CLKREQ	B81	A81	NC		
		NC	B82	A82	GND		

8.3   mPCIe connector (J38)

The mPCIe (mini PCI Express) port is PCIe 2.0 compliant and it supports USB (port USB2). The mPCI is PCIe 2.0 compliant.

Header	Pin	Signal	Description	Type	Pin	Signal	Description	Type
	1	Wake#	Wake event	I-3.3	2	3.3V	Power +3.3V	PWR
	3	N.C.	-	NC	4	Gnd	Ground	PWR
	5	N.C.	-	NC	6	1.5V	Power +1.5V	PWR
	7	Clkreq#	Clock request	I-3.3	8	N.C.	-	NC
	9	GND	Ground	PWR	10	N.C.	-	NC
	11	PE_Clk-	PCIe® clock-	DSO	12	N.C.	-	NC
	13	PE_Clk+	PCIe® clock+	DSO	14	N.C.	-	NC
	15	GND	Ground	PWR	16	N.C.	-	NC
	17	N.C.	-	NC	18	Gnd	Ground	PWR
	19	N.C.	-	NC	20	W_Disable#	Wireless disable	O-3.3
1	21	GND	Ground	PWR	22	PE_RST#	PCIe® reset	O-3.3
	23	PE_RX-	PCIe® receive-	DSI	24	3.3V	Power +3.3V	PWR
	25	PE_RX+	PCIe® receive+	DSI	26	Gnd	Ground	PWR
	27	Gnd	Ground	PWR	28	1.5V	Power +1.5V	PWR
	29	Gnd	Ground	PWR	30	I2C_Clk	I2C™ clock	O-3.3
	31	PE_TX-	PCIe® transmit-	DSO	32	I2C_Data	I2C™ data	IO-3.3
	33	PE_TX+	PCIe® transmit+	DSO	34	Gnd	Ground	PWR
	35	Gnd	Ground	PWR	36	USB2-	Diff. pair USB2 -	DSIO-3.3
	37	Gnd	Ground	PWR	38	USB2+	Diff. pair USB2 +	DSIO-3.3
	39	3.3V	Power +3.3V	PWR	40	Gnd	Ground	PWR
	41	3.3V	Power +3.3V	PWR	42	N.C.	-	NC
	43	Gnd	Ground	PWR	44	N.C.	-	NC
	45	N.C.	-	NC	46	N.C.	-	NC
	47	N.C.	-	NC	48	1.5V	Power +1.5V	PWR
	49	N.C.	-	NC	50	Gnd	Ground	PWR
	51	N.C.	-	NC	52	3.3V	Power +3.3V	PWR

8.4   mSATA/mPCIe Connector (J43)

The mSATA/mPCIe interface complies with SATA 3.0 and it supports USB (port USB2).

Header	Pin	Signal	Description	Type	Pin	Signal	Description	Type
	1	Wake#	Wake event	I-3.3	2	3.3V	Power +3.3V	PWR
	3	N.C.	-	NC	4	Gnd	Ground	PWR
	5	N.C.	-	NC	6	1.5V	Power +1.5V	PWR
	7	Clkreq#	Clock request	I-3.3	8	N.C.	-	NC
	9	Gnd	Ground	PWR	10	N.C.	-	NC
	11	PE_CLK-	PCIe® clock-	DSO	12	N.C.	-	NC
	13	PE_CLK+	PCIe® clock+	DSO	14	N.C.	-	NC
	15	Gnd	Ground	PWR	16	N.C.	-	NC
	17	N.C.	-	NC	18	Gnd	Ground	PWR
	19	N.C.	-	NC	20	W_Disable#	Wireless disable	O-3.3
	21	Gnd	Ground	PWR	22	PE_RST#	PCIe® reset	O-3.3
	23	SATA_RX+	S-ATA® receive+	DSI	24	3.3V	Power +3.3V	PWR
	25	SATA_RX-	S-ATA® receive-	DSI	26	Gnd	Ground	PWR
	27	Gnd	Ground	PWR	28	1.5V	Power +1.5V	PWR
	29	Gnd	Ground	PWR	30	I2C_Clk	I2C™ clock	IO-3.3
	31	SATA_TX-	S-ATA® transmit-	DSO	32	I2C_Data	I2C™ data	IO-3.3
	33	SATA_TX+	S-ATA® transmit+	DSO	34	Gnd	Ground	PWR
	35	Gnd	Ground	PWR	36	USB3-	Diff. pair USB3 -	DSIO-0.4V
	37	Gnd	Ground	PWR	38	USB3+	Diff. pair USB3 +	DSIO-0.4V
	39	3.3V	Power +3.3V	PWR	40	Gnd	Ground	PWR
	41	3.3V	Power +3.3V	PWR	42	N.C.	-	NC
	43	Gnd	Ground	PWR	44	N.C.	-	NC
	45	N.C.	-	NC	46	N.C.	-	NC
	47	N.C.	-	NC	48	1.5V	Power +1.5V	PWR
	49	N.C.	-	NC	50	Gnd	Ground	PWR
	51	Sel_SATA#	S-ATA® identification	I-1.8	52	3.3V	Power +3.3V	PWR

8.5 PCI slot connectors (J18 & J28)

KTA75/Flex support 2 PCI slots PCI0 – PCI1 (J18 – J28).

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note
	PWR	-12V	F01	E01	TRST#	O	
	O	TCK	F02	E02	+12V	PWR	
	PWR	GND	F03	E03	TMS	O	
NC	I	TDO	F04	E04	TDI	O	
	PWR	+5V	F05	E05	+5V	PWR	
	PWR	+5V	F06	E06	INTA#	I	
	I	INTB#	F07	E07	INTC#	I	
	I	INTD#	F08	E08	+5V	PWR	
NC	-	-	F09	E09	-	-	NC
NC	-	-	F10	E10	+5V (I/O)	PWR	
NC	-	-	F11	E11	-	-	NC
	PWR	GND	F12	E12	GND	PWR	
	PWR	GND	F13	E13	GND	PWR	
NC	-	-	F14	E14	GNT3#	OT	
	PWR	GND	F15	E15	RST#	O	
	O	CLKB	F16	E16	+5V (I/O)	PWR	
	PWR	GND	F17	E17	GNT0/1#	OT	
	I	REQ0/1#	F18	E18	GND	PWR	
	PWR	+5V (I/O)	F19	E19	PME#	I	
	IOT	AD31	F20	E20	AD30	IOT	
	IOT	AD29	F21	E21	+3.3V	PWR	
	PWR	GND	F22	E22	AD28	IOT	
	IOT	AD27	F23	E23	AD26	IOT	
	IOT	AD25	F24	E24	GND	PWR	
	PWR	+3.3V	F25	E25	AD24	IOT	
	IOT	C/BE3#	F26	E26	GNT1#	OT	
	IOT	AD23	F27	E27	+3.3V	PWR	
	PWR	GND	F28	E28	AD22	IOT	
	IOT	AD21	F29	E29	AD20	IOT	
	IOT	AD19	F30	E30	GND	PWR	
	PWR	+3.3V	F31	E31	AD18	IOT	
	IOT	AD17	F32	E32	AD16	IOT	
	IOT	C/BE2#	F33	E33	+3.3V	PWR	
	PWR	GND	F34	E34	FRAME#	IOT	
	IOT	IRDY#	F35	E35	GND	PWR	
	PWR	+3.3V	F36	E36	TRDY#	IOT	
	IOT	DEVSEL#	F37	E37	GND	PWR	
	PWR	GND	F38	E38	STOP#	IOT	
	IOT	LOCK#	F39	E39	+3.3V	PWR	
	IOT	PERR#	F40	E40	SDONE	IO	
	PWR	+3.3V	F41	E41	SB0#	IO	
	IOC	SERR#	F42	E42	GND	PWR	
	PWR	+3.3V	F43	E43	PAR	IOT	
	IOT	C/BE1#	F44	E44	AD15	IOT	
	IOT	AD14	F45	E45	+3.3V	PWR	
	PWR	GND	F46	E46	AD13	IOT	
	IOT	AD12	F47	E47	AD11	IOT	
	IOT	AD10	F48	E48	GND	PWR	
	PWR	GND	F49	E49	AD09	IOT	
SOLDER SIDE					**COMPONENT SIDE**		
	IOT	AD08	F52	E52	C/BE0#	IOT	
	IOT	AD07	F53	E53	+3.3V	PWR	
	PWR	+3.3V	F54	E54	AD06	IOT	
	IOT	AD05	F55	E55	AD04	IOT	
	IOT	AD03	F56	F56	GND	PWR	
	PWR	GND	F57	E57	AD02	IOT	
	IOT	AD01	F58	E58	AD00	IOT	
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR	
	IOT	ACK64#	F60	E60	REQ64#	IOT	
	PWR	+5V	F61	E61	+5V	PWR	
	PWR	+5V	F62	E62	+5V	PWR	

8.5.1 Signal Description –PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the risingedge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33MHz.
PME#	Power Management Event interrupt signal. Wake up signal.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level–they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted. While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.

ERROR REPORTING PINS. The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the 45signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.

INTERRUPT PINS (OPTIONAL). Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.
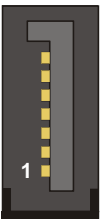
8.6   SATA0, 1, 2, 3, 4, 5 (J12, J13, J9, J11,J10 & J39)

The six SATA ports comply with SATA 3.0 and supports IDE emulation mode, AHCI (Advanced Host Controller Interface) 1.3 mode and RAID mode (RAID 0, RAID 1 and RAID10) across all 6 ports.

The SATA5 (J39) is shared with the mSATA connector.

The SATA 3.0 supports transfer rates up to 6 Gbit/s, but also SATA 1.0 and SATA 2.0 transfer rates are supported, 1.5 Gbit/s and 3.0 Gbit/s respectively.

The S-ATA® interface is available through standard L-type connector (7 pins).

Header	Pin	Signal	Description	Type
	1	GND	Ground	PWR
	2	TX+	Transmit (positive)	DSO
	3	TX-	Transmit (negative)	DSO
	4	GND	Ground	PWR
	5	RX-	Receive (negative)	DSI
	6	RX+	Receive (positive)	DSI
	7	GND	Ground	PWR

Available cable kit:

PN 821035 Cable SATA 500mm

9   BIOS

The BIOS Setup is used to view and configure BIOS settings for the board. The BIOS Setup is accessed by pressing the <Del> -key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins.

The BIOS settings will be loaded automatically when loading "Restore Default" see "Save & Exit" menu. In this Users Guide the default settings are indicated by **bold**. Please notice that "Restore User Defaults" might have different set of default values.

9.1   Main

```
         Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
      Main  Advanced  Chipset  Boot  Security  Save & Exit

   BIOS Information                                          Choose the system default
   BIOS Vendor                  American Megatrends          language.
   Core Version                 4.6.5.3
   Compliancy                   UEFI 2.3; PI 1.2
   Project Version              KTA7X025 x64
   Build Date and Time          09/26/2013 09:12:19

   Memory Information
   Total Memory                 8176 MB (DDR3)
   EC Firmware Version          V1.21 07/05/13

   Board Information
   Product Name                 KTA75/Flex
   PCB ID                       02
   Serial  #                    01185946                     →← : Select Screen
   Part    #                    810540-4500                  ↑↓ : Select Item
   Boot Count                   71                           Enter: Select
                                                             +/- : Change Opt.
   System Language              [English]                    F1: General Help
                                                             F2: Previous Values
   System Date                  [Mon 11/28/2013]             F3: Optimized Defaults
   System Time                  [11:21:40]                   F4: Save & Exit
                                                             ESC: Exit
   Access Level                 Administrator

         Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Blue text for settings that can be changed. White text for actual setting to be changed via the control keys. Black text for settings that cannot be changed via control keys.

The following table describes the changeable settings:

Feature	Options	Description
System Language	English	(only English available)
System Date	MM/DD/YYYY	Set the system date.
System Time	HH:MM:SS	Set the system time.

9.2   Advanced

```
              Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
     Main  Advanced  Chipset   Boot   Security    Save & Exit

  ► PCI Subsystem Settings                              PCI, PCI-X and PCI Express
  ► ACPI Settings                                       Settings.
  ► Trusted Computing
  ► CPU Configuration
  ► IDE Configuration
  ► USB Configuration
  ► Super IO Configuration
  ► Hardware Health Configuration
  ► LAN Configuration
  ► PCI-E Port
  ► Network Stack
                                                        →← : Select Screen
                                                        ↑↓ : Select Item
                                                        Enter: Select
                                                        +/- : Change Opt.
                                                        F1: General Help
                                                        F2: Previous Values
                                                        F3: Optimized Defaults
                                                        F4: Save & Exit
                                                        ESC: Exit


              Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

The Advanced (main) menu contains only submenu selections which will be described in more details on the following pages.

In order to make a selection of a submenu activated the ↑↓ keys until the requested submenu becomes white color, then activate the <Enter>.

9.2.1 Advanced - PCI Subsystem Settings

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Advanced

PCI Bus Driver Version	V 2.05.02	Value to be programmed into PCI Latency Timer Register.
PCI Common Settings		
PCI Latency Timer	[32 PCI Bus Clocks]	
VGA Palette Snoop	[Disabled]	
PERR# Generation	[Disabled]	
SERR# Generation	[Disabled]	
► PCI Express Settings		

→← : Select Screen
↑↓ : Select Item
Enter: Select
+/- : Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.15.1227. Copyright © 2012 American Megatrends, Inc

Function	Selection	Description
PCI Latency Timer	32 PCI Bus Clocks 64 PCI Bus Clocks 96 PCI Bus Clocks 128 PCI Bus Clocks 160 PCI Bus Clocks 192 PCI Bus Clocks 224 PCI Bus Clocks 248 PCI Bus Clocks	Value to be programmed into PCI Latency Timer Register.
VGA Palette Snoop	**Disabled** Enabled	Enables or Disables VGA Palette Registers Snooping.
PERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate PERR#.
SERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate SERR#.

Note: The selection in **bold** is the default selection.

PCI Express Settings

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Advanced

PCI Express Device Register Settings | | Enables or Disables PCI Express
Relaxed Ordering | [Disabled] | Device Relaxed Ordering.
Extended Tag | [Disabled] |
No Snoop | [Enabled] |
Maximu Payload | [Auto] |
Maximum Read Request | [Auto] |

PCI Express Link Register Settings
ASPM Support   [Disabled]
WARNING: Enabling ASPM may cause
         some PCI-E devices to fail
Extended Synch   [Disabled]

Link Training Retry   [5]   →← : Select Screen
Link Training Timeout (uS)   100   ↑↓ : Select Item
Unpopulated Links   [Keep Link ON] Enter: Select
                                                      +/- : Change Opt.
                                                      F1: General Help
                                                      F2: Previous Values
                                                      F3: Optimized Defaults
                                                      F4: Save & Exit
                                                      ESC: Exit

Version 2.15.1227. Copyright © 2012 American Megatrends, Inc

Function	Selection	Description
Relaxed Ordering	**Disabled** Enabled	Enables or Disables PCI Express Device Relaxed Ordering.
Extended Tag	**Disabled** Enabled	If Enabled allows Device to use 8-bit Tag field as a requester.
No Snoop	Disabled **Enabled**	Enables or Disables PCI Express Device No Snoop option.
Maximum Payload	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.
Maximum Read Request	**Auto** 128 Bytes 256 Bytes 512 Bytes 1024 Bytes 2048 Bytes 4096 Bytes	Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.
ASPM Support	**Disabled** Auto Force L0s	Set the ASPM Level: Force L0s - Force all links to L0s State. Auto – BIOS auto configure Disable – Disabled ASPM
Extended Synch	**Disabled** Enabled	If Enabled allows generation of Extended Syncronization patterns.
Link Training Retry	Disabled 2 3 **5**	Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.
Link Training Timeout (uS)	**100**	Defines number of Microseconds software will wait before polling ´Link Training´ bit in Link Status register. Value range from 10 to 1000uS.
Unpopulated Links	**Keep Link ON** Disabled	In order to save power, software will disable unpopulated PCI Express links, if this option set to Disabled.

9.2.2 Advanced - APCI Settings

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Advanced

ACPI Settings		Enables or Disables BIOS APCI Auto Configuration.
Enable ACPI Auto Configuration	[Disabled]	
Enable Hibernation	[Enabled]	
ACPI Sleep State	[S3 only (Suspend to …]	
Lock Legacy Resources	[Disabled]	

→← : Select Screen
↑↓ : Select Item
Enter: Select
+/- : Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.15.1227. Copyright © 2012 American Megatrends, Inc

Function	Selection	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS APCI Auto Configuration.
Enable Hibernation	Disabled **Enabled**	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled S3 only(Suspend to RAM)	Select ACPI sleep state the system will enter when the SUSPEND button is pressed.
Lock Legacy Resources	**Disabled** Enabled	Enables or Disables Lock Legacy Resources.

9.2.3 Advanced - Trusted Computing

```
                    Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
        Advanced

    Configuration                                             Enables or Disables BIOS support
       Security Device Support          [Enable]              for security device. O.S. will not
       TPM State                        [Enabled]             show Security Device. TCG EFI
    Pending operation                   [None]                protocol and INT1A interface will
                                                              not be available.
    Current Status Information
       TPM Enabled Status:              [Enabled]
       TPM Active Status:               [Activated]
       TPM Owner Status:                [Unowned]

                                                              →← : Select Screen
                                                              ↑↓ : Select Item
                                                              Enter: Select
                                                              +/- : Change Opt.
                                                              F1: General Help
                                                              F2: Previous Values
                                                              F3: Optimized Defaults
                                                              F4: Save & Exit
                                                              ESC: Exit

                    Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Function	Selection	Description
Security Device Support	**Disabled** Enabled	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
TPM State	**Disabled** Enabled	Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.
Pending operation	**None** Enable Take Ownership Disable Take Ownership TPM Clear	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.

Note: TPM State and Pending operation are only visible if Security Device Support is Enabled followed by Save and Exit.

9.2.4 Advanced - CPU Configuration

```
                    Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
      Advanced

   CPU Configuration                                              Enable/disable the generation of
                                                                  ACPI _PPC, _PSS, and _PCT
   Module Version: 4.6.5.1 TrinityPI 018                          objects.
   AGESA Vesrion: 1.0.0.8

   PSS Support                   [Enabled]
   PSTATE Adjustment             [PState 0]
   PPC Adjustment                [PState 0]
   NX Mode                       [Enabled]
   SVM Mode                      [Enabled]
   CPB Mode                      [Auto]
   C6 Mode                       [Enabled]
 ► Node 0 Information
                                                                  →← : Select Screen
                                                                  ↑↓ : Select Item
                                                                  Enter: Select
                                                                  +/- : Change Opt.
                                                                  F1: General Help
                                                                  F2: Previous Values
                                                                  F3: Optimized Defaults
                                                                  F4: Save & Exit
                                                                  ESC: Exit


                    Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```
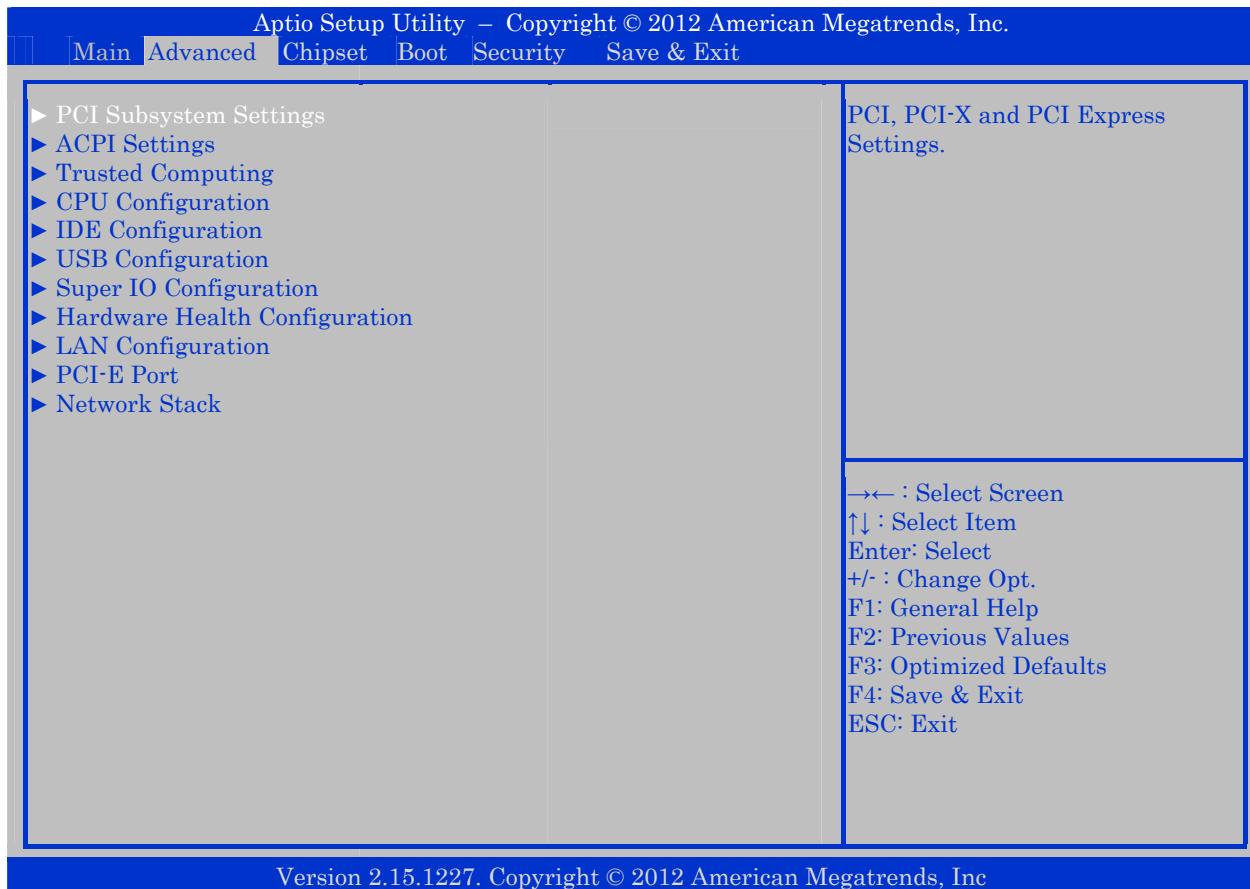
Function	Selection	Description
PSS Support	Disabled **Enabled**	Enable/disable the generation of ACPI _PPC, _PSS, and _PCT objects.
PSTATE Adjustment	**PState 0** – Pstate 7	Provide to adjust startup P-state level.
PPC Adjustment	**PState 0** – Pstate 4	Provide to adjust _PPC object.
NX Mode	Disabled **Enabled**	Enable/disable Ni-execute page protection Function.
SVM Mode	Disabled **Enabled**	Enable/disable CPU Virtualization.
CPB Mode	**Auto** Disabled	Auto/disable CPB.
C6 Mode	Disabled **Enabled**	Enable/disable C6.

Node 0 Information

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Advanced

Socket0: AMD R-464L APU with Radeon™ HD Graphics
Quad Core Running @2329 MHz 600mV
Max Speed: 2300 MHz   Intended Speed: 2300 MHz
Min Speed: 900 MHz
Microcode Patch Level: 6001116

----------- Cache per Core ------------
L1 Instruction Cache: 32 KB/2-way
      L1 Data Cache: 16 KB/4-way
            L2 Cache: 1024 KB/16-way
No L3 Cache Present

→← : Select Screen
↑↓ : Select Item
Enter: Select
+/- : Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.15.1227. Copyright © 2012 American Megatrends, Inc

9.2.5 Advanced - IDE Configuration

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Advanced

IDE Configuration

SATA Port0   Maxtor 6L120M0 (122.9GB)
SATA Port1   Not Pressent
SATA Port2   Not Pressent
SATA Port3   Not Pressent
SATA Port4   Not Pressent
SATA Port5   Not Pressent

→← : Select Screen
↑↓ : Select Item
Enter: Select
+/- : Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.15.1227. Copyright © 2012 American Megatrends, Inc

9.2.6 Advanced - USB Configuration

```
                    Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
        Advanced

    USB Configuration                                          Enables Legacy USB support.
                                                               AUTO option disables legacy
    USB Devices:                                               support if no USB devices are
          1 Keyboard, 1 Mouse                                  connected. DISABLE option will
                                                               keep USB devices available only for
    Legacy USB Support              [Enabled]                  EFI applications.
    USB3.0 Support                  [Disabled]
    XHCI Hand-off                   [Enabled]
    EHCI Hand-off                   [Disabled]

    USB hardware delays and time-outs:
    USB transfer time-out           [20 sec}
    Device reset time-out           [20 sec]
    Device power-up delay           [Auto]
                                                               →← : Select Screen
                                                               ↑↓ : Select Item
                                                               Enter: Select
                                                               +/- : Change Opt.
                                                               F1: General Help
                                                               F2: Previous Values
                                                               F3: Optimized Defaults
                                                               F4: Save & Exit
                                                               ESC: Exit

                    Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Function	Selection	Description
Legacy USB Support	**Enabled** Disabled Auto	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
USB3.0 Support	**Enabled** Disabled	Enable/Disable USB3.0 (XHCI) Controller support.
XHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
EHCI Hand-off	Enabled **Disabled**	This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.
USB transfer time-out	1, 5, 10, **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.
Device reset time-out	10, **20 sec**, 30, 40	USB mass storage device Start Unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Host Controller. ´Auto´ uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

9.2.7 Advanced - Super IO Configuration

```
              Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
    Advanced

    Super IO Configuration                                    Set Parameters of Serial Port 1
                                                              (COMA)
    Super IO Chip                 IT8516F
 ► Serial Port 1 Configuration
 ► Serial Port 2 Configuration




                                                              →← : Select Screen
                                                              ↑↓ : Select Item
                                                              Enter: Select
                                                              +/- : Change Opt.
                                                              F1: General Help
                                                              F2: Previous Values
                                                              F3: Optimized Defaults
                                                              F4: Save & Exit
                                                              ESC: Exit



              Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

The 2 submenus are shown and described on the following pages.

Serial Port 1 Configuration

```
         Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
   Advanced

     Serial Port 1 Configuration                              Enable or Disable Serial Port
                                                              (COM)
     Serial Port                    [Enabled]
     Device Settings                IO=3F8h; IRQ=4;

     Change Settings                [Auto]




                                                              →← : Select Screen
                                                              ↑↓ : Select Item
                                                              Enter: Select
                                                              +/- : Change Opt.
                                                              F1: General Help
                                                              F2: Previous Values
                                                              F3: Optimized Defaults
                                                              F4: Save & Exit
                                                              ESC: Exit



         Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Function	Selection	Description
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM)
Change Settings (Note1)	**Auto** IO=3F8h; IRQ=4; IO=3F8h; IRQ=3,4,5,6,7,10,11,12; IO=2F8h; IRQ=3,4,5,6,7,10,11,12; IO=3E8h; IRQ=3,4,5,6,7,10,11,12; IO=2E8h; IRQ=3,4,5,6,7,10,11,12;	Select an optimal setting for Super IO device.

Note1: only if Serial Port = Enabled

Serial Port 2 Configuration

```
            Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
   Advanced

   Serial Port 2 Configuration                                      Enable or Disable Serial Port
                                                                    (COM)
   Serial Port                      [Enabled]
   Device Settings                  IO=2F8h; IRQ=3;

   Change Settings                  [Auto]




                                                                    →← : Select Screen
                                                                    ↑↓ : Select Item
                                                                    Enter: Select
                                                                    +/- : Change Opt.
                                                                    F1: General Help
                                                                    F2: Previous Values
                                                                    F3: Optimized Defaults
                                                                    F4: Save & Exit
                                                                    ESC: Exit




              Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Function	Selection	Description
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM)
Change Settings (Note1)	**Auto** IO=2F8h; IRQ=3; IO=3F8h; IRQ=3,4,5,6,7,10,11,12; IO=2F8h; IRQ=3,4,5,6,7,10,11,12; IO=3E8h; IRQ=3,4,5,6,7,10,11,12; IO=2E8h; IRQ=3,4,5,6,7,10,11,12;	Select an optimal setting for Super IO device.

Note1: only if Serial Port = Enabled

9.2.8 Advanced - Hardware Health Configuration

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Advanced

Hardware Health Configuration		Use external connected sensor instead of onboard..
System Temperature	: 30ºC/86ºF	
CPU Temperature	: 49.10ºC/120ºF	
System Fan Speed	: 3134 RPM	
System Temperature Ext Type	[OneWire @ GPIO16]	
Fan Cruise Control	[Thermal]	
Fan Settings	35	
Fan Min limit	25	
Fan Max limit	80	
CPU Fan Speed	: 1374 RPM	
Fan Cruise Control	[Thermal]	→← : Select Screen
Fan Settings	50	↑↓ : Select Item
Fan Min limit	0	Enter: Select
Fan Max limit	100	+/- : Change Opt.
		F1: General Help
12V Supply	: 11.70 V	F2: Previous Values
		F3: Optimized Defaults
Watchdog Function	0	F4: Save & Exit
		ESC: Exit

Version 2.15.1227. Copyright © 2012 American Megatrends, Inc

Function	Selection	Description
System Temperature Ext Type　　　　　(note1)	**Disabled** LM75 @ 0x90 OneWire @ GPIO16	
Fan Cruise Control (System Fan)	**Disabled** Thermal　　　(note2) Speed	Disabled = Full speed. Thermal: Regulate according to specified ºC. Speed: Regulate according to specified RPM.
Fan Settings (System Fan)	30 – 90　(note2,note3) 1000 – 9999　(note4)	
Fan Min limit (System Fan)　　(note5)	**0** 　　　　　(note6)	Minimum PWM %, can be used to make sure fan is always active. Make sure Min limit < Max limit.
Fan Max limit (System Fan)　　(note5)	**100** 　　　　　(note6)	Maximum PWM %, can be used to limit the fan noise. Make sure Min limit < Max limit.
Fan Cruise Control (CPU Fan)	**Disabled** Thermal Speed	Disabled = Full speed. Thermal: Regulate according to specified ºC. Speed: Regulate according to specified RPM.
Fan Settings (CPU Fan)	30 – 90　　(note3) 1000 – 9999　(note4)	
Fan Min limit (CPU Fan)　　(note7)	**0** 　　　　　(note6)	Minimum PWM %, can be used to make sure fan is always active. Make sure Min limit < Max limit.
Fan Max limit (CPU Fan)　　(note7)	**100** 　　　　　(note6)	Maximum PWM %, can be used to limit the fan noise. Make sure Min limit < Max limit.
Watchdog Function	0 - 255　　(note8)	0 = Disabled. Enter the service interval in seconds before system will reset. Refer to manual how to reload the timer.

Note1: Only visible if external temperature sensor is connected.
(Example PN1053-4925 "Cable Temperature Sensor - 44P, 400 mm").

Note2: Only visible if external temperature sensor is connected and selected.

Note3: ºC (if Fan Cruise Control = Thermal) use either digit keys to enter value or +/- keys to increase/decrease value. Don't use mix of digit keys and +/- keys.

Note4: RPM (if Fan Cruise Control = Speed) use either digit keys to enter value or +/- keys to increase/decrease value by 100. Don't use mix of digit keys and +/- keys.

Note5: Only visible if external temperature sensor is connected and if System Fan Cruise Control is Thermal.

Note6: Use number keys to enter value.

Note7: Only visible if CPU Fan Cruise Control is Thermal.

Note8: Seconds, use digit keys to enter value. Value 0 means Watchdog is disabled. Refer to "KT-API-V2 User Manual" to control the Watchdog via API or refer to "KT-API-V2 User Manual DLL" how to control Watchdog via Windows DLL.

9.2.9 Advanced - LAN Configuration

```
              Aptio Setup Utility  -  Copyright © 2012 American Megatrends, Inc.
        Advanced

    LAN Configuration                                         Control of Ethernet Devices and
                                                              PXE boot.
    ETH1 Configuration (Upper)         [Enabled]
       MAC Address & Link status:      00E0F42BBC9E+
    ETH2 Configuration (Lower)         [Enabled]
       MAC Address & Link status:      00E0F42 BBC9F-



                                                              →← : Select Screen
                                                              ↑↓ : Select Item
                                                              Enter: Select
                                                              +/- : Change Opt.
                                                              F1: General Help
                                                              F2: Previous Values
                                                              F3: Optimized Defaults
                                                              F4: Save & Exit
                                                              ESC: Exit



               Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Function	Selection	Description
ETH1 Configuration (Upper)	Disabled **Enabled** With PXE boot	Control of Ethernet Devices and PXE boot.
ETH2 Configuration (Lower)	Disabled **Enabled** With PXE boot	Control of Ethernet Devices and PXE boot.

9.2.10 Advanced – PCI-E Port

<table>
<tr>
<td colspan="3">Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.</td>
</tr>
<tr>
<td colspan="3">Advanced</td>
</tr>
<tr>
<td>PCU-E Port

Display port 0 Output Mode
Display port 1 Output Mode
Display port 2 Output Mode
Display port 3 Output Mode</td>
<td>[DP]
[DP]
[DP]
[Disabled]</td>
<td>Enable/Disable UEFI network stack.

→← : Select Screen
↑↓ : Select Item
Enter: Select
+/- : Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit</td>
</tr>
<tr>
<td colspan="3">Version 2.15.1227. Copyright © 2012 American Megatrends, Inc</td>
</tr>
</table>

Function	Selection	Description
Display port # Output Mode (# = 0, 1, 2, 3)	DP eDP Single Link DVI-D Dual Link DVI-D HDMI Travis DP-to-VGA Travis DP-to-LVDS Nutmeg DP-to-VGA Single Link DVI-I CRT (VGA) LVDS Auto Detect Disabled Deafult Settings	NB PCIE Connect Type (Display device).

Defaults: Port 0, 1, 2 = DP and Port 3 = Disabled.

9.2.11 Network Stack

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Advanced

Network stack	[Enable]	Enable/Disable UEFI network stack.
Ipv4 PXE Support	[Enable]	
Ipv6 PXE Support	[Enable]	

→← : Select Screen
↑↓ : Select Item
Enter: Select
+/- : Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
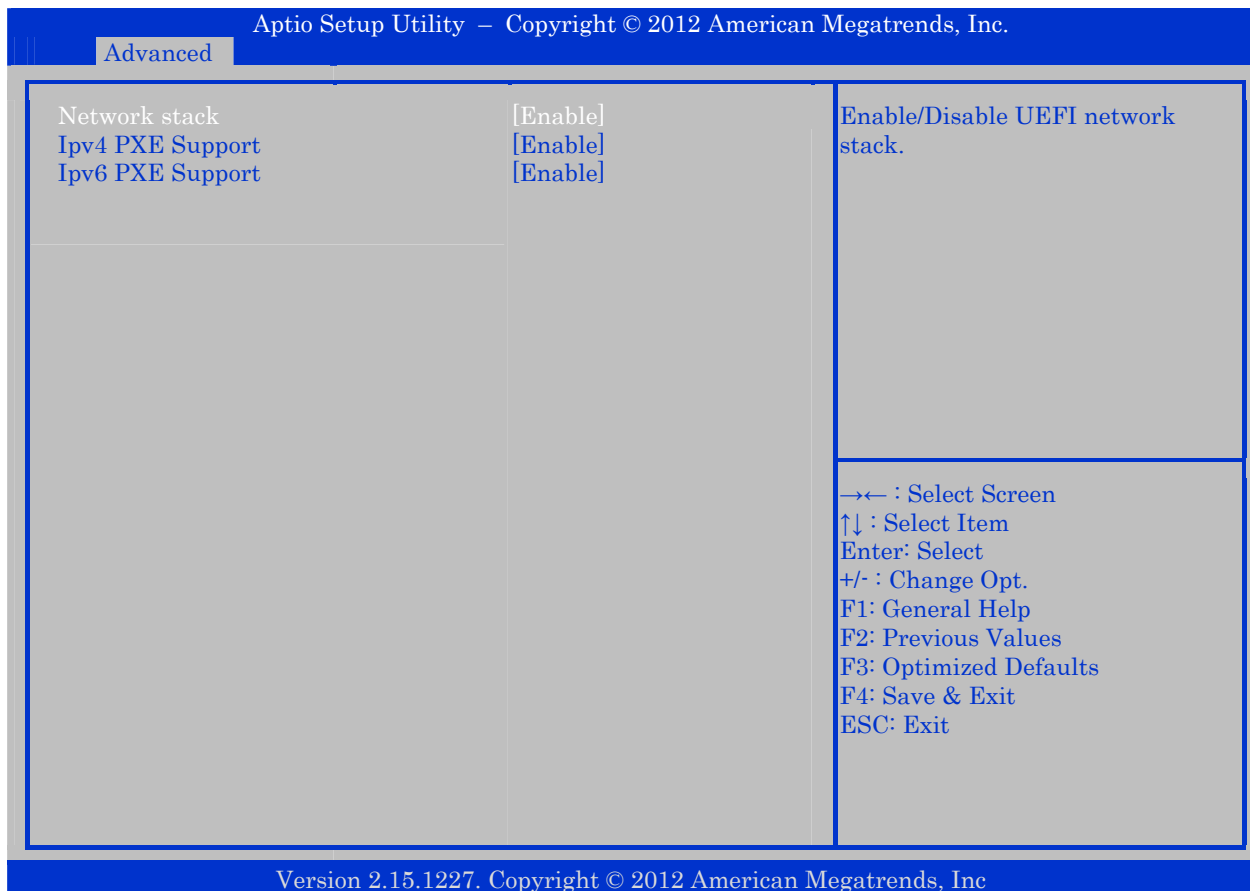
Function	Selection	Description
Network stack	**Disable** Enabled	Enable/Disable UEFI network stack.
Ipv4 PXE Support (Note1)	**Enabled** Disabled	Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.
Ipv6 PXE Support (Note1)	**Enabled** Disabled	Enable Ipv6 PXE Boot Support. If disabled IPV6 PXE boot option will not be created.

Note1: Only if Network stack = Enabled.

9.3   Chipset

```
          Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
     Main   Advanced   Chipset   Boot   Security   Save & Exit

  ▶ South Bridge                                      South Bridge Parameters
  ▶ North Bridge



                                                      →← : Select Screen
                                                      ↑↓ : Select Item
                                                      Enter: Select
                                                      +/- : Change Opt.
                                                      F1: General Help
                                                      F2: Previous Values
                                                      F3: Optimized Defaults
                                                      F4: Save & Exit
                                                      ESC: Exit


          Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

9.3.1 South Bridge

```
                    Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
          Chipset

   AMD Reference code Version:        Trinity PI 1.0.0.8        Options for SATA Configuration.

► SB SATA Configuration
► SB USB Configuration
► SB HD Azalia Configuration

   Restore AC Power Loss              [Power On]


                                                                →← : Select Screen
                                                                ↑↓ : Select Item
                                                                Enter: Select
                                                                +/- : Change Opt.
                                                                F1: General Help
                                                                F2: Previous Values
                                                                F3: Optimized Defaults
                                                                F4: Save & Exit
                                                                ESC: Exit



             Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Please find description of the "SB SATA Configuration", "SB USB Configuration" and "SB HD Azalia Configuration" on the following pages.

Function	Selection	Description
Restore AC Power Loss	Power Off **Power On** Last State	Select AC Power state when power is re-applied after a power failure.

SB SATA Configuration

Chipset

OnChip SATA Channel	[Enabled]	
OnChip SATA Type	[AHCI]	
OnChip IDE Mode	[Legacy mode]	
SATA IDE Combined Mode	[Enabled]	

→← : Select Screen
↑↓ : Select Item
Enter: Select
+/- : Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
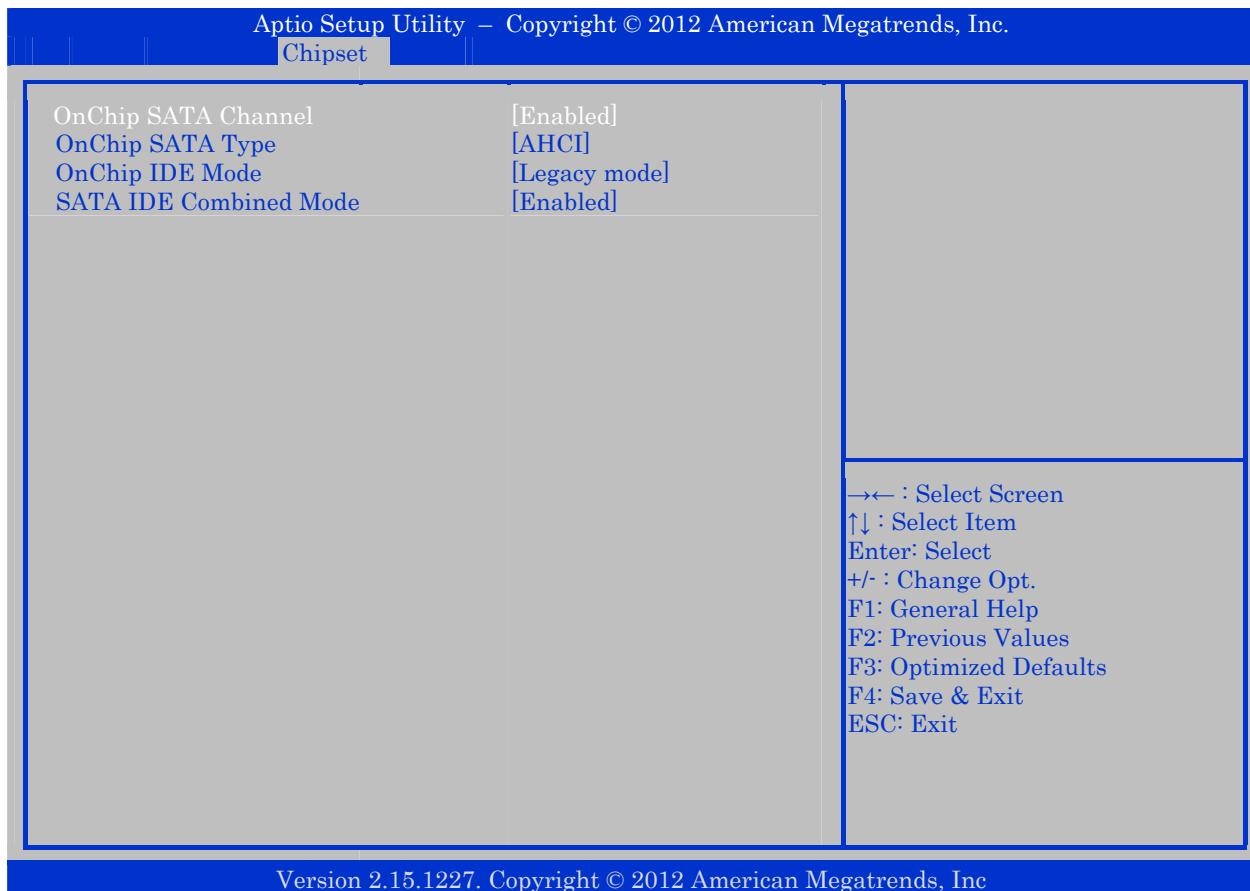
Function	Selection	Description
OnChip SATA Channel	Disabled **Enabled**	
OnChip SATA Type	Native IDE RAID **AHCI** Legacy IDE IDE ->AHCI AHCI as ID 7804 IDE->AHCI as ID 7804	Native IDE /n RAID Native IDE /n AHCI /n Legacy IDE /n IDE ->AHCI /n AHCI as ID 7804 /n IDE->AHCI as ID 7804
OnChip IDE mode	**Legacy mode** Native mode	
SATA IDE Combined Mode	Disabled **Enabled**	

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Chipset

XHCI Controller 0	[Enabled]	XHCI Enable Help.
XHCI Controller 1	[Enabled]	
OHCI HC (Bus 0 Dev 18 Fn 0)	[Enabled]	
EHCI HC (Bus 0 Dev 18 Fn 2)	[Enabled]	
OHCI HC (Bus 0 Dev 19 Fn 0)	[Enabled]	
EHCI HC (Bus 0 Dev 19 Fn 2)	[Enabled]	
OHCI HC (Bus 0 Dev 20 Fn 5)	[Enabled]	
USB PORT 0	[Enabled]	
USB PORT 1	[Enabled]	
USB PORT 2	[Enabled]	
USB PORT 3	[Enabled]	
USB PORT 4	[Enabled]	
USB PORT 5	[Enabled]	→← : Select Screen
USB PORT 6	[Enabled]	↑↓ : Select Item
USB PORT 7	[Enabled]	Enter: Select
USB PORT 8	[Enabled]	+/- : Change Opt.
USB PORT 9	[Enabled]	F1: General Help
		F2: Previous Values
XHCI0 PORT 0	[Enabled]	F3: Optimized Defaults
XHCI0 PORT 1	[Enabled]	F4: Save & Exit
XHCI1 PORT 0	[Enabled]	ESC: Exit
XHCI1 PORT 1	[Enabled]	

Version 2.15.1227. Copyright © 2012 American Megatrends, Inc

Scroll to see further settings.

SB USB Configuration

Function	Selection	Description
XHCI Controller 0	Disabled **Enabled**	XHCI Enable Help.
XHCI Controller 1	Disabled **Enabled**	XHCI Enable Help.
OHCI HC (Bus 0 Dev 18 Fn 0)	Disabled **Enabled**	
EHCI HC (Bus 0 Dev 18 Fn 2)	Disabled **Enabled**	
OHCI HC (Bus 0 Dev 19 Fn 0)	Disabled **Enabled**	
EHCI HC (Bus 0 Dev 19 Fn 2)	Disabled **Enabled**	
OHCI HC (Bus 0 Dev 20 Fn 5)	Disabled **Enabled**	
USB PORT 0 - 9	Disabled **Enabled**	
XHCI0 PORT 0	Disabled **Enabled**	
XHCI0 PORT 1	Disabled **Enabled**	
XHCI1 PORT 0	Disabled **Enabled**	
XHCI1 PORT 1	Disabled **Enabled**	
USB PORT FL0	Disabled **Enabled**	
USB PORT FL1	Disabled **Enabled**	

SB HD Azalia Configuration

```
                Aptio Setup Utility  –   Copyright © 2012 American Megatrends, Inc.
                     Chipset

  HD Audio Azalia Device              [Enabled]
  Audio Front Panel                   [Auto]
     Audio Jack Sensing               [Auto]
  Azalia Snoop                        [Disabled]




                                                     →← : Select Screen
                                                     ↑↓ : Select Item
                                                     Enter: Select
                                                     +/- : Change Opt.
                                                     F1: General Help
                                                     F2: Previous Values
                                                     F3: Optimized Defaults
                                                     F4: Save & Exit
                                                     ESC: Exit




                  Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```
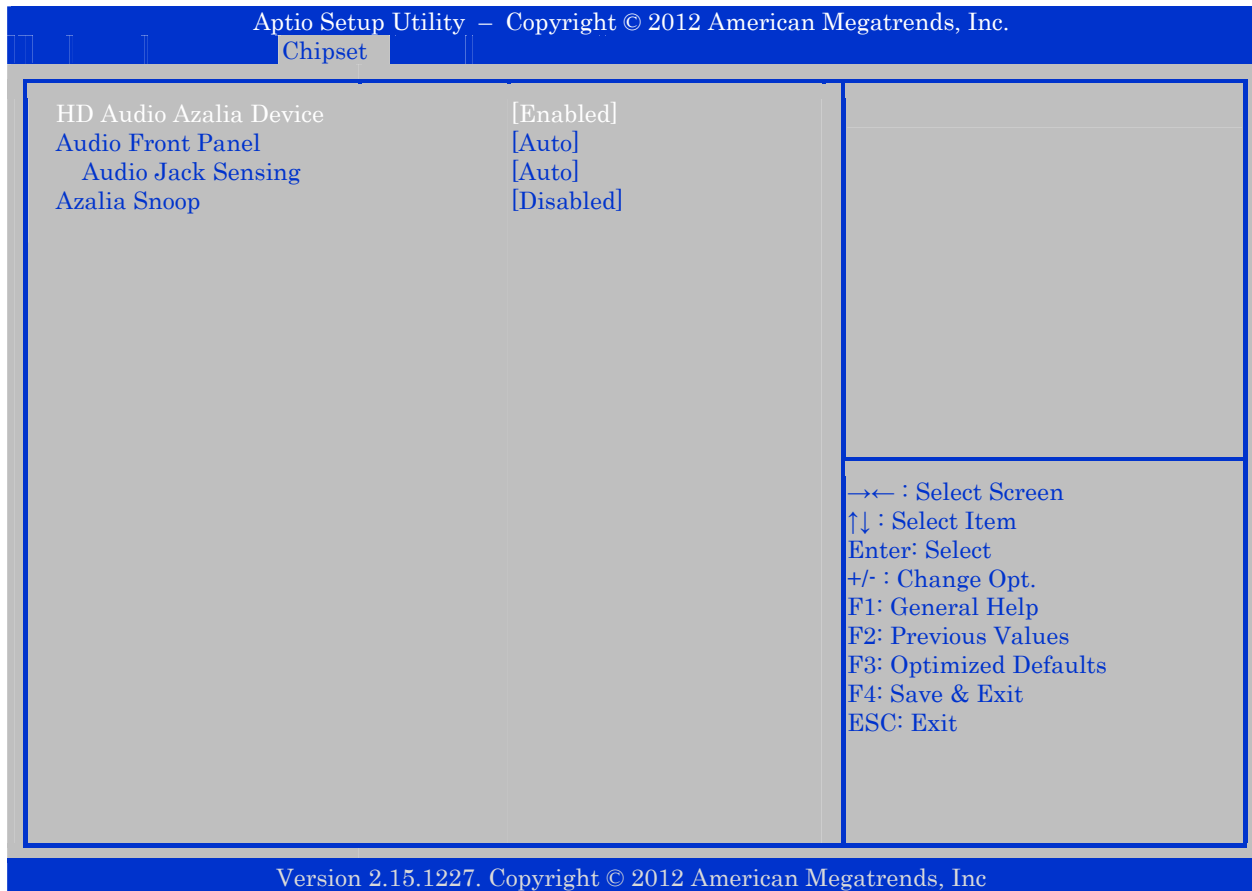
Function	Selection	Description
HD Audio Azalia Device	Auto Disabled **Enabled**	
Audio Front Panel	**Auto** Disabled Enabled	
Audio Jack Sensing	Disabled **Auto**	Auto: The insertions of audio jacks are auto determined. Disabled: Driver assumes that all jacks are inserted (useful when using the Audio pinrow)
Azalia Snoop	**Disabled** Enabled	Enable or disable internal HDMI codec for Azalia.

9.3.2 North Bridge

```
               Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
         Chipset

    North Bridge Configuration                              GFX Configuration.

  ► Graphics Configuration
    Memory Information

    Total Memory: 8176 MB (DDR3)
  ► Memory Configuration
  ► Socket 0 Information

                                                       →← : Select Screen
                                                       ↑↓ : Select Item
                                                       Enter: Select
                                                       +/- : Change Opt.
                                                       F1: General Help
                                                       F2: Previous Values
                                                       F3: Optimized Defaults
                                                       F4: Save & Exit
                                                       ESC: Exit

         Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Graphics Configuration

```
              Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
                   Chipset

      GFX Configuration                                      Select Primary Video Device that
                                                             BIOS will use as output.
      Primary Video Device              [IGD Video]

      Brightness Control Mode Switch    [Control by Driver]
      Integrated Graphics               [Auto]
      PSPP Policy                       [Performance]




                                                             →← : Select Screen
                                                             ↑↓ : Select Item
                                                             Enter: Select
                                                             +/- : Change Opt.
                                                             F1: General Help
                                                             F2: Previous Values
                                                             F3: Optimized Defaults
                                                             F4: Save & Exit
                                                             ESC: Exit



              Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Function	Selection	Description
Primary Video Device	**IGD Video** NB PCIe slot Video SB PCIe slot Video	Select Primary Video Device that BIOS will use as output.
Brightness Control Mode Switch	Control by VBIOS **Control by Driver**	Switch Brightness Control Mode between VBIOS/DRIVER.
Integrated Graphics	**Auto** Disabled Force	Enable Integrated Graphics controller.
PSPP Policy	Disabled **Performance** Balanced-High Balanced-Low Power Saving	PCIe speed power policy

Memory Configuration

Chipset

Memory Configuration		This option Allows User to select different Memory Clock. Default value is 800MHz.
Memory Clock	[Auto]	
Memory Hole Remapping	[Enabled]	
Bank Interleaveing	[Enabled]	
Channel Interleaving	[Enabled]	
Memory Clear	[Disabled]	

→← : Select Screen
↑↓ : Select Item
Enter: Select
+/- : Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Version 2.15.1227. Copyright © 2012 American Megatrends, Inc

Function	Selection	Description
Memory Clock	**Auto** 800MHz 1066MHz 1333MHz 1600MHz 1866MHz	This option Allows User to select different Memory Clock. Default value is 800MHz
Memory Hole Remapping	Disabled **Enabled**	Memory Hole Remapping.
Bank Interleaveing	Disabled **Enabled**	Bank Interleaveing
Channel Interleaving	Disabled **Enabled**	Channel Interleaving
Memory Clear	**Disabled** Enabled	Enable/Disable Memory Clear function.

Socket 0 Information

Chipset

Socket 0 Information

   Starting Address: 0 KB
    Ending Address: 8388607 KB

Dimm0: size=8192 MB, speed=800 MHz
Dimm1: Not Present

→← : Select Screen
↑↓ : Select Item
Enter: Select
+/- : Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

9.4   Boot

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.		
Main Advanced Chipset **Boot** Security Save & Exit		

```
Boot Configuration                                                Number of seconds to wait for
Setup Prompt Timeout              1                                setup activation key.
Bootup NumLock State             [On]                             65535 (0xFFFF) means indefinite
                                                                  waiting.
Quit Boot                        [Disabled]
Fast Boot                        [Disabled]

CSM16 Module Version              07.69

GateA20 Active                   [Upon Request]
Option ROM Message               [Force BIOS]
INT19 Trap Response              [Immediate]

                                                                 →←  : Select Screen
Boot Option Priorities                                           ↑↓ : Select Item
Boot Option #1                   [P0: Maxtor 6L120M0 …]          Enter: Select
Boot Option #2                   [UEFI: Built-in EFI …]          +/- : Change Opt.
▶ CSM parameters                                                 F1: General Help
                                                                 F2: Previous Values
                                                                 F3: Optimized Defaults
                                                                 F4: Save & Exit
                                                                 ESC: Exit
```
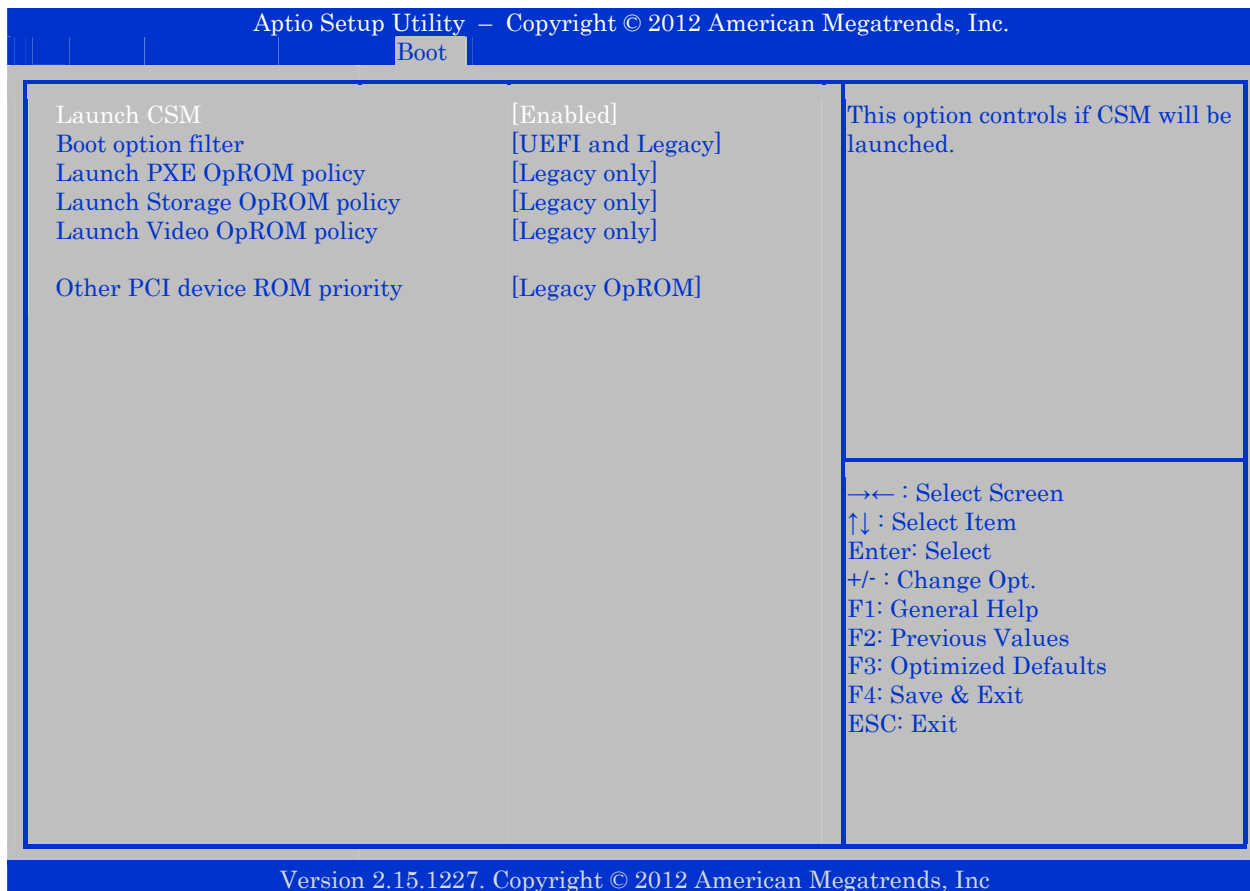
Version 2.15.1227. Copyright © 2012 American Megatrends, Inc

Note: When pressing <F7> while booting it is possible manually to select boot device.

Function	Selection	Description
Setup Prompt Timeout	**1**, 2 - 65535 (Note)	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the Keyboard Numlock state.
Quit Boot	**Disabled** Enabled	Enables or disables Quiet Boot option.
Fast Boot	**Disabled** Enabled	Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
GateA20 Active	**Upon Request** Always	Upon Request: GA20 can be disabled using BIOS services. Always: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.
Option ROM Message	**Force BIOS** Keep Current	Set display mode for Option ROM.
INT19 Trap Response	**Immediate** Postponed	BIOS reaction on INT19 trapping by Option ROM. Immediate: execute the trap right away. Postponed: execute the trap during legacy boot.
Boot Option #1	(list of bootable devices)	Sets the system boot order.

Note: To enter number use digit keys and/or +/- keys.

9.4.1 CSM parameters

```
                    Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
                                        Boot

      Launch CSM                        [Enabled]              This option controls if CSM will be
      Boot option filter                [UEFI and Legacy]      launched.
      Launch PXE OpROM policy           [Legacy only]
      Launch Storage OpROM policy       [Legacy only]
      Launch Video OpROM policy         [Legacy only]

      Other PCI device ROM priority     [Legacy OpROM]



                                                               →← : Select Screen
                                                               ↑↓ : Select Item
                                                               Enter: Select
                                                               +/- : Change Opt.
                                                               F1: General Help
                                                               F2: Previous Values
                                                               F3: Optimized Defaults
                                                               F4: Save & Exit
                                                               ESC: Exit


                      Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Function	Selection	Description
Launch CSM	**Enabled** Disabled	This option controls if CSM will be launched.
Boot option filter	**UEFI and Legacy** Legacy only UEFI only	This option controls what devices system can boot to.
Launch PXE OpROM policy	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and Legacy PXE OpROM.
Launch Storage OpROM policy	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and Legacy Storage OpROM.
Launch Video OpROM policy	Do not launch UEFI only **Legacy only**	Controls the execution of UEFI and Legacy Video OpROM.
Other PCI device ROM priority	UEFI OpROM **Legacy OpROM**	For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

9.5   Security

```
           Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
     Main   Advanced   Chipset   Boot   Security    Save & Exit

   Password Description                              Set Administrator Password

   If ONLY the Administrator's password is set,
   then this only limits access to Setup and is
   only asked for when entering Setup.
   If ONLY the User's password is set, then this
   is a power on password and must be entered to
   boot or enter Setup. In Setup the User will
   have Administrator rights.
   The password length must be
   in the following range:
   Minimum length                      3
   Maximum length                      20


   Administrator Password                            →← : Select Screen
   User Password                                     ↑↓ : Select Item
                                                     Enter: Select
                                                     +/- : Change Opt.
   System Mode state            Setup                F1: General Help
   Secure Boot state            Disabled             F2: Previous Values
                                                     F3: Optimized Defaults
   Secure Boot                  [Enabled]            F4: Save & Exit
   Secure Boot Mode             [Standard]           ESC: Exit


           Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```
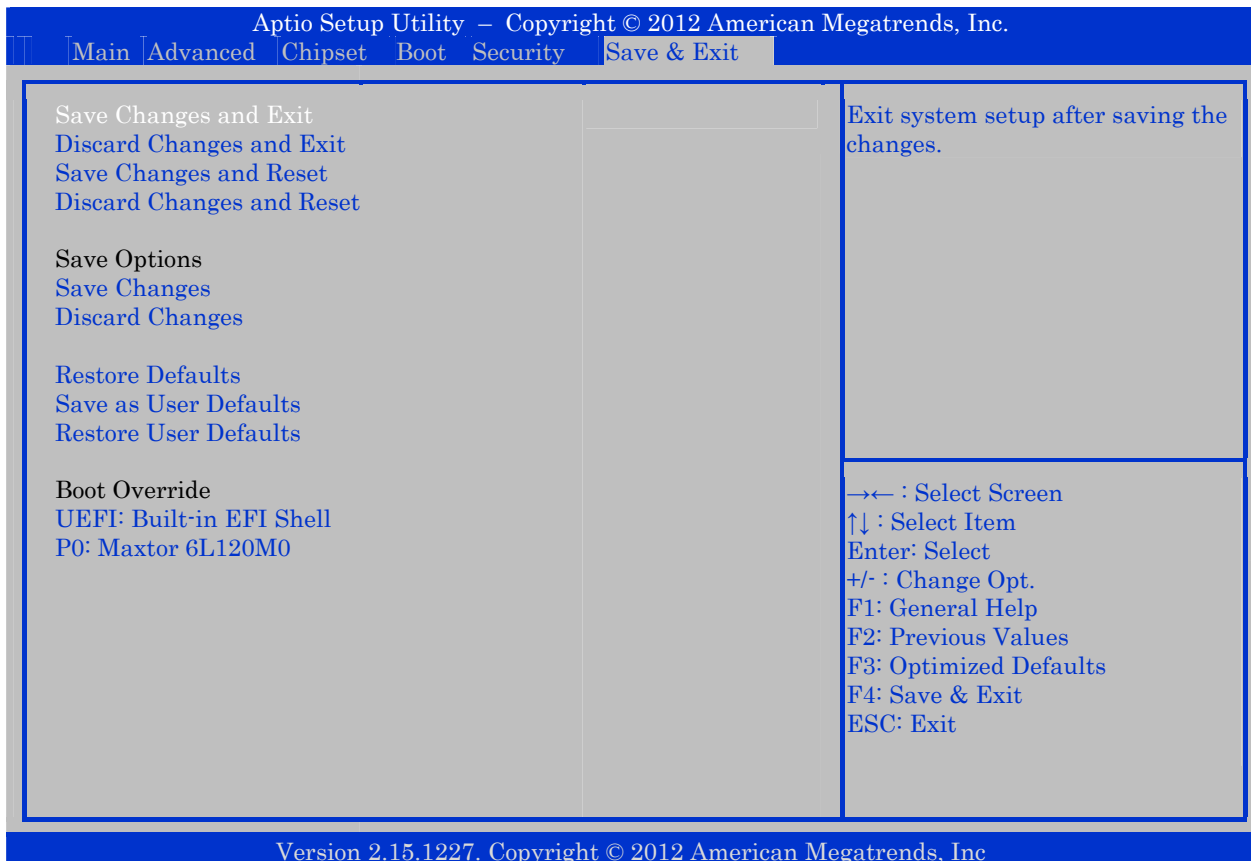
Function	Selection	Description
Administrator Password	(See Password description above)	Set Administrator Password
User Password	(See Password description above)	Set User Password
Secure Boot	Disabled **Enabled**	Secure Boot flow control. Secure Boot is possible only if System runs in User Mode.
Secure Boot Mode	**Standard** Custom	Secure Boot mode selector. Standard: fixed Secure boot policy. Custom: changeable Image Execution policy and Secure Boot Key databases.

9.6　　Save & Exit

This Menu is special; having no "selections" for each function, or in other words, the function is the same as the selection.

```
Aptio Setup Utility  –  Copyright © 2012 American Megatrends, Inc.
  Main  Advanced  Chipset   Boot   Security    Save & Exit

    Save Changes and Exit                           Exit system setup after saving the
    Discard Changes and Exit                        changes.
    Save Changes and Reset
    Discard Changes and Reset

    Save Options
    Save Changes
    Discard Changes

    Restore Defaults
    Save as User Defaults
    Restore User Defaults

    Boot Override                                   →← : Select Screen
    UEFI: Built-in EFI Shell                        ↑↓ : Select Item
    P0: Maxtor 6L120M0                              Enter: Select
                                                    +/- : Change Opt.
                                                    F1: General Help
                                                    F2: Previous Values
                                                    F3: Optimized Defaults
                                                    F4: Save & Exit
                                                    ESC: Exit

          Version 2.15.1227. Copyright © 2012 American Megatrends, Inc
```

Note: When pressing <F7> while booting it is possible manually to select boot device.

Function	Description
Save Changes and Exit	Exit system setup after saving the changes.
Discard Changes and Exit	Exit system setup without saving any changes.
Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Reset	Reset the system without saving any changes.
Save Changes	Save Changes done so far to any of the setup options.
Discard Changes	Discard Changes done so far to any of the setup options.
Restore Defaults	Restore/Load Default values for all the setup options.
Save as User Defaults	Save the Changes done so far as User Defaults.
Restore User Defaults	Restore the User Defaults to all the setup options.
(possible list of boot devices)	Selection table of bootable devices. When selected system will boot on selected device.

10 AMI BIOS Beep Codes

Boot Block Beep Codes:

Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes:

Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes:

Beeps	Troubleshooting Action
1, 2 or 3	Reset the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond "all hope", eliminate the possibility of interference due to a malfunctioning add-in card. Remove all expansion cards, except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reset the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

Appendix: Mating Connectors

The Mating connectors / Cables are connectors or cable kits which are fitting the On-board connector.

Connector		Onboard Connectors		Mating Connectors	
		Manufacturer	P/N	Manufacturer	P/N
DisplayPort	J3/J4/J43	Foxconn	3VD11203-H7AB-4H		
USB10/USB11/USB12/USB13	J14/J15	Lotes	ABA-USB-104-K01		
ETH1/ETH2	J8	Ude	RMT-123AGF1F		
USB6/USB7/USB8/USB9	J20	Foxconn	UB11123-Q8DF-4F		
Audio stack	J40	Lotes	ABA-JAK-028-K03		
Power ATX-BTX	J17	Molex	44206-0002	Molex	5557-24R
Power ATX-core	J19	Lotes	ABA-POW-003-K02	Molex	39-01-2045
Audio Header	J41	Molex	87832-2620	Molex Kontron	51110-2651 821043 (kit)
Power Out	J18	Molex	22-23-2041	Molex Kontron	22-01-2045 1027-3669 (Kit)
USB4/USB5	J16	Foxconn	HS1105F-RNP9		
SPI	J21	Pinrex	512-90-10GBE5		
COM1/COM2	J22/J23	Pinrex	512-90-10GBE5	Molex Kontron	90635-1103 821017 (kit)
LPC	J29	Foxconn	HC11101-P0		
Frontpanel	J5	Wieson	G2120HT0038-016	Molex Kontron	90635-1243 821042 (kit)
CPU Fan/System Fan	J24/J25	Tyco	1470947-1	Molex	47054-1000
Feature	J26	Pinrex	52C-90-44GB00	Don Connex	A05c-44-B-G-A-1-G
		Foxconn	HS5422F	Kontron	1052-5885 (kit)
KBD/MSE	J27	Molex	22-23-2061	Molex Kontron	22-01-2065 1053-2384 (kit)

Cable & Driver Kit KTA70M/KTA75 (PN 826600-R11) contains:

    2x PN 821017 Cable, COM, 2.54mm, 100mm

    1x PN 1052-5885 Cable, Feature 44pol 1 to1, 300mm

    1x PN 1053-2384 Bracket Cable 6-Pin to PS2-Kbd-Mse

    1x PN 821042 Cable, Front Panel Open-End

    1x PN 821043 Cable, Audio Open-End

    6x PN 821035 Cable, SATA, 500mm

    1x PN 1052-5814 Cable, ATX Power for KTA70M

    1x PN 1027-3669 Cable Power Out for KTA70M

    1x PN 821401 Cable+Bracket, USB, 10poled

    1x PN 1052-5818 SW,Man&Driver CD,KA70M/KTA75

Appendix: OS Setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on KTA7x Driver CD or they can be downloaded from the homepage http://www.kontron.com/

For some OS like Win7 when installing OS via USB DVD, USB Keyboard/Mouse, please connect the USB DVD, USB Keyboard/Mouse to USB2.0 ports only or disable USB3.0 in BIOS.

Corporate Offices

Europe, Middle East & Africa	**North America**	**Asia Pacific**
Oskar-von-Miller-Str. 1	14118 Stowe Drive	17 Building,Block #1,ABP
85386 Eching/Munich	Poway, CA 92064-7147	188 Southern West 4th Ring Road
Germany	USA	Beijing 100070, P.R.China
Tel.: +49 (0) 8165/ 77 777	Tel.: +1 888 294 4558	Tel.: + 86 10 63751188
Fax: +49 (0) 8165/ 77 219	Fax: +1 858 677 0898	Fax: + 86 10 83682438
info@kontron.com	info@us.kontron.com	info@kontron.cn