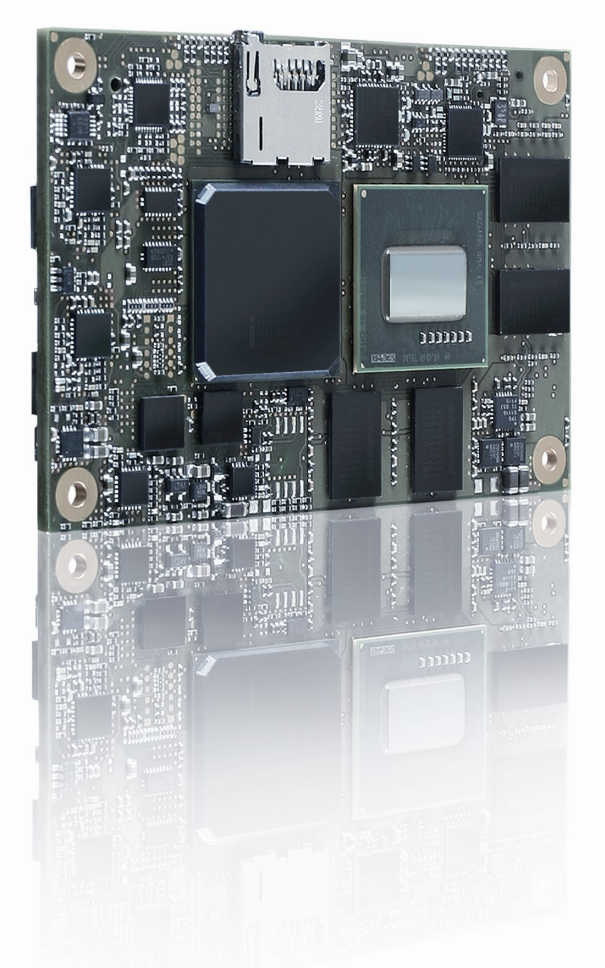
» Kontron User's Guide «



COMe-mTT10

Document Revision 130

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1 User Information

1.1 About This Document

This document provides information about products from Kontron Europe GmbH and/or its subsidiaries. No warranty of suitability, purpose, or fitness is implied. While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied “as-is” and is subject to change without notice.

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1.4 Standards

Kontron Europe GmbH is certified to ISO 9000 standards.

1.5 Warranty

For this Kontron Europe GmbH product warranty for defects in material and workmanship exists as long as the warranty period, beginning with the date of shipment, lasts. During the warranty period, Kontron Europe GmbH will decide on its discretion if defective products are to be repaired or replaced.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

Warranty does not apply for defects arising/resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, as well as the operation outside of the product´s environmental specifications and improper installation and maintenance.

Kontron Europe GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Europe GmbH that are caused by a faulty Kontron Europe GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Europe GmbH and/or its subsidiaries are available for technical support. We are committed to make our product easy to use and will help you use our products in your systems.

Please consult our Website at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section http://emdcustomersection.kontron.com for the latest BIOS downloads, Product Change Notifications, Board Support Packages, DemoImages, 3D drawings and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 Product Description

The credit card size (55mm x 84 mm) COM Express® mini SFF COM, COMe-mTT10, featuring an Intel® Atom™ processor E6xx and is designed according to the PICMG COM Express® R.2.0 pin-out Type 10 specification. The COMe-mTTi10 family is designed with industrial-grade components that are fully functional even at the extended temperature range (E2) from -40 to +85°C, special build versions for commercial temperature are available as well. With its memory onboard, a robust micro-SD Card socket or optional a SATA Flash memory, it is ideal for use in harsh environments and thus complements the existing portfolio perfectly.

2.2 Naming clarification

COM Express® defines a Computer-On-Module, or COM, with all components necessary for a bootable host computer, packaged as a super component.

» COMe-bXX# modules are Kontron's COM Express® modules in basic form factor (125mm x 95mm)

» COMe-cXX# modules are Kontron's COM Express® modules in compact form factor (95mm x 95mm)

» COMe-mXX# modules are Kontron's COM Express® modules in mini form factor (55mm x 84mm)

The product names for Kontron COM Express® Computer-on-Modules consist of a short form of the industry standard (**COMe-**), the form factor (**b**=basic, **c**=compact, **m**=mini), the capital letters for the CPU and Chipset Codenames (**XX**) and the pin-out type (**#**) followed by the CPU Name.

2.3 Understanding COM Express® Functionality

All Kontron COM Express® basic and compact modules contain two 220pin connectors; each of it has two rows called Row A & B on primary connector and Row C & D on secondary connector. COM Express® Computer-on-modules feature the following maximum amount of interfaces according to the PICMG module Pin-out type:

Feature	Pin-Out Type 1	Pin-Out Type 10	Pin-Out Type 2	Pin-Out Type 6
HD Audio	1x	1x	1x	1x
Gbit Ethernet	1x	1x	1x	1x
Serial ATA	4x	4x	4x	4x
Parallel ATA	-	-	1x	-
PCI	-	-	1x	-
PCI Express x1	6x	6x	6x	8x
PCI Express x16 (PEG)	-	-	1x	1x
USB Client	1x	1x	-	-
USB 2.0	8x	8x	8x	8x
USB 3.0	-	2x	-	4x
VGA	1x	-	1x	1x
LVDS	Dual Channel	Single Channel	Dual Channel	Dual Channel
DP++ (SDVO/DP/HDMI/DVI)	1x optional	1x	3x shared with PEG	3x
LPC	1x	1x	1x	1x
External SMB	1x	1x	1x	1x
External I2C	1x	1x	1x	1x
GPIO	8x	8x	8x	8x
SDIO shared w/GPIO	1x optional	1x optional	-	1x optional
UART (2-wire COM)	-	2x	-	2x
FAN PWM out	-	1x	-	1x

2.4 COM Express® Documentation

This product manual serves as one of three principal references for a COM Express® design. It documents the specifications and features of COMe-mTT10. Additional references are available at your Kontron Support or at PICMG®:

» The COM Express® Specification defines the COM Express® module form factor, pin-out, and signals. This document is available at the PICMG® website by filling out the order form.

» The COM Express® Design Guide by PICMG® serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express® modules.

Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.5 COM Express® Benefits

COM Express® modules are very compact, highly integrated computers. All Kontron COM Express® modules feature a standardized form factor and a standardized connector layout which carry a specified set of signals. Each COM is based on the COM Express® specification. This standardization allows designers to create a single-system baseboard that can accept present and future COM Express® modules.

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A single baseboard design can use a range of COM Express® modules with different sizes and pin-outs. This flexibility can differentiate products at various price/performance points, or when designing future proof systems that have a built-in upgrade path. The modularity of a COM Express® solution also ensures against obsolescence when computer technology evolves. A properly designed COM Express® baseboard can work with several successive generations of COM Express® modules.

A COM Express® baseboard design has many advantages of a customized computer-board design and, additionally, delivers better obsolescence protection, heavily reduced engineering effort, and faster time to market.

3 Product Specification

3.1 Modules & Accessories

The COM Express® mini sized Computer-on-Module COMe-mTT10 (NTC1) follows pin-out Type 10 and is compatible to PICMG specification COM.0 Rev 2.0. The COMe-mTT10, based on Intel's Queens Bay platform, is available in different variants to cover the demand of different performance, price and power:

Commercial grade modules (0°C to 60°C operating), COMe-mTTc10

Product Number	Product Name	Processor	PCH and Features
34004-2000-16-1	COMe-mTTc10 E680 2GB/mSD	Intel® Atom™ E680	EG20T, 3xPCIe, 2GB DDR2, microSD socket
34004-1000-16-1	COMe-mTTc10 E680 1GB/mSD	Intel® Atom™ E680	EG20T, 3xPCIe, 1GB DDR2, microSD socket
34004-1000-13-1	COMe-mTTc10 E660 1GB/mSD	Intel® Atom™ E660	EG20T, 3xPCIe, 1GB DDR2, microSD socket
34004-1000-10-1	COMe-mTTc10 E640 512MB/mSD	Intel® Atom™ E640	EG20T, 3xPCIe, 1GB DDR2, microSD socket
34004-5100-06-1	COMe-mTTc10 E620 512MB/mSD	Intel® Atom™ E620	EG20T, 3xPCIe, 512MB DDR2, microSD socket

Industrial grade modules (E2, -40°C to 85°C operating), COMe-mTTi10

Product Number	Product Name	Processor	PCH and Features
34003-1040-16-1	COMe-mTTi10 E680T 1GB/4GB	Intel® Atom™ E680T	EG20T, 3xPCIe, 1GB DDR2, 4GB SATA SLC SSD
34003-1040-13-1	COMe-mTTi10 E660T 1GB/4GB	Intel® Atom™ E660T	EG20T, 3xPCIe, 1GB DDR2, 4GB SATA SLC SSD
34003-1040-10-1	COMe-mTTi10 E640T 1GB/4GB	Intel® Atom™ E640T	EG20T, 3xPCIe, 1GB DDR2, 4GB SATA SLC SSD
34003-2000-16-1	COMe-mTTi10 E680T 2GB/mSD	Intel® Atom™ E680T	EG20T, 3xPCIe, 2GB DDR2, microSD socket
34003-1000-16-1	COMe-mTTi10 E680T 1GB/mSD	Intel® Atom™ E680T	EG20T, 3xPCIe, 1GB DDR2, microSD socket
34003-1000-13-1	COMe-mTTi10 E660T 1GB/mSD	Intel® Atom™ E660T	EG20T, 3xPCIe, 1GB DDR2, microSD socket
34003-1000-10-1	COMe-mTTi10 E640T 1GB/mSD	Intel® Atom™ E640T	EG20T, 3xPCIe, 1GB DDR2, microSD socket
34003-5100-06-1	COMe-mTTi10 E620T 512MB/mSD	Intel® Atom™ E620T	EG20T, 3xPCIe, 512MB DDR2, microSD socket

Possible memory and onboard Flash configurations 3400x-MMFF-xx-x:

» MM = 51: 512MB DDR2 Memory (4 x 1Gb chips on bottom)

» MM = 10: 1024MB DDR2 Memory (8 x 1Gb chips)

» MM = 20: 2048MB DDR2 Memory (8 x 2Gb chips)

» FF = 00: microSD Card onboard

» FF = 20: 2GB onboard SATA SSD

» FF = 40: 4GB onboard SATA SSD

» FF = 80: 8GB onboard SATA SSD

» FF = 16: 16GB onboard SATA SSD

» FF = 32: 32GB onboard SATA SSD

Please contact your local sales for customized Memory/Flash combinations

Accessories

Product Number	Carrier Boards
34101-0000-00-1	COM Express® Eval Carrier Type 10
34104-0000-00-0	COM Express® Reference Carrier-i Type 10

Product Number	Cooling & Mounting
34003-0000-99-0	HSP COMe-mTT10 thread (11mm)
34003-0000-99-1	HSP COMe-mTT10 through (11mm)
34003-0000-99-2	HSP COMe-mTT10 slim thread (6.5mm)
34003-0000-99-3	HSP COMe-mTT10 slim though (6.5mm)
34003-0000-99-0C01	HSK COMe-mTT10 slim passive thread
34099-0000-99-0	COMe mini Active Uni Cooler (for CPUs up to 10W)
34099-0000-99-1	COMe mini Passive Uni Cooler (for CPUs up to 5W)
34099-0000-99-2	COMe mini Passive Uni Cooler Slim (for CPUs up to 3-5W)
34017-0000-00-0	COMe mMount KIT 5/8mm 1set

Product Number	Adapter & Cables
9-5000-0352	ADA-LVDS-DVI 18bit (LVDS to DVI converter)
9-5000-0353	ADA-LVDS-DVI 24bit (LVDS to DVI converter)
34120-0000-00-2	ADA-COMe-T10-T2 (Pin-out Type 10 to Type 2 Adapter)
96006-0000-00-1	COMe POST T10

3.2 Functional Specification

Processor

The Intel® Atom™ E600 (Tunnel Creek) CPU family supports:

» Intel® Hyper-Threading Technology

» Intel® Virtualization Technology (VT-x)

» Idle States

» Enhanced Intel SpeedStep® Technology

» Thermal Monitoring Technologies

» Execute Disable Bit

CPU specifications

Processor	Cores / Threads	CPU Clock	L2 Cache	VT-x	HTT	EIST	Max TDP
Intel® Atom™ E620T/E620	1 / 2	600MHz	512KB	Yes	Yes	Yes	3.3W
Intel® Atom™ E640T/E640	1 / 2	1000MHz	512KB	Yes	Yes	Yes	3.6W
Intel® Atom™ E660T/E660	1 / 2	1300MHz	512KB	Yes	Yes	Yes	3.6W
Intel® Atom™ E680T/E680	1 / 2	1600MHz	512KB	Yes	Yes	Yes	4.5W

Memory

Sockets	memory down
Memory Type	DDR2-800
Maximum Size	2GB
Technology	Single Channel (32bit)

Graphics Core

The integrated Intel® GMA 600 based on PowerVR SGX535 core supports:

Graphics Core Render Clock	400MHz (E680/E660 CPU) 320MHz (E640/E620 CPU)
Execution Units / Pixel Pipelines	4
Max Graphics Memory	759MB
GFX Memory Bandwidth (GB/s)	4.2
GFX Memory Technology	DVMT
API (DirectX/OpenGL)	9.0L / 2.1
Shader Model	3.0
Hardware accelerated Video	H.264,MPEG2/4,VC1,WMV9, DivX
Independent/Simultaneous Displays	2
Display Port	-
HDCP support	-

Monitor output

CRT max Resolution	-
TV out:	-

LVDS

LVDS Bits/Pixel	1x18 / 1x24
LVDS Bits/Pixel with dithering	-
LVDS max Resolution:	1280x768, 80MHz
PWM Backlight Control:	YES
Supported Panel Data:	EDID

Display Interfaces

Discrete Graphics	-
Digital Display Interface DDI1	SDVOB
Digital Display Interface DDI2	-
Digital Display Interface DDI3	-
Maximum Resolution on DDI	1920x1080

Platform Controller Hub

The 90nm Intel Platform Controller Hub EG20T Topcliff supports:

» PCI Express Revision 1.0

» USB 2.0

» USB Client

» SDIO 2.0

» SATA 3Gb/s

Storage

onboard SSD	2-32GB SLC, 2-64GB MLC (SATA)
SD Card support	1x SD 2.0 shared with GPIO, 1x onboard microSD-Card socket
IDE Interface	-
Serial-ATA	up to 2x SATA 3Gb/s
SATA AHCI	AHCI 1.1 with NCQ and Port Multiplier
SATA RAID	-

When the optional SATA onboard drive is used only 1 SATA interface (SATA 0) is available

Connectivity

USB	6x USB 2.0
USB Client	1x USB Client (USB #7)
PCI	-
PCI External Masters	-
PCI Express	3x PCIe x1 Gen1
Max PCI Express	4x PCIe x1 without Topcliff
PCI Express x2/x4 configuration	-
Ethernet	10/100/1000 Mbit
Ethernet controller	Broadcom BCM54610

Ethernet

The Broadcom BCM54610 ethernet supports:

» Jumbo packets up to 10KB

» WOL (Wake On LAN)

» PXE (Preboot eXecution Environment)

Misc Interfaces and Features

Supported BIOS Size/Type	2MB SPI
Audio	HD Audio
Onboard Hardware Monitor	WINBOND W83L771W
Trusted Platform Module*	Infineon TPM 1.2 SLB9635TT optional
Miscellaneous	1x CAN optional / 2x UART

*The TPM Option is only valid for commercial temperature grade modules

Kontron Features

External I2C Bus	Fast I2C, MultiMaster capable
M.A.R.S. support	YES
Embedded API	KEAPI1
Custom BIOS Settings / Flash Backup	YES
Watchdog support	Dual Staged

Additional features

» All solid capacitors (POSCAP). No tantalum capacitors used.

» Optimized RTC Battery monitoring to secure highest longevity

» Real fast I2C with transfer rates up to 40kB/s.

» Discharge logic on all onboard voltages for highest reliability

Power Features

Singly Supply Support	YES
Supply Voltage	4.75 - 14V
ACPI	ACPI 3.0
S-States	S0, S3, S4, S5
S5 Eco Mode	YES
Misc Power Management	DPST 3.2

Power Consumption and Performance

Full Load Power Consumption	5.2 - 7.5W
Kontron Performance Index	1833 - 4290
Kontron Performance/Watt	349 - 571

Detailed Power Consumption measurements in all states and bechmarks for CPU, Graphics and Memory performance are available in Application Note KEMAP054 at EMD Customer Section.

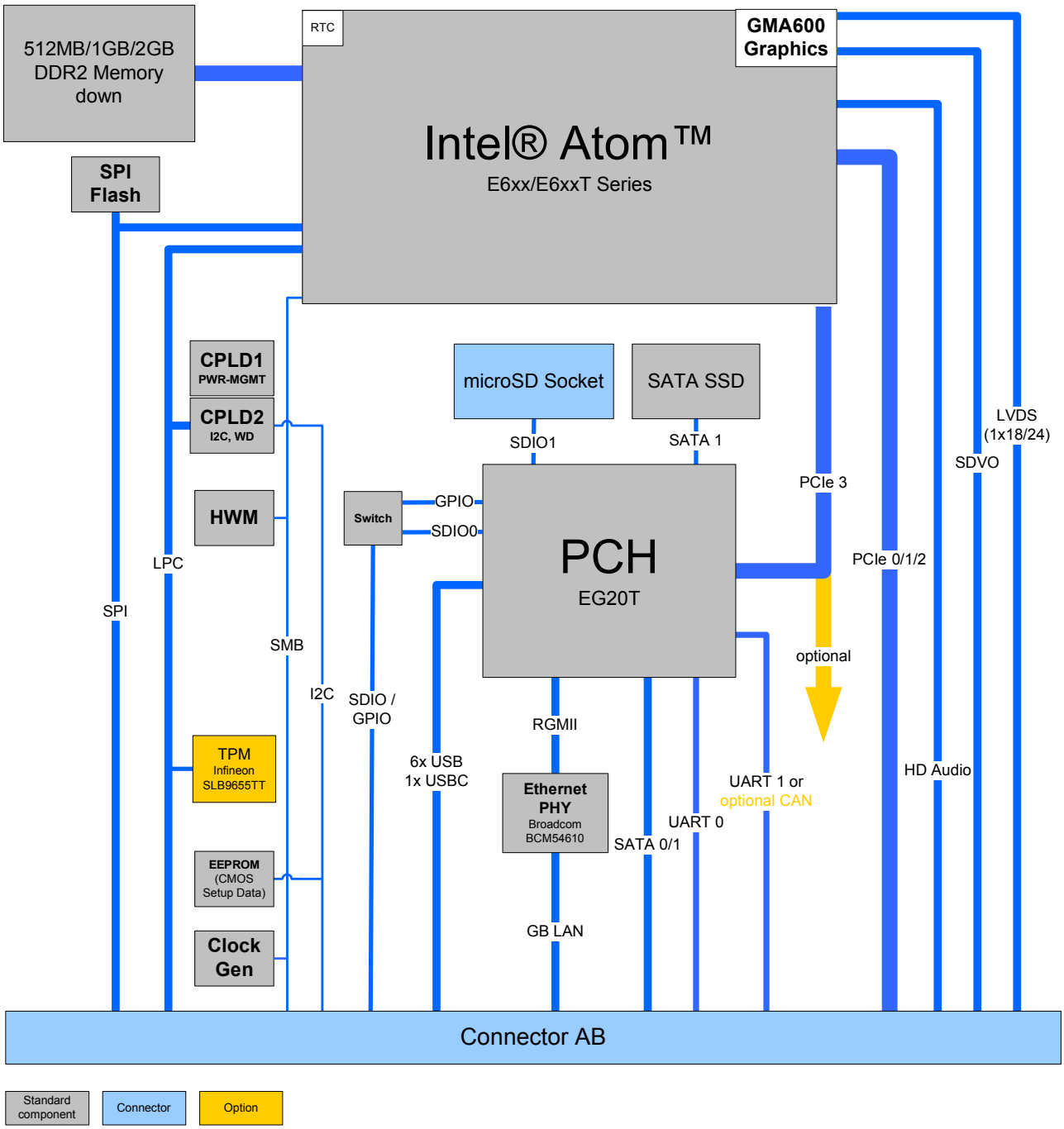
Real Time Clock

The E6xx CPU integrated RTC specifies a battery current up to 24µA. To secure a common longevity for external backup batteries Intel recommends to use following types in combination with E6xx.

Battery Type	Capacity	Typ. RTC current	Worst Case Battery Life*
Panasonic Lithium CR2032	225 mAh	24µA	1.1 yrs
Panasonic Lithium CR2450	620 mAh	24µA	2.9 yrs
Panasonic Lithium CR2477	1000 mAh	24µA	4.8 yrs

*RTC Battery life assuming CPU in S5 state 24/7 for 365 days.

3.3 Block Diagram



3.4 Electrical Specification

3.4.1 Supply Voltage

Following supply voltage is specified at the COM Express® connector:

VCC:	4.75 - 14V
Standby:	5V DC +/- 5%
RTC:	2.5V - 3.47V

- 5V Standby voltage is not mandatory for operation.
- Extended Temperature (E1) variants are validated for 12V supply only

3.4.2 Power Supply Rise Time

» The input voltages shall rise from ≤10% of nominal to within the regulation ranges within 0.1ms to 20ms.

» There must be a smooth and continuous ramp of each DC input voltage from 10% to 90% of its final set-point following the ATX specification

3.4.3 Supply Voltage Ripple

» Maximum 100 mV peak to peak 0 – 20 MHz

3.4.4 Power Consumption

The maximum Power Consumption of the different COMe-mTT10 variants is 5.2 - 7.5W (100% CPU load on all cores; 90°C CPU temperature). Further information with detailed measurements are available in Application Note KEMAP054 available on EMD Customer Section. Information there is available after registration.

3.4.5 ATX Mode

By connecting an ATX power supply with VCC and 5VSB, PWR_OK is set to low level and VCC is off. Press the Power Button to enable the ATX PSU setting PWR_OK to high level and powering on VCC. The ATX PSU is controlled by the PS_ON# signal which is generated by SUS_S3# via inversion. VCC can be 4.75 - 14V in ATX Mode. On Computer-on-Modules supporting a wide range input down to 4.75V the input voltage shall always be higher than 5V Standby (VCC > 5VSB).

State	PWRBTN#	PWR_OK	V5_StdBy	PS_ON#	VCC
G3	x	x	0V	x	0V
S5	high	low	5V	high	0V
S5 → S0	PWRBTN Event	low → high	5V	high → low	0 V→ VCC
S0	high	high	5V	low	VCC

3.4.6 Single Supply Mode

In single supply mode (or automatic power on after power loss) without 5V Standby the module will start automatically when VCC power is connected and Power Good input is open or at high level (internal PU to 3.3V). PS_ON# is not used in this mode and VCC can be 4.75 - 14V.

To power on the module from S5 state press the power button or reconnect VCC. Suspend/Standby States are not supported in Single Supply Mode.

State	PWRBTN#	PWR_OK	V5_StdBy	VCC
G3	x	x	x	0
G3 → S0	high	open / high	x	connecting VCC
S5	high	open / high	x	VCC
S5 → S0	PWRBTN Event	open / high	x	reconnecting VCC

Signals marked with “x” are not important for the specific power state. There is no difference if connected or open.

All ground pins have to be tied to the ground plane of the carrier board.

3.5 Power Control

Power Supply

The COMe-mTT10 supports a power input from 4.75 - 14V. The supply voltage is applied through the VCC pins (VCC) of the module connector.

Power Button (PWRBTN#)

The power button (Pin B12) is available through the module connector described in the pinout list. To start the module via Power Button the PWRBTN# signal must be at least 50ms (50ms ≤ t < 4s, typical 400ms) at low level (Power Button Event).

Pressing the power button for at least 4seconds will turn off power to the module (Power Button Override).

Power Good (PWR_OK)

The COMe-mTT10 provides an external input for a power-good signal (Pin B24). The implementation of this subsystem complies with the COM Express® Specification. PWR_OK is internally pulled up to 3.3V and must be high level to power on the module.

Reset Button (SYS_RESET#)

The reset button (Pin B49) is available through the module connector described in the pinout list. The module will stay in reset as long as SYS_RESET# is grounded. If available, the BIOS setting for “Reset Behavior” must be set to “Power Cycle”.

Modules with Intel® Chipset and active Management Engine do not allow to hold the module in Reset out of S0 for a long time. At about 10s holding the reset button the ME will reboot the module automatically

SM-Bus Alert (SMB_ALERT#)

With an external battery manager present and SMB_ALERT# (Pin B15) connected the module always powers on even if BIOS switch “After Power Fail” is set to “Stay Off”.

3.6 Environmental Specification

3.6.1 Temperature Specification

Kontron defines following temperature grades for Computer-on-Modules in general. Please see chapter 'Product Specification' for available temperature grades for the COMe-mTT10

Temperature Specification	Operating	Non-operating	Validated Input Voltage
Commercial grade	0°C to +60°C	-30°C to +85°C	VCC: 4.75 - 14V
Extended Temperature (E1)	-25°C to +75°C	-30°C to +85°C	VCC: 12V
Industrial grade by **Screening** (XT)	-40°C to +85°C	-40°C to +85°C	VCC: 12V
Industrial grade by **Design** (E2)	-40°C to +85°C	-40°C to +85°C	VCC: 4.75 - 14V

Operating with Kontron heatspreader plate assembly

The operating temperature defines two requirements:

» the maximum ambient temperature with ambient being the air surrounding the module.

» the maximum measurable temperature on any spot on the heatspreader's surface

Test specification:

Temperature Grade	Validation requirements
Commercial grade	at 60°C HSP temperature the CPU @ 100% load needs to run at nominal frequency
Extended Temperature (E1)	at 75°C HSP temperature the CPU @ 75% load is allowed to start speedstepping for thermal protection
Industrial grade by **Screening** (XT)	at 85°C HSP temperature the CPU @ 50% load is allowed to start throttling for thermal protection
Industrial grade by **Design** (E2)	at 85°C HSP temperature the CPU @ 50% load is allowed to start throttling for thermal protection

Operating without Kontron heatspreader plate assembly

The operating temperature is the maximum measurable temperature on any spot on the module's surface.

3.6.2 Humidity

» 93% relative Humidity at 40°C, non-condensing (according to IEC 60068-2-78)

3.7 Standards and Certifications

RoHS II

The **COMe-mTT10** is compliant to the directive 2011/65/EU on the Restriction of the use of certain Hazardous Substances (RoHS II) in electrical and electronic equipment

Component Recognition UL 60950-1

The **COM Express® mini** form factor Computer-on-Modules are Recognized by Underwriters Laboratories Inc. Representative samples of this component have been evaluated by UL and meet applicable UL requirements.

UL Listings:

» NWGQ2.E304278

» NWGQ8.E304278

WEEE Directive

WEEE Directive 2002/96/EC is not applicable for Computer-on-Modules.

Conformal Coating

Conformal Coating is available for Kontron Computer-on-Modules and for validated SO-DIMM memory modules. Please contact your local sales or support for further details.

Shock & Vibration

The **COM Express® mini** form factor Computer-on-Modules successfully passed shock and vibration tests according to

» IEC/EN 60068-2-6 (Non operating Vibration, sinusoidal, 10Hz-4000Hz, +/-0.15mm, 2g)

» IEC/EN 60068-2-27 (Non operating Shock Test, half-sinusoidal, 11ms, 15g)

EMC

Validated in Kontron reference housing for EMC the **COMe-mTT10** follows the requirements for electromagnetic compatibility standards

» EN55022

PTCRB

The COMe-mTT10 is PTCRB certified within Kontron KM2M800 M2M

3.8 MTBF

The following MTBF (Mean Time Before Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and the Telcordia (Bellcore) issue 2 calculation for the remaining parts.

The calculation method used is "Telcordia Issue 2 Method 1 Case 3" in a ground benign, controlled environment (GB,GC). This particular method takes into account varying temperature and stress data and the system is assumed to have not been burned in.

Other environmental stresses (extreme altitude, vibration, salt water exposure, etc) lower MTBF values.

System MTBF (hours): 34003*: 238615 @ 40°C (w/PCB)

34004*: 241971 @ 40°C (w/PCB)

Fans usually shipped with Kontron Europe GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

3.9 Mechanical Specification

Module Dimension

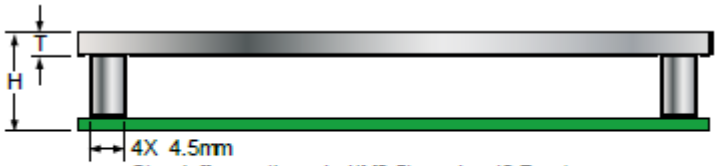
» 55mm x 84mm (±0.2mm)

» Height approx. 3.5mm (withouth printed circuit board)

CAD drawings are available at EMD CustomerSection

Height

The COM Express® specification defines a module height of 13mm from bottom to heatspreader top:



Thickness 'T' is implemantation specific and may be 3mm.
Height 'H' (which includes PCB thickness) shall be 13.00mm

Kontron provides standard HSP for the specified height of 13mm and slim-line Heatspreader for a reduced height of 8.5mm for mini sized Computer-on-Modules. Universal Cooling solutions to be mounted on the HSP are 14.3mm (34099-0000-00-0/1) or 8mm (34099-0000-00-2) in height. This allows combinations of a total module height of 8.5mm or 13mm with the Heatspreader and between 16.5mm and 27.3mm with a cooling solution.

3.10 Thermal Management, Heatspreader and Cooling Solutions

A heatspreader plate assembly is available from Kontron Europe GmbH for the COMe-mTT10. The heatspreader plate on top of this assembly is NOT a heat sink. It works as a COM Express®-standard thermal interface to use with a heat sink or external cooling devices.

External cooling must be provided to maintain the heatspreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heatspreader plate temperature on any spot of the heatspreader's surface according the module specifications:

- 60°C for commercial grade modules
- 75°C for extended temperature grade modules (E1)
- 85°C for industrial temperature grade modules (E2/XT)

The aluminum slugs and thermal pads or the heat-pipe on the underside of the heatspreader assembly implement thermal interfaces between the heatspreader plate and the major heat-generating components on the COMe-mTT10. About 80 percent of the power dissipated within the module is conducted to the heatspreader plate and can be removed by the cooling solution.

You can use many thermal-management solutions with the heatspreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COM Express® application and environmental conditions. Active or passive cooling solutions provided from Kontron Europe GmbH for the COMe-mTT10 are usually designed to cover the power and thermal dissipation for a commercial grade temperature range used in a housing with proper air flow.

Documentation and CAD drawings of COMe-mTT10 heatspreader and cooling solutions are provided at http://emdcustomersection.kontron.com.

4 Features and Interfaces

4.1 Onboard SSD

The COMe-mTT10 features an onboard Greenliant SATA NAND flash drive with capacities of 2-32GB SLC, 2-64GB MLC (SATA). Due to performance and longevity reasons standard variants with onboard flash use SLC type only. The following SATA NANDrives are available:

Basic features of the SATA NANDrives

» ATA/ATAPI-8 compliant Host interface with 48-bit address feature set and SMART support

» RoHS compliant NAND flash type

» SATA 1.5Gb/s Host transfer rate

» Hardware error detection, correction ECC and advanced wear leveling

» Bad block management

» TRIM support

» SMART support

» 0°C to +70°C temperature range for MLC types A-M-C/B-M-C

» -40°C to +85°C temperature range for MLC types B-M-I

» -40°C to +85°C temperature range for all SLC types

Single-level Cell (SLC) NANDrive™

Flash Part No.	GLS85LS				
Flash Part No.	1002P-S-I-FZJE-ND104	1004P-S-I-FZJE-ND104	1008P-S-I-FZJE-ND104	1016P-S-I-FZJE-ND104	1032P-S-I-FZJE-ND104
Product Revision	CC1	CC1	CC1	CC1	CC1
Flash Size	**2GByte**	**4GByte**	**8GByte**	**16GByte**	**32GByte**
Burst Read/Write Speed	35/20 MB/s	70/35 MB/s	70/50 MB/s	70/55 MB/s	120/80 MB/s
Total Bytes	2,000,388,096	4,001,292,288	8,012,390,400	16,013,942,784	32,017,047,552
Active Mode Power	450mW	560mW	750mW	590mW	855mW
Typical P/E Cycles per block	100,000	100,000	60,000	60,000	60,000

(Data based on Datasheet S71432 Rev. 03.100 from 11-2013 and S71445 Rev. 01.400 from 11-2013)

Multi-level Cell (MLC) NANDrive™

Flash Part No.	GLS85LS					
Flash Part No.	1002A-M-C-FZJE-ND103 1002A-M-I-FZJE-ND103	1004A-M-C-FZJE-ND103 1004A-M-I-FZJE-ND103	1008B-M-C-FZJE-ND103 1008B-M-I-FZJE-ND103	1016B-M-C-FZJE-ND103 1016B-M-I-FZJE-ND103	1032B-M-C-FZJE-ND103 1032B-M-I-FZJE-ND103	1064B-M-C-FZJE-ND103 1064B-M-I-FZJE-ND103
Product Revision	CB2	CB2	CB2	CB2	CB2	CB2
Flash Size	**2GByte**	**4GByte**	**8GByte**	**16GByte**	**32GByte**	**64GByte**
Burst Read/Write Speed	35/10 MB/s	35/10 MB/s	35/10 MB/s	70/20 MB/s	70/30 MB/s	110/60 MB/s
Total Bytes	1,941,553,152	3,941,941,248	8,012,390,400	16,013,942,784	32,017,047,552	64,023,257,088
Active Mode Power	360mW	360mW	360mW	440mW	565mW	820mW
Typical P/E Cycles per block	5,000	5,000	5,000	5,000	5,000	5,000

(Data based on Datasheet S71430 Rev 02.00 from 10-2013)

4.2 S5 Eco Mode

Kontron's new high-efficient power-off state S5 Eco enables lowest power-consumption in soft-off state – less than 1 mA compared to the regular S5 state this means a reduction by at least factor 200!

In the "normal" S5 mode the board is supplied by 5V_Stb and needs usually up to 300mA just to stay off. This mode allows to be switched on by power button, RTC event and WakeOnLan, even when it is not necessary. The new S5 Eco mode reduces the current enormous.

The S5 Eco Mode can be enabled in BIOS Setup, when the BIOS supports this feature.

Following prerequisites and consequences occur when S5 Eco Mode is enabled

» The power button must be pressed at least for 200ms to switch on.

» Wake via Power button only.

» "Power On After Power Fail"/"State after G3": only "stay off" is possible

4.3 LPC

The Low Pin Count (LPC) Interface signals are connected to the LPC Bus bridge located in the CPU or chipset. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combines legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® Specification. Implementation information is provided in the COM Express® Design Guide maintained by PICMG. Please refer to the official PICMG documentation for additional information.

The LPC bus does not support DMA (Direct Memory Access) and a clock buffer is required when more than one device is used on LPC. This leads to limitations for ISA bus and SIO (standard I/O´s like Floppy or LPT interfaces) implementations.

All Kontron COM Express® Computer-on-Modules imply BIOS support for following external baseboard LPC Super I/O controller features for the **Winbond/Nuvoton 5V 83627HF/G and 3.3V 83627DHG-P**:

83627HF/G	Phoenix BIOS	AMI CORE8	AMI / Phoenix EFI
PS/2	YES	YES	YES
COM1/COM2	YES	YES	YES
LPT	YES	YES	YES
HWM	YES	YES	NO
Floppy	NO	NO	NO
GPIO	NO	NO	NO
83627DHG-P	**Phoenix BIOS**	**AMI CORE8**	**AMI / Phoenix EFI**
PS/2	YES	YES	YES
COM1/COM2	YES	YES	YES
LPT	YES	YES	YES
HWM	NO	NO	NO
Floppy	NO	NO	NO
GPIO	NO	NO	NO

Features marked as not supported do not exclude OS support (e.g. HWM can be accessed via SMB). For any other LPC Super I/O additional BIOS implementations are necessary. Please contact your local sales or support for further details.

4.4 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines. Sometimes SPI is called a “four wire” serial bus, contrasting with three, two, and one wire serial buses.

The SPI interface can only be used with a SPI flash device to boot from external BIOS on the baseboard.

4.5 SPI boot

The COMe-mTT10 supports boot from an external SPI Flash. It can be configured by pin A34 (BIOS_DIS#0) and pin B88 (BIOS_DIS1#) in following configuration:

BIOS_DIS0#	BIOS_DIS1#	Function
open	open	Boot on-module BIOS
GND	open	Boot baseboard LPC FWH
open	GND	Baseboard SPI = Boot Device 1, on-module SPI = Boot Device 2
GND	GND	Baseboard SPI = Boot Device 2, on-module SPI = Boot Device 1

By default only SPI Boot Device 1 is used in configuration 3 & 4. Both SPI Boot Devices are used by splitting the BIOS with modified descriptor table in customized versions only

Recommended SPI boot flash types for 8-SOIC package

Size	Manufacturer	Part Number	Device ID
16Mbit	Atmel	AT26DF161	0x1F4600
16Mbit	Atmel	AT26DF161A	0x1F4601
16Mbit	Atmel	AT25DF161	0x1F4602
16Mbit	Atmel	AT25DQ161	0x1F8600
16Mbit	Macronix	MX25L1605A(D)(36E)(06E)	0xC22015
16Mbit	Macronix	MX25L1635D	0xC22415
16Mbit	SST/Microchip	SST25VF016B	0xBF2541
16Mbit	Winbond	W25X16BV	0xEF3015
16Mbit	Winbond	W25Q16BV(CV)	0xEF4015
Size	**Manufacturer**	**Part Number**	**Device ID**
32Mbit	Atmel	AT25/26DF321	0x1F4700
32Mbit	Atmel	AT25DF321A	0x1F4701
32Mbit	Macronix	MX25L3205A(D)(06E)	0xC22016
32Mbit	Macronix	MX25L3225D(35D)(36D)	0xC25E16
32Mbit	SST/Microchip	SST25VF032B	0XBF254A
32Mbit	Winbond	W25X32BV	0xEF3016
32Mbit	Winbond	W25Q32BV,	0xEF4016
Size	**Manufacturer**	**Part Number**	**Device ID**
64Mbit	Atmel	AT25DF641(A)	0x1F4800
64Mbit	Atmel	AT25DQ641	0x1F8800
64Mbit	Macronix	MX25L6405D(45E)(36E)(06E)(73E)	0xC22017
64Mbit	Macronix	MX25L6455E	0xC22617
64Mbit	Macronix	MX25U6435F	0xC22537
64Mbit	SST/Microchip	SST25VF064C	0xBF254B
64Mbit	Winbond	W25X64BV	0xEF3017
64Mbit	Winbond	W25Q64BV(CV)(FV)	0xEF4017
64Mbit	Winbond	W25Q64DW	0XEF6017
64Mbit	Winbond	W25Q64FW	0XEF6017

Using an external SPI flash

To program an external SPI flash follow these steps:

» Connect a SPI flash with correct size (similar to BIOS ROM file size) to the module SPI interface

» Open pin A34 and B88 to boot from the module BIOS

» Boot the module to DOS/EFI-Shell with access to the BIOS image and Firmware Update Utility provided on EMD Customer Section

» Connect pin B88 (BIOS_DIS1#) to ground to enable the external SPI flash

» Execute Flash.bat/Flash.efi to program the complete BIOS image to the external SPI flash

» reboot

Your module will now boot from the external SPI flash when BIOS_DIS1# is grounded.

External SPI flash on Modules with Intel® ME

If booting from the external (baseboard mounted) SPI flash then exchanging the COM Express® module for another one of the same type will cause the Intel® Management Engine to fail during next start. This is by design of the ME because it bounds itself to the very module it has been flashed to. In the case of an external SPI flash this is the module present at flash time.

To avoid this issue please make sure to conduct a complete flash of the external SPI flash device after changing the COMexpress module for another one. If disconnecting and reconnecting the same module again this step is not necessary.

4.6 M.A.R.S.

The Smart Battery implementation for Kontron Computer-on-Modules called **M**obile **A**pplication for **R**echargeable **S**ystems is a BIOS extension for external Smart Battery Manager or Charger. It includes support for SMBus charger/selector (e.g. Linear Technology LTC1760 Dual Smart Battery System Manager) and provides ACPI compatibility to report battery information to the Operating System.

Reserved SM-Bus addresses for Smart Battery Solutions on the carrier:

8-bit Address	7-bit Address	Device
12h	0x09	SMART_CHARGER
14h	0x0A	SMART_SELECTOR
16h	0x0B	SMART_BATTERY

4.7 UART

The COMe-mTT10 supports two Serial RX/TX only UART Ports defined in COM Express® specification on Pins A98/A99 for UART0 and Pins A101/A102 for UART1. The 16550 compatible UARTs are provided from the - and resources are subordinated to other UARTS e.g. from external LPC Super I/O.

UART features:

» 9600 to 115.2k Baud

» 8bit Word length

» 1 Stop bit

» Odd, even or no parity support

» 256byte FIFO Buffer for UART0

» 64byte FIFO Buffer for UART1

» Hardware Flow Control on UART0

» Initialized per default to COM3 3F8h/IRQ4 and COM4 2F8/IRQ3 without external SIO

» Initialized per default to COM3 3E8h/IRQ5 and COM4 2E8/IRQ10 with external SIO present

Due to the protection circuitry required according COM Express® specification the transfer speed can only be guaranteed for 9600 Baud. Please contact your local sales or support for customized versions without protection circuitry

4.8 CAN

The COMe-mTT10 optionally supports the EG20T implemented CAN interface as defined in COM Express® specification on Pins Pins A101/A102 instead of UART1. To connect the CAN interface from the module to the CAN bus, it is necessary to add transceiver hardware on the Carrier Board.

CAN Controller features:

» CAN Protocol Version 2.0B Active

» Supports bit rate up to 1Mbit/second

» Supports 32 message objects

» Programmable FIFO

4.9 Fast I2C

The COMe-mTT10 supports a CPLD implemented LPC to I2C bridge using the WISHBONE I2C Master Core provided from opencores.org. The I2C Interface supports transfer rates up to 40kB/s and can be configured in Setup

Specification for external I2C:

» Speed up to 400kHz

» Compatible to Philips I2C bus standard

» Multi-Master capable

» Clock stretching support and wait state generation

» Interrupt or bit-polling driven byte-by-byte data-transfers

» Arbitration lost interrupt with automatic transfer cancellation

» Start/Stop signal generation/detection

» Bus busy detection

» 7bit and 10bit addressing

4.10 GPIO - General Purpose Input and Output

The COMe-mTT10 offers 4 General Purpose Input (GPI) pins and 4 General Purpose Output (GPO) pins. On a 3.3V level digital in- and outputs are available.

Signal	Pin	Description
GPI0	A54	General Purpose Input 0
GPI1	A63	General Purpose Input 1
GPI2	A67	General Purpose Input 2
GPI3	A85	General Purpose Input 3
GPO0	A93	General Purpose Output 0
GPO1	B54	General Purpose Output 1
GPO2	B57	General Purpose Output 2
GPO3	B63	General Purpose Output 3

Configuration

The GPI and GPO pins can be configured via JIDA32/K-Station. Please refer to the JIDA32/K-Station manual in the driver download packet on our customer section.

4.11 Dual Staged Watchdog Timer

Basics

A watchdog timer (or computer operating properly (COP) timer) is a computer hardware or software timer that triggers a system reset or other corrective action if the main program, due to some fault condition, such as a hang, neglects to regularly service the watchdog (writing a “service pulse” to it, also referred to as “kicking the dog”, “petting the dog”, “feeding the watchdog” or “triggering the watchdog”). The intention is to bring the system back from the nonresponsive state into normal operation.

The COMe-mTT10 offers a watchdog which works with two stages that can be programmed independently and used one by one.

Time-out events

Reset	A reset will restart the module and starts POST and operating system new.
NMI	A non-maskable interrupt (NMI) is a computer processor interrupt that cannot be ignored by standard interrupt masking techniques in the system. It is typically used to signal attention for non-recoverable hardware errors.
SCI	A system control interrupt (SCI) is a OS-visible interrupt to be handled by the OS using AML code
Delay	Might be necessary when an operating system must be started and the time for the first trigger pulse must extended. (Only available in the first stage)
WDT Signal only	This setting triggers the WDT Pin on baseboard connector (COM Express® Pin B27) only
Cascade:	Does nothing, but enables the 2nd stage after the entered time-out.

WDT Signal

B27 on COM Express® Connector offers a signal that can be asserted when a watchdog timer has not been triggered within time. It can be configured to any of the 2 stages. Deassertion of the signal is automatically done after reset. If deassertion during runtime is necessary please ask your Kontron technical support for further help.

4.12 Speedstep Technology

The Intel® processors offer the Intel® Enhanced SpeedStep™ technology that automatically switches between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. It enables you to adapt high performance computing on your applications. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage, conserving battery life while maintaining a high level of performance. The frequency is set back automatically to the high frequency, allowing you to customize performance.

In order to use the Intel® Enhanced SpeedStep™ technology the operating system must support SpeedStep™ technology.

By deactivating the SpeedStep feature in the BIOS, manual control/modification of CPU performance is possible. Setup the CPU Performance State in the BIOS Setup or use 3rd party software to control CPU Performance States.

4.13 C-States

New generation platforms include power saving features like SuperLFM, EIST (P-States) or C-States in O/S idle mode.

Activated C-States are able to dramatically decrease power consumption in idle mode by reducing the Core Voltage or switching of parts of the CPU Core, the Core Clocks or the CPU Cache.

Following C-States are defined:

C-State	Description	Function
C0	Operating	CPU fully turned on
C1	Halt State	Stops CPU main internal clocks via software
C1E	Enhanced Halt	Similar to C1, additionally reduces CPU voltage
C2	Stop Grant	Stops CPU internal and external clocks via hardware
C2E	Extended Stop Grant	Similar to C2, additionally reduces CPU voltage
C3	Deep Sleep	Stops all CPU internal and external clocks
C3E	Extended Stop Grant	Similar to C3, additionally reduces CPU voltage
C4	Deeper Sleep	Reduces CPU voltage
C4E	Enhanced Deeper Sleep	Reduces CPU voltage even more and turns off the memory cache
C6	Deep Power Down	Reduces the CPU internal voltage to any value, including 0V
C7	Deep Power Down	Similar to C6, additionally LLC (LastLevelCache) is switched off

C-States are usually enabled by default for low power consumption, but active C-States my influence performance sensitive applications or real-time systems.

» Active C6-State may influence data transfer on external Serial Ports

» Active C7-State may cause lower CPU and Graphics performance

It's recommended to disable C-States / Enhanced C-States in BIOS Setup if any problems occur.

4.14 Hyper Threading

Hyper Threading (officially termed Hyper Threading Technology or HTT) is an Intel®-proprietary technology used to improve parallelization of computations performed on PC´s. Hyper-Threading works by duplicating certain sections of the processor—those that store the architectural state but not duplicating the main execution resources. This allows a Hyper-Threading equipped processor to pretend to be two “logical” processors to the host operating system, allowing the operating system to schedule two threads or processes simultaneously. Hyper Threading Technology support always relies on the Operating System.

4.15 ACPI Suspend Modes and Resume Events

The COMe-mTT10 supports the S-states S0, S3, S4, S5. S5eco Support: YES

The following events resume the system from S3:

» USB Keyboard (1)

» USB Mouse (1)

» Power Button

» WakeOnLan (2)

The following events resume the system from S4:

» Power Button

» WakeOnLan (2)

The following events resume the system from S5:

» Power Button

» WakeOnLan (2)

The following events resume the system from S5Eco:

» Power Button

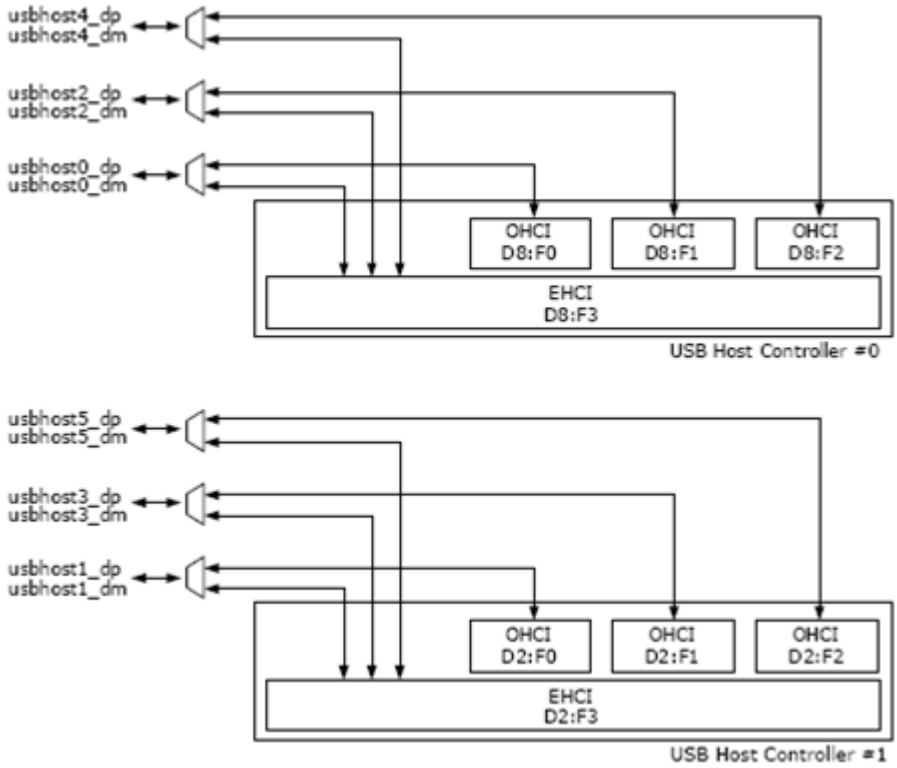
(1) OS must support wake up via USB devices and baseboard must power the USB Port with StBy-Voltage
(2) Depending on the Used Ethernet MAC/Phy WakeOnLan must be enabled in BIOS setup and driver options

4.16 USB

The available USB configuration of the COMe-mTT10 module is described in the following table:

COM Express Port	EG20 Port	Comment
USB0	USB0	-
USB1	USB1	-
USB2	USB2	-
USB3	USB3	-
USB4	USB4	-
USB5	USB5	-
USB6	USB5	Optional instead of COMe USB#5
USB7	USB Client	USB Client only

Internal USB mapping



4.17 SDIO

The SD card standard is a standard for removable memory storages designed and licensed by the SD Card Association (http://sdcard.org). The card form factor, electrical interface, and protocol are all part of the SD Card specification. The Intel® Platform Controller Hub EG20T supports 2 SDIO interfaces. On nanoETXexpress-TT the first interface SDIO#0 is shared with the module GPIO signals. On modules without SATA SSD the second EG20T SDIO interface SDIO#1 is available via onboard microSD connector.

The integrated SD Host Controller conforms to SD Host Controller Standard Specification Ver. 1.0.

Features:

» SDHC up to speed class 6

» SDIO Card Specification Ver. 1.10

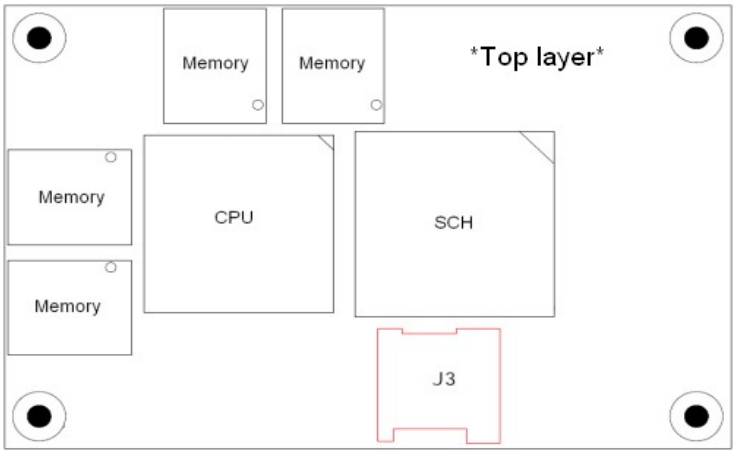
» MMC System Specification Ver. 4.1

» SD bus transfer mode

» MMC transfer mode

SDIO interface on COM Express connector:

General purpose Input/output	SD card interface signals
GPI0	SLOT0_DATA0
GPI1	SLOT0_DATA1
GPI2	SLOT0_DATA2
GPI3	SLOT0_DATA3
GPO0	SLOT0_CLK
GPO1	SLOT0_CMD
GPO2	SLOT0_WP
GPO3	SLOT0_CD#



onboard microSD connector J3

Pin	Pin name	Signal
1	DAT2	SDIO1_DAT0
2	CD/DAT3	SDIO1_DAT3
3	CMD	SDIO1_CMD
4	VDD	3.3V S0
5	CLK	SDIO1_CLK
6	VSS2	GND
7	DAT0	SDIO1_DAT1
8	DAT1	SDIO1_DAT2
9	SWITCH1	SDIO1_CD#
10	SWITCH2	GND
11	SHIELD1	GND
12	SHIELD2	GND
13	SHIELD3	GND
14	SHIELD4	GND
15	SHIELD5	GND

- The SD_CMD line needs a pull-up resistor that can vary depending on the length of the electrical paths (typical from 10kOhm to 100kOhm)
- The maximum length for SDIO signals on the baseboard should be 80mm.

5 System Resources

5.1 Interrupt Request (IRQ) Lines

5.1.1 In 8259 PIC mode

IRQ #	Used For	Available	Comment
0	Timer0	No	-
1	Keyboard	No	-
2	Cascade	No	-
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	PCI	Yes (No)	Note (1)
7	External SIO - LPT1	for PCI	Dynamic (BIOS default)
8	RTC	No	-
9	ACPI	No	Note (2)
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	-
14	PCI	for PCI	Dynamic (BIOS default)
15	PCI	for PCI	Dynamic (BIOS default)

1 If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.
2 Not available if ACPI is used

5.1.2 In APIC mode

IRQ #	Used For	Available	Comment
0	Timer0	No	-
1	Keyboard	No	-
2	Cascade	No	-
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	PCI	for PCI	Dynamic (BIOS default)
7	External SIO - LPT1	Yes (No)	Note (1)
8	RTC	No	-
9	ACPI	No	Note (2)
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	-
14	PCI	for PCI	Dynamic (BIOS default)
15	PCI	for PCI	Dynamic (BIOS default)
16	PIRQ[A]	No	PCI IRQ line 1 + US15W graphics + USB UHCI Controller #1; Note(3)
17	PIRQ[B]	No	PCI IRQ line 2 + LAN Controller + USB UHCI Controller #2; Note(3)
18	PIRQ[C]	No	PCI IRQ line 3 + USB UHCI Controller #3; Note(3)
19	PIRQ[D]	No	PCI IRQ line 4 + USB UHCI Controller #4; Note(3)
20	PIRQ[E]	No	Note(3)
21	PIRQ[F]	No	Note(3)
22	PIRQ[G]	No	Note(3)
23	PIRQ[H]	No	Note(3)

(1) If the "Used For" device is disabled in setup, the corresponding interrupt is available for other device.
(2) Not available if ACPI is used
(3) ACPI OS decides on particular IRQ usage

5.2 Memory Area

The first 640 kB of DRAM are used as main memory. Using DOS, you can address 1 MB of memory directly. Memory area above 1 MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for infor- mation about HIMEM.SYS and EMM386.EXE. Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Used for	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic controller
C0000h – CFFFFh	VGA BIOS	No	Used by onboard VGA ROM
D0000h – DFFFFh	-	Yes	Free for shadow RAM in standard configurations.
E0000h – FFFFFh	System BIOS	No	Fixed
E0000000h – F0000000h	PCIe Config Space	No	Fixed
FEC00000h-FEC00040h	IOxAPIC	No	Fixed
FED00000h FED003FFh	HPET	No	Fixed
FED04000 FED4BFFF	TPM	No	Fixed
FFC00000h - FFFFFFFFh	BIOS Flash	No	Fixed

5.3 I/O Address Map

The I/O-port addresses of the are functionally identical to a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0100h with additional hardware for compatibility reasons, even if available.

I/O Address	Used for	Available	Comment
0000 - 001F	System Ressources	No	Fixed
0020 - 003F	Interrupt Controller 1	No	Fixed
0040 - 005F	Timer, Counter	No	Fixed
0060 - 006F	Keyboard controller	No	Fixed
0070 - 007F	RTC and CMOS Registers	No	Fixed
0080	BIOS Postcode	No	Fixed
0084 - 008F	DMA Page Register	No	Fixed
0090 - 009F	System Control	No	Fixed
00A0 - 00BF	Interrupt Controller	No	Fixed
00E0 - 00EF	System Control	No	Fixed
00F0 - 00FF	Math Coprocessor	No	Fixed
03B0 - 03DF	VGA	No	Fixed
0400 - 043F	Chipset	No	Fixed
0480 - 04BF	Chipset	No	Fixed
04D0 - 04D1	Chipset	No	Fixed
0900 - 091F	Power Management	No	Fixed
09C0 - 09FF	GPE	No	Fixed
0A05 – 0A06	WB83627HG Hardware Monitor	No	Fixed if WB83627HG is in system
0A80 – 0A81	CPLD	No	Fixed
0CF8 - 0CFF	PCI Configuration	No	Fixed

5.4 Peripheral Component Interconnect (PCI) Devices

All devices follow the Peripheral Component Interconnect 2.3 (PCI 2.3) respectivily the PCI Express Base 1.0a specification. The BIOS and OS control memory and I/O resources. Please see the PCI 2.3 specification for details.

PCI Device	B:D:F	PCI IRQ	Interface	Comment
Host Bridge	0:0:0	None	internal	Chipset (Tunnelcreek)
Video Controller	0:2:0	INTA	internal	Chipset (Tunnelcreek)
SDVO Controller	0:03:0	INTA	internal	Chipset (Tunnelcreek)
PCIe Port 0	0:23:0	INTA	internal	Chipset (Tunnelcreek)
PCIe Port #0 Slot	-	A/B/C/D	PCIe	Slot #1
PCIe Port 1	0:24:0	INTA	internal	Chipset (Tunnelcreek)
PCIe Port #1 Slot	-	B/C/D/A	PCIe	Slot #2
PCIe Port 2	0:25:0	INTA	internal	Chipset (Tunnelcreek)
PCIe Port #2 Slot	-	C/D/A/B	PCIe	Slot #3
PCIe Port 3	0:26:0	INTA	internal	Chipset (Tunnelcreek)
HDA Controller	0:27:0	INTA	internal	Chipset (Tunnelcreek)
LPC Bridge	0:31:0	-	internal	Chipset (Tunnelcreek)
PCIe-PORT	X:00:0	INTD	PCIe	Chipset (Topcliff)
Packet Hub	Y:00:0	-	PCIe	Chipset (Topcliff)
GbE	Y:00:1	INTD	PCIe	Chipset (Topcliff)
GPIO	Y:00:2	INTD	PCIe	Chipset (Topcliff)
OHCI00	Y:02:0	INTC	PCIe	Chipset (Topcliff)
OHCI01	Y:02:1	INTC	PCIe	Chipset (Topcliff)
OHCI02	Y:02:2	INTC	PCIe	Chipset (Topcliff)
EHCI0	Y:02:3	INTC	PCIe	Chipset (Topcliff)
USB Device	Y:02:4	INTC	PCIe	Chipset (Topcliff)
SDIO #0	Y:04:0	INTB	PCIe	Chipset (Topcliff)
SDIO #1	Y:04:1	INTB	PCIe	Chipset (Topcliff)
SATA II	Y:06:0	INTA	PCIe	Chipset (Topcliff)
OHCI10	Y:08:0	INTD	PCIe	Chipset (Topcliff)
OHCI11	Y:08:1	INTD	PCIe	Chipset (Topcliff)
OHCI12	Y:08:2	INTD	PCIe	Chipset (Topcliff)
EHCI1	Y:08:3	INTD	PCIe	Chipset (Topcliff)
DMA0	Y:10:0	INTC	PCIe	Chipset (Topcliff)
UART #0	Y:10:1	INTC	PCIe	Chipset (Topcliff)
UART #1	Y:10:2	INTC	PCIe	Chipset (Topcliff)
UART #2	Y:10:3	INTC	PCIe	Chipset (Topcliff)
UART #3	Y:10:4	INTC	PCIe	Chipset (Topcliff)
DMA1	Y:12:0	INTB	PCIe	Chipset (Topcliff)
SPI	Y:12:1	INTB	PCIe	Chipset (Topcliff)
I2C	Y:12:2	INTB	PCIe	Chipset (Topcliff)
CAN	Y:12:3	INTB	PCIe	Chipset (Topcliff)
IEEE1588 block	Y:12:4	INTB	PCIe	Chipset (Topcliff)

5.5 I2C Bus

I2C Address	Used For	Available	Comment
58h	S5 Eco	No	S5 Eco Resistor
A0h	JIDA-EEPROM	No	Module EEPROM
AEh	FRU-EEPROM	No	Baseboard EEPROM

Do not access the digital potentiometer manually

5.6 JILI I2C Bus

I2C Address	Used For	Available	Comment
A0h	JILI-EEPROM	No	EEPROM for JILI Data

5.7 SDVO I2C Bus

I2C Address	Used For	Available	Comment
-	-	-	-

5.8 System Management (SM) Bus

Address	Device	Comment
12h	SMART_CHARGER	Not to be used with any SM bus deivce except a charger
14h	SMART_SELECTOR	Not to be used with any SM bus deivce except a selector or manager
16h	SMART_BATTERY	Not to be used with any SM bus deivce except a battery
98h	Winbond W83771W HWM	Do not use under any circumstances
A0h	SPD EEPROM	Do not use under any circumstances
D2h	Clock Generator	Do not use under any circumstances

6 Pinout List

6.1 General Signal Description

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1,8V Output
O-3,3	3,3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection

To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfills the fire-protection requirements of IEC/EN60950

6.2 Connector X1A Row A

Pin	Signal	Description	Type	Termination	Comment
A1	GND_1	Power Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet Receive Data-	DP-I	-	-
A3	GBE0_MDI3+	Ethernet Receive Data+	DP-I	-	-
A4	GBE0_LINK100#	Ethernet Speed LED 100Mbps	OD	-	-
A5	GBE0_LINK1000#	Ethernet Speed LED 1000Mbps	OD	-	-
A6	GBE0_MDI2-	Ethernet Receive Data-	DP-I	-	-
A7	GBE0_MDI2+	Ethernet Receive Data+	DP-I	-	-
A8	GBE0_LINK#	LAN Link LED	OD	-	-
A9	GBE0_MDI1-	Ethernet Receive Data-	DP-I	-	-
A10	GBE0_MDI1+	Ethernet Receive Data+	DP-I	-	-
A11	GND_2	Power Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet Transmit Data-	DP-O	-	-
A13	GBE0_MDI0+	Ethernet Transmit Data+	DP-O	-	-
A14	GBE0_CTREF	LAN Reference Voltage	O-3.3	100nF to GND	-
A15	SUS_S3#	Indicates Suspend to RAM state	O-3.3	-	CPLD I/O
A16	SATA0_TX+	SATA 0 Transmit Data+	DP-O	-	-
A17	SATA0_TX-	SATA 0 Transmit Data-	DP-O	-	-
A18	SUS_S4#	Indicates Suspend to Disk state; same as SUS_S5#	O-3.3	-	CPLD I/O
A19	SATA0_RX+	SATA 0 Receive Data+	DP-I	-	-
A20	SATA0_RX-	SATA 0 Receive Data-	DP-I	-	-
A21	GND_3	Power Ground	PWR	-	-
A22	RSVD	Not Connected	nc	-	-
A23	RSVD	Not Connected	nc	-	-
A24	SUS_S5#	Indicates Soft Off state; same function as SUS_S4#	O-3.3	-	CPLD I/O
A25	RSVD	Not Connected	nc	-	-
A26	RSVD	Not Connected	nc	-	-
A27	BATLOW#	Indicates low external battery (not implemented)	I-3.3	-	CPLD I/O
A28	ATA_ACT#	SATA Activity Indicator	OD	-	-
A29	HDA_SYNC	HD Audio SYNC	O-3.3	-	-
A30	HDA_RST#	HD Audio Reset	O-3.3	-	-
A31	GND_4	Power Ground	PWR	-	-
A32	HDA_CLK	HD Audio CLK	O-3.3	PD ~10k in TNC	24MHz
A33	HDA_SDOUT	HD Audio Data	O-3.3	-	-
A34	BIOS_DIS0#	Disable Module BIOS.Enable boot from a FWH on Baseboard	I-3.3	PU ~15k in CPLD 3.3V_S5	For ext.LPC FWH
A35	THRMTRIP#	CPU thermal shutdown indicator	O-3.3	PU 10k 3.3V_S0	-
A36	USB6-	USB Data- Port #6 (optional)	DP-I/O	PD 12k in Topcliff	-
A37	USB6+	USB Data+ Port #6 (optional)	DP-I/O	PD 12k in Topcliff	-
A38	USB_6_7_OC#	USB Over current Pair 4 / 5 / 6	I-3.3	PU 10k 3.3V_S5	-
A39	USB4-	USB Data- Port #4	DP-I/O	PD 12k in Topcliff	-
A40	USB4+	USB Data+ Port #4	DP-I/O	PD 12k in Topcliff	-
A41	GND_5	Power Ground	PWR	-	-
A42	USB2-	USB Data- Port #2	DP-I/O	PD 12k in Topcliff	-
A43	USB2+	USB Data+ Port #2	DP-I/O	PD 12k in Topcliff	-
A44	USB_2_3_OC#	USB Over current Pair 2 / 3	I-3.3	PU 10k 3.3V_S5	-
A45	USB0-	USB Data- Port #0	DP-I/O	PD 12k in Topcliff	-
A46	USB0+	USB Data+ Port #0	DP-I/O	PD 12k in Topcliff	-
A47	VCC_RTC	RTC Battery Supply +3V	PWR	-	-
A48	EXCD0_PERST#	PCI Express Card 0 Reset	O-3.3	no PU/PD allowed!	-
A49	EXCD0_CPPE#	PCI Express Card 0 Request	I-3.3	no PU/PD allowed!	-
A50	LPC_SERIRQ	LPC Serial Interrupt Request	IO-3.3	PU 10k 3.3V_S0	-
A51	GND_6	Power Ground	PWR	-	-
A52	RSVD	Not Connected	nc	-	-
A53	RSVD	Not Connected	nc	-	-
A54	SDIO_D0 / GPI0	SDIO#0 Data0 / General Purpose Input 0	I/O-3.3	PU 10k/100k to V3.3_S0	-
A55	RSVD	Not Connected	nc	-	-
A56	RSVD	Not Connected	nc	-	-
A57	GND_7	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCIe lane #3 Transmit+ (Optional)	DP-O	PD ~50R(PU @ reset) in TNC	only available on no-TopCliff var.
A59	PCIE_TX3-	PCIe lane #3 Transmit- (Optional)	DP-O	PD ~50R in TNC	only available on no-TopCliff var.
A60	GND_8	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCIe lane #2 Transmit+	DP-O	PD ~50R(PU @ reset) in TNC	-
A62	PCIE_TX2-	PCIe lane #2 Transmit-	DP-O	PD ~50R in TNC	-
A63	SDIO_D1 / GPI1	SDIO#0 Data1 / General Purpose Input 1	I/O-3.3	PU 10k/100k to V3.3_S0	-
A64	PCIE_TX1+	PCIe lane #1 Transmit+	DP-O	PD ~50R(PU @ reset) in TNC	-

A65	PCIE_TX1-	PCIe lane #1 Transmit-	DP-O	PD ~50R in TNC	-
A66	GND_9	Power Ground	PWR	-	-
A67	SDIO_D2 / GPI2	SDIO#0 Data2 / General Purpose Input 2	I/O-3.3	PU 10k/100k to V3.3_S0	-
A68	PCIE_TX0+	PCIe lane #0 Transmit+	DP-O	PD ~50R(PU @ reset) in TNC	-
A69	PCIE_TX0-	PCIe lane #0 Transmit-	DP-O	PD ~50R in TNC	-
A70	GND_10	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS Channel A DAT0+	DP-O	-	-
A72	LVDS_A0-	LVDS Channel A DAT0-	DP-O	-	-
A73	LVDS_A1+	LVDS Channel A DAT1+	DP-O	-	-
A74	LVDS_A1-	LVDS Channel A DAT1-	DP-O	-	-
A75	LVDS_A2+	LVDS Channel A DAT2+	DP-O	-	-
A76	LVDS_A2-	LVDS Channel A DAT2-	DP-O	-	-
A77	LVDS_VDD_EN	LVDS Panel Power Control	O-3.3	buffered; forced LOW in S5/S3	-
A78	LVDS_A3+	LVDS Channel A DAT3+	DP-O	-	-
A79	LVDS_A3-	LVDS Channel A DAT3+	DP-O	-	-
A80	GND_11	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS Channel A Clock+	DP-O	-	20-80MHz
A82	LVDS_A_CK-	LVDS Channel A Clock-	DP-O	-	20-80MHz
A83	LVDS_I2C_CK	LVDS I2C Clock (DDC)	IO-3.3	PU 10k 3.3V_S0	-
A84	LVDS_I2C_DAT	LVDS I2C Data (DDC)	IO-3.3	PU 10k 3.3V_S0	-
A85	SDIO_D3 / GPI3	SDIO# Data3 / General Purpose Input 3	I/O-3.3	PU 10k/100k to V3.3_S0	-
A86	RSVD	Not Connected	nc	-	-
A87	RSVD	Not Connected	nc	-	-
A88	PCIE0_CK_REF+	PCIe Clock (positive)	DP-O	-	100MHz
A89	PCIE0_CK_REF-	PCIe Clock (negative)	DP-O	-	100MHz
A90	GND_12	Power Ground	PWR	-	-
A91	SPI_POWER	Power supply for Carrier Board SPI	PWR	-	100mA (max.)
A92	SPI_MISO	Data in to Module from Carrier SPI	I-3.3	-	-
A93	SDIO_Clk / GPO0	SDIO#0 Clock / General Purpose Output 0	O-3.3	- / PD 100k	-
A94	SPI_CLK	Clock from Module to Carrier SPI	O-3.3	-	20MHz
A95	SPI_MOSI	Data out from Module to Carrier SPI	O-3.3	-	-
A96	TPM_PP	(TPM) Physical Presence pin	I-3.3	PD 4.7k	-
A97	TYPE10#	Indicates TYPE10# to carrier board	O	PD 4.7k	-
A98	SER0_TX	UART transmitter	O-3.3	-	14.5V tolerance
A99	SER0_RX	UART receiver	I-3.3	PU 47k / 10k 3.3V_S0	14.5V tolerance
A100	GND_14	Power Ground	PWR	-	-
A101	SER1_TX	UART transmitter / optional CAN-TX	O-3.3	-	14.5V / 3.3V tolerance
A102	SER1_RX	UART receiver / optional CAN-RX	I-3.3	PU 47k / 10k 3.3V_S0	14.5V / 3.3V tolerance
A103	LID#	LID button	nc	-	not supported
A104	VCC_12V_7	12V VCC	PWR	-	-
A105	VCC_12V_8	12V VCC	PWR	-	-
A106	VCC_12V_9	12V VCC	PWR	-	-
A107	VCC_12V_10	12V VCC	PWR	-	-
A108	VCC_12V_11	12V VCC	PWR	-	-
A109	VCC_12V_12	12V VCC	PWR	-	-
A110	GND_15	Power Ground	PWR	-	-

6.3 Connector X1A Row B

Pin	Signal	Description	Type	Termination	Comment
B1	GND_16	Power Ground	PWR	-	-
B2	GBE0_ACT#	Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC Frame Indicator	O-3.3	-	-
B4	LPC_AD0	LPC Address / Data Bus	IO-3.3	PU 100k	-
B5	LPC_AD1	LPC Address / Data Bus	IO-3.3	PU 100k	-
B6	LPC_AD2	LPC Address / Data Bus	IO-3.3	PU 100k	-
B7	LPC_AD3	LPC Address / Data Bus	IO-3.3	PU 100k	-
B8	LPC_DRQ0#	Not Connected	nc	-	-
B9	LPC_DRQ1#	Not Connected	nc	-	-
B10	LPC_CLK	LPC Clock	O-3.3	-	up to 33MHz
B11	GND_17	Power Ground	PWR	-	-
B12	PWRBTN#	Power Button Input	I-3.3	PU 10k 3.3V_S5	active on falling edge
B13	SMB_CLK	SMBus Clock	O-3.3	PU 10k in S5 / 5k in S0 3.3V	-
B14	SMB_DAT	SMBus Data	IO-3.3	PU 10k in S5 / 5k in S0 3.3V	-
B15	SMB_ALERT#	SMBus Interrupt	IO-3.3	PU 10k 3.3V_S0	-
B16	SATA1_TX+	SATA 0 Transmit Data+	DP-O	-	-
B17	SATA1_TX-	SATA 0 Transmit Data-	DP-O	-	-
B18	SUS_STAT#	Indicates imminent suspend operation	O-3.3	-	CPLD I/O
B19	SATA1_RX+	SATA 0 Receive Data+	DP-I	-	-
B20	SATA1_RX-	SATA 0 Receive Data-	DP-I	-	-
B21	GND_18	Power Ground	PWR	-	-
B22	RSVD	Not Connected	nc	-	-
B23	RSVD	Not Connected	nc	-	-
B24	PWR_OK	Power OK from power supply	I-5T	PU 511k 3.3V_S5	CPLD I/O
B25	RSVD	Not Connected	nc	-	-
B26	RSVD	Not Connected	nc	-	-
B27	WDT	Indicator for Watchdog Timeout	O-3.3	-	CPLD I/O
B28	HDA_SDIN2	Not Connected	nc	-	not supported
B29	HDA_SDIN1	Audio Codec Serial Data in 1	I-3.3	PD ~10k in TNC	-
B30	HDA_SDIN0	Audio Codec Serial Data in 0	I-3.3	PD ~10k in TNC	-
B31	GND_19	Power Ground	PWR	-	-
B32	SPKR	Speaker Interface	O-3.3	-	-
B33	I2C_CK	General Purpose I2C Clock	IO-3.3	PU 2k2 3.3V_S5	CPLD I/O
B34	I2C_DAT	General Purpose I2C Data	IO-3.3	PU 2k2 3.3V_S5	CPLD I/O
B35	THRM#	Over Temperature Indicator	I-3.3	PU 10k 3.3V_S0	-
B36	USB7-	USB Data- Client (Client Mode)	DP-I/O	PD 12k in Topcliff	-
B37	USB7+	USB Data+ Client (Client Mode)	DP-I/O	PD 12k in Topcliff	-
B38	USB_4_5_OC#	USB Over current Pair 4 / 5 / 6	I-3.3	PU 10k 3.3V_S5	-
B39	USB5-	USB Data- Port #5 (n.a. if USB6 option is used)	DP-I/O	PD 12k in Topcliff	-
B40	USB5+	USB Data+ Port #5 (n.a. if USB6 option is used)	DP-I/O	PD 12k in Topcliff	-
B41	GND_20	Power Ground	PWR	-	-
B42	USB3-	USB Data- Port #3	DP-I/O	PD 12k in Topcliff	-
B43	USB3+	USB Data+ Port #3	DP-I/O	PD 12k in Topcliff	-
B44	USB_0_1_OC#	USB Over current Pair 0 / 1	I-3.3	PU 10k 3.3V_S5	-
B45	USB1-	USB Data- Port #0	DP-I/O	PD 12k in Topcliff	-
B46	USB1+	USB Data+ Port #0	DP-I/O	PD 12k in Topcliff	-
B47	EXCD1_PERST#	PCIe Express Card 1 Reset	O-3.3	-	no PU or PD allowed!
B48	EXCD1_CPPE#	PCIe Express Card 1 Request	I-3.3	-	-
B49	SYS_RESET#	Reset button input	I-3.3	PU 5k-25k 3.3_S5 in CPLD	-
B50	CB_RESET#	Carrier Board Reset	O-3.3	-	CPLD I/O
B51	GND_21	Power Ground	PWR	-	-
B52	RSVD	Not Connected	nc	-	-
B53	RSVD	Not Connected	nc	-	-
B54	SDIO_CMD / GPO1	SDIO#0 Command / General Purpose Output 1	I/O-3.3	PU 75k V3.3V_S0 / PD 100k	-
B55	RSVD	Not Connected	nc	-	-
B56	RSVD	Not Connected	nc	-	-
B57	SDIO_WP / GPO2	SDIO#0 Write Protection /General Purpose Output 2	I-3.3	PU 10k V3.3V_S0 / PD 100k	-
B58	PCIE_RX3+	PCIe lane #3 Receive+ (Optional)	DP-I	PD ~50R(PU @ reset) in TNC	only available on no-TopCliff var.
B59	PCIE_RX3-	PCIe lane #3 Receive- (Optional)	DP-I	PD ~50R(PU @ reset) in TNC	only available on no-TopCliff var.
B60	GND_22	Power Ground	PWR	-	-
B61	PCIE_RX2+	PCIe lane #2 Receive+	DP-I	PD ~50R(PU @ reset) in TNC	-
B62	PCIE_RX2-	PCIe lane #2 Receive-	DP-I	PD ~50R(PU @ reset) in TNC	-
B63	SDIO_CD# / GPO3	SDIO#0 CardDetect / General Purpose Output 3	I-3.3	PU 10k V3.3V_S0 / PD 100k	-
B64	PCIE_RX1+	PCIe lane #1 Receive+	DP-I	PD ~50R(PU @ reset) in TNC	-

B65	PCIE_RX1-	PCIe lane #1 Receive-	DP-I	PD ~50R(PU @ reset) in TNC	-
B66	WAKE0#	PCI Express Wake Event	I-3.3	PU 1k 3.3V_S5	-
B67	WAKE1#	General Purpose Wake Event	I-3.3	PU 1k 3.3V_S5	-
B68	PCIE_RX0+	PCIe lane #0 Receive+	DP-I	PD ~50R(PU @ reset) in TNC	-
B69	PCIE_RX0-	PCIe lane #0 Receive-	DP-I	PD ~50R(PU @ reset) in TNC	-
B70	GND_23	Power Ground	PWR	-	-
B71	DDI0_PAIR0+	SDVOB_RED_P	DP-O	-	SDVO
B72	DDI0_PAIR0-	SDVOB_RED_N	DP-O	-	SDVO
B73	DDI0_PAIR1+	SDVOB_GREEN_P	DP-O	-	SDVO
B74	DDI0_PAIR1-	SDVOB_GREEN_N	DP-O	-	SDVO
B75	DDI0_PAIR2+	SDVOB_BLUE_P	DP-O	-	SDVO
B76	DDI0_PAIR2-	SDVOB_BLUE_N	DP-O	-	SDVO
B77	DDI0_PAIR4+	SDVOB_INT_P	DP-I	-	SDVO
B78	DDI0_PAIR4-	SDVOB_INT_N	DP-I	-	SDVO
B79	LVDS_BKLT_EN	Backlight Enable	O-3.3	buffered; forced LOW in S5/S3	-
B80	GND_24	Power Ground	PWR	-	-
B81	DDI0_PAIR3+	SDVOB_CLKIN_P	DP-O	100-200MHz	SDVO
B82	DDI0_PAIR3-	SDVOB_CLKIN_N	DP-O	100-200MHz	SDVO
B83	LVDS_BKLT_CTRL	Backlight Brightness Control	O-3.3	-	-
B84	VCC_5V_SBY	+5V Standby	PWR	-	-
B85	VCC_5V_SBY	+5V Standby	PWR	-	-
B86	VCC_5V_SBY	+5V Standby	PWR	-	-
B87	VCC_5V_SBY	+5V Standby	PWR	-	-
B88	BIOS_DIS1#	Disable Module BIOS.Enable boot from SPI on Baseboard	I-3.3	PU ~15k in CPLD 3.3V_S5	For ext.SPI
B89	DDI0_HPD	Not Connected	nc	-	not supported
B90	GND_25	Power Ground	PWR	-	-
B91	DDI0_PAIR5+	SDVOB_TVCLKIN_P	DP-I	100-200MHz	SDVO
B92	DDI0_PAIR5-	SDVOB_TVCLKIN_N	DP-I	100-200MHz	SDVO
B93	DDI0_PAIR6+	SDVO_STALLP	DP-I	-	SDVO
B94	DDI0_PAIR6-	SDVO_STALLN	DP-I	-	SDVO
B95	DDI0_DDC_AUX_SEL	nc / SDVOB_CTRLCLK (Optional)	nc	optional use by COMe Type1	-
B96	RSVD	nc / SDVOB_CTRLDATA(Optional)	nc	optional use by COMe Type1	-
B97	SPI_CS#	SPI Chipselect	O	3.3V_S5	-
B98	DDI0_AUX+	SDVOB_CTRLCLK	O	-	-
B99	DDI0_AUX-	SDVOB_CTRLDATA	I/O	-	-
B100	GND_26	Power Ground	PWR	-	-
B101	FAN_PWMOUT	Not connected	nc	-	not supported
B102	FAN_TACHIN	Not connected	nc	-	not supported
B103	SLEEP#	Not Connected	nc	-	-
B104	VCC_12V_16	12V VCC	PWR	-	-
B105	VCC_12V_17	12V VCC	PWR	-	-
B106	VCC_12V_18	12V VCC	PWR	-	-
B107	VCC_12V_19	12V VCC	PWR	-	-
B108	VCC_12V_20	12V VCC	PWR	-	-
B109	VCC_12V_21	12V VCC	PWR	-	-
B110	GND_27	Power Ground	PWR	-	-

The termination resistors in this table are already mounted on the module. Refer to the design guide for information about additional termination resistors.

7 BIOS Operation

The module is equipped with AMI® Aptio, which is located in an onboard SPI serial flash memory.

7.1 Determining the BIOS Version

The AMI® Aptio version is displayed in the main menu of the setup utility.

» BIOS Vendor: American Megatrends

» Core Version: x.x.x.x

» BIOS Date: mm/dd/yyyy hh:mm:ss

» BIOS Version: NTC1RXXX

7.2 BIOS Update

Kontron provides continuous BIOS updates for Computer-on-Modules. The updates are provided for download on http://emdcustomersection.kontron.com with a detailed change description within the according Product Change Notification (PCN). Please register for EMD Customer Section to get access to BIOS downloads and PCN service.

Modules with BIOS Region/Setup only inside the flash can be updated with AFU utilities (usually 1-3MB BIOS binary file size) directly. Modules with Intel® Management Engine, Ethernet, Flash Descriptor and other options additionally to the BIOS Region (usually 4-8MB BIOS binary file size) requires a different update process with Intel Flash Utility FPT and a wrapper to backup and restore configurations and the MAC address. Therefore it is strongly recommended to use the batch file inside the BIOS download package available on EMD Customer Section.

» Boot the module to DOS/EFI Shell with access to the BIOS image and Firmware Update Utility provided on EMD Customer Section

» Execute Flash.bat in DOS or Flash.nsh in EFI Shell

Any modification of the update process may damage your module!

Backup the BIOS / Create a BIOS with custom defaults:

» Change your BIOS settings according your needs

» Save and Exit Setup with option “Save as User Defaults”. Your customized settings are now stored inside the flash in a second area additional to the manufacturer defaults

» Boot the module to DOS or EFI Shell with access to the update utilities

» Extract the BIOS region including your custom defaults with **afuefix64.efi CBIOS.bin /O** in EFI Shell or **afudos.exe CBIOS.rom /O** in DOS

Now you can clone the BIOS with your customized default settings to other modules or external SPI flashes with above mention AFU utilites. On modules with Management Engine and Ethernet inside the Flash the same BIOS core version should already be programmed on the target.

AMI APTIO update utilities for DOS, EFI Shell and Windows are available for free at AMI.com:
http://www.ami.com/support/downloads/amiflash.zip

7.3 Setup Guide

The Aptio Setup Utility changes system behavior by modifying the Firmware configuration. The setup program uses a number of menus to make changes and turn features on or off.

Functional keystrokes in POST:

Key	Function
DEL	Enter Setup
F2	Enter Setup
F7	Boot Menu

7.4 POST Codes

Important POST codes during boot-up

AB	BIOS Setup
AD	EFI Shell
AE	Windows

7.4.1 Start AMI® Aptio Setup Utility

To start the AMI® BIOS setup utility, press <DEL> or <F2> when the following string appears during bootup.

Press <DEL> to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
+/-	Change Option
<Enter>	Execute command or select submenu.
<F1>	General Help window.
<F2>	Previous Values
<F3>	Load the optimized default configuration.
<F4>	Save and exit.
<Esc>	Exit menu.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (►) marks all submenus.

Item Specific Help Window

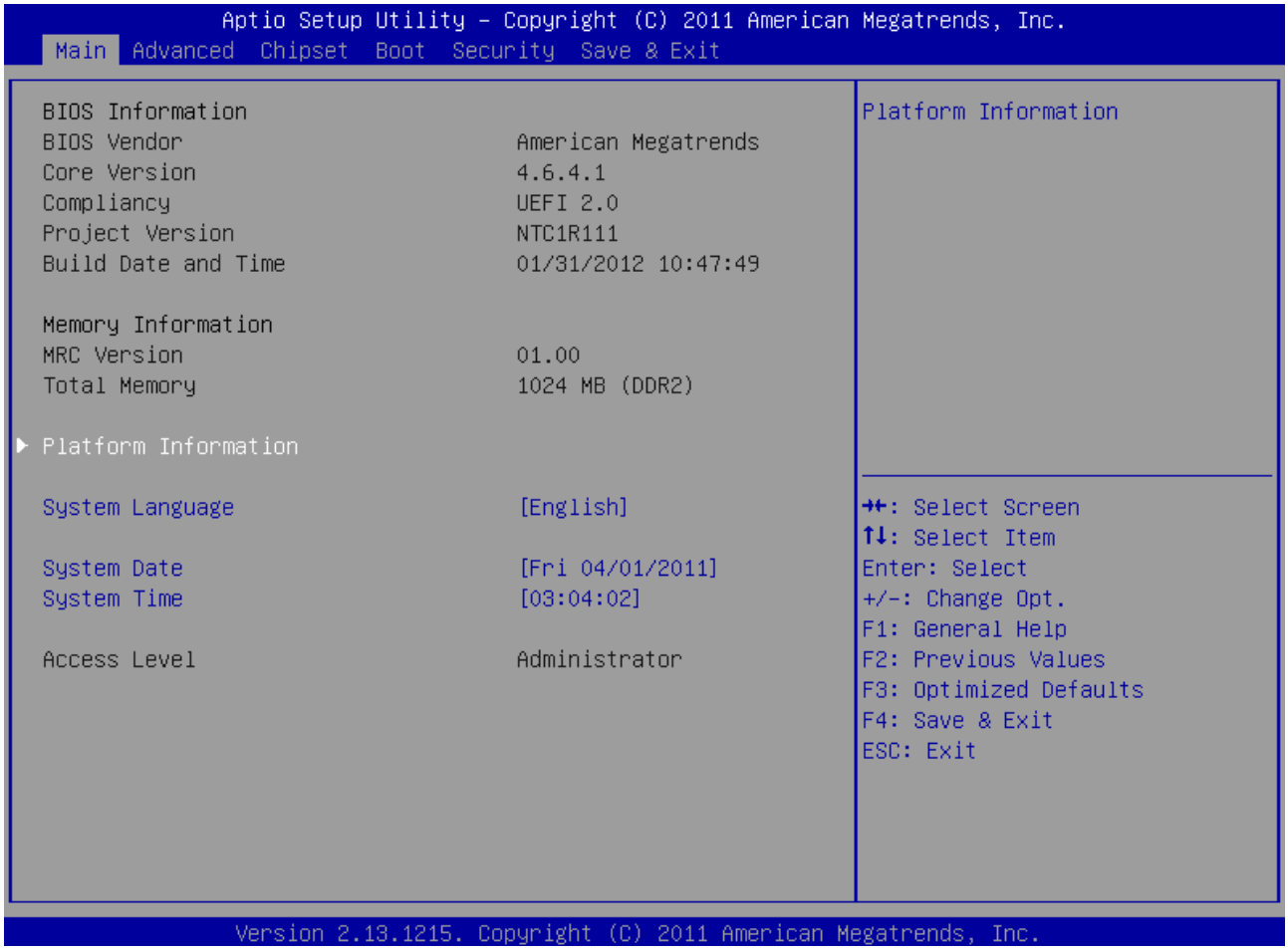
The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

7.5 BIOS Setup

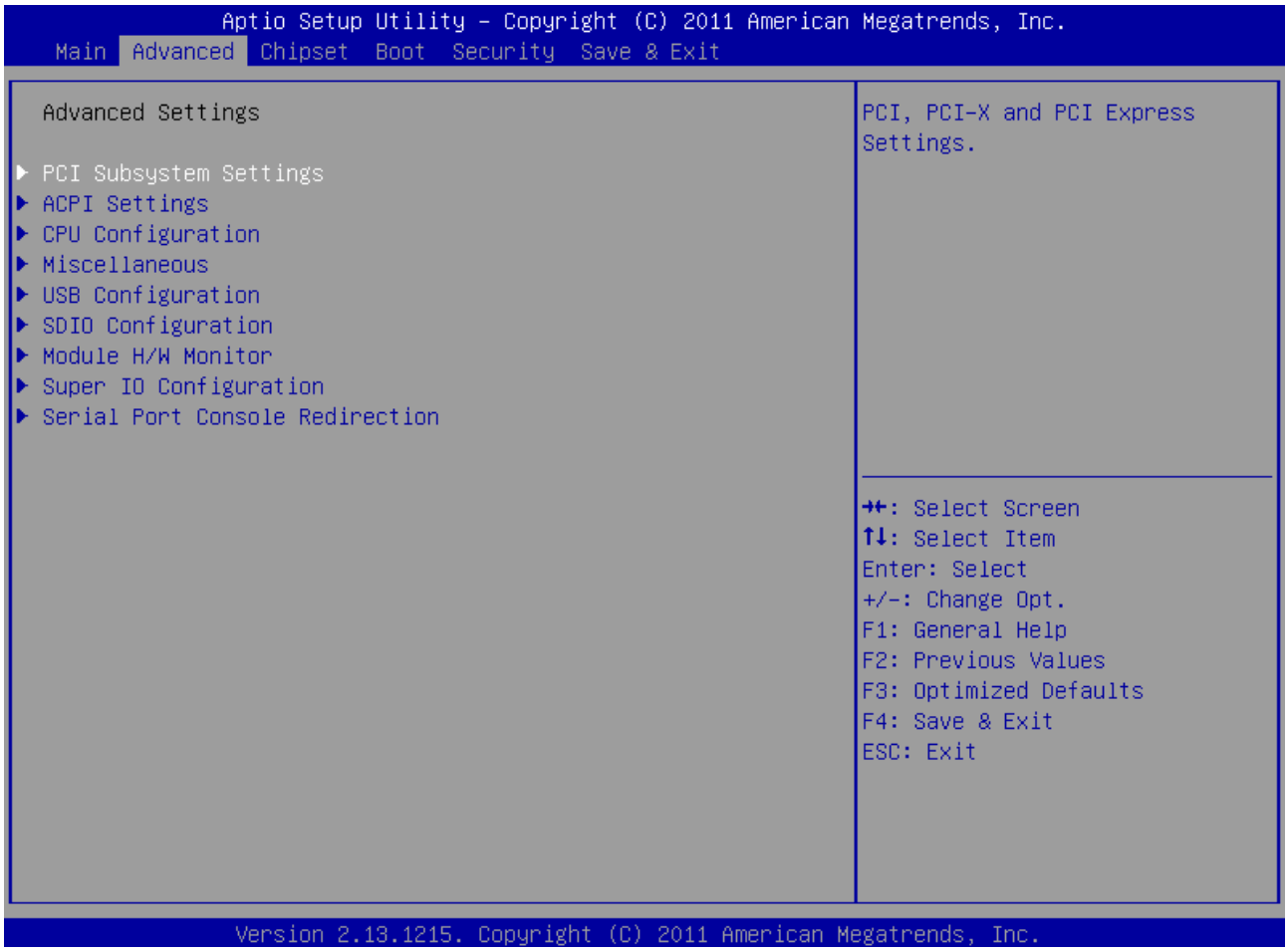
7.5.1 Main



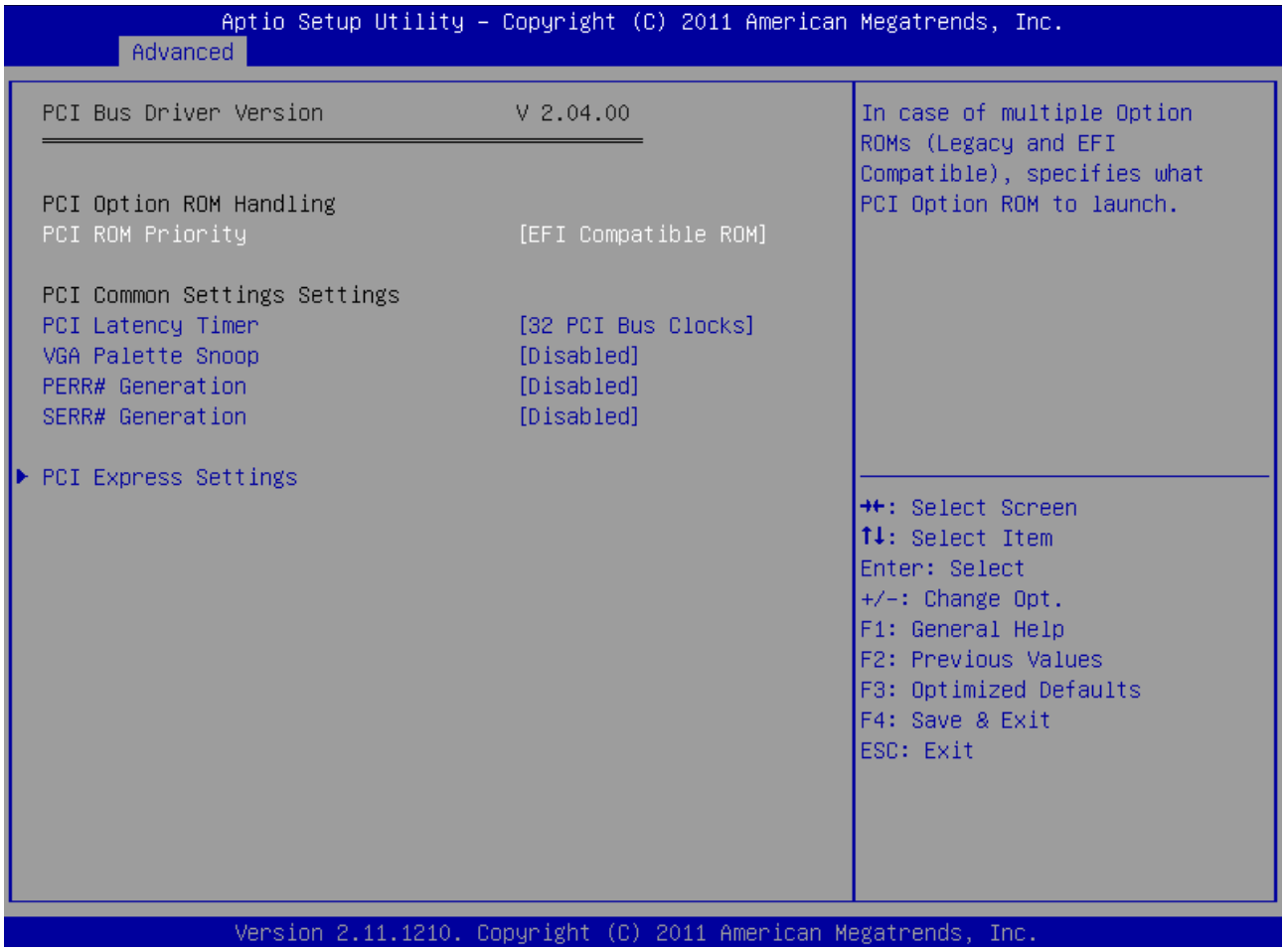
Feature	Options	Description
System Language	**English**	Choose the system default language
System Date	[mm/dd/yyyy]	Set the Date. Use 'Tab' to switch between Date elements
System Time	[hh:mm:ss]	Set the Time. Use 'Tab' to switch between Time elements

Platform Information

7.5.2 Advanced

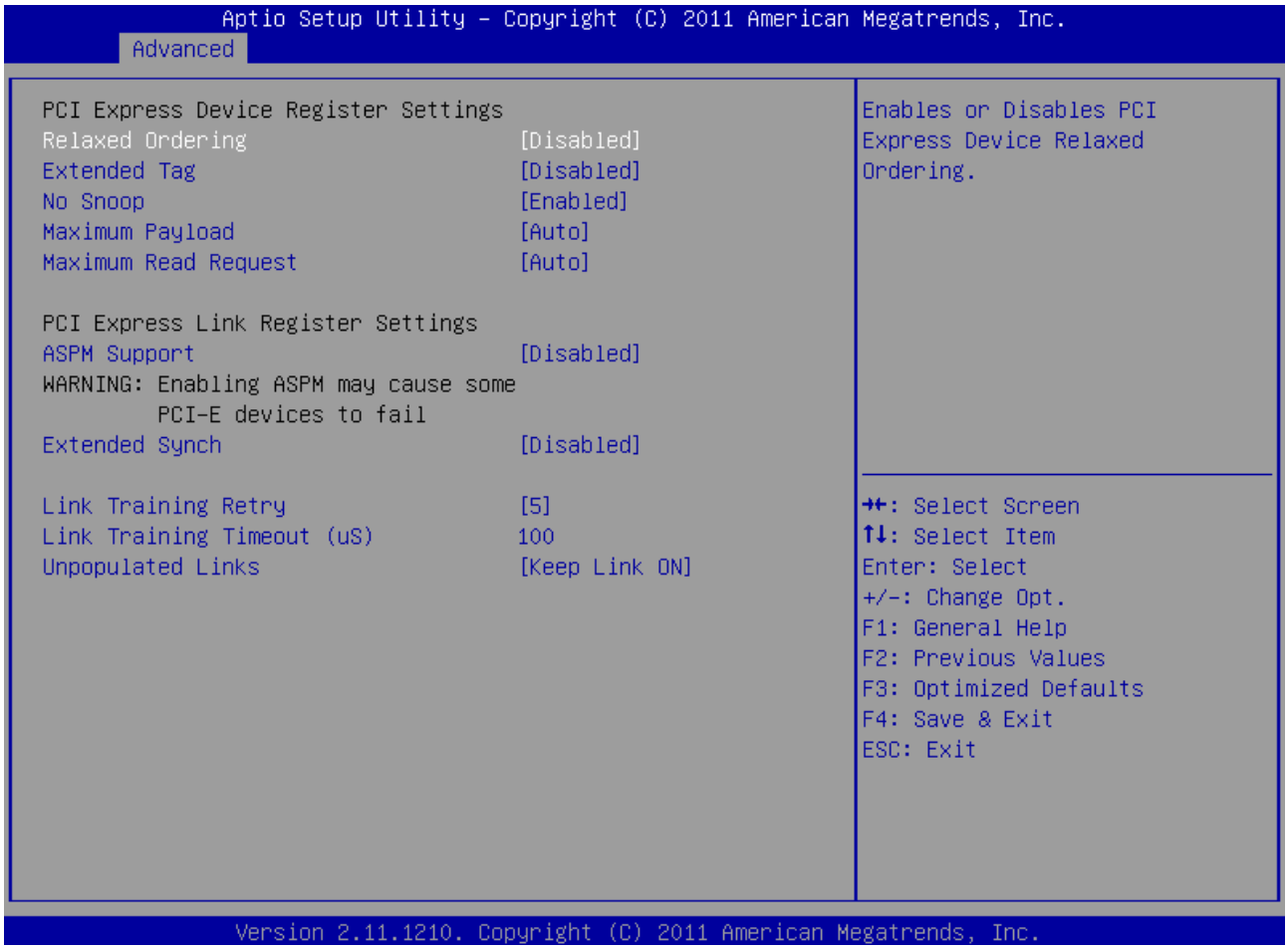


PCI Subsystem Settings



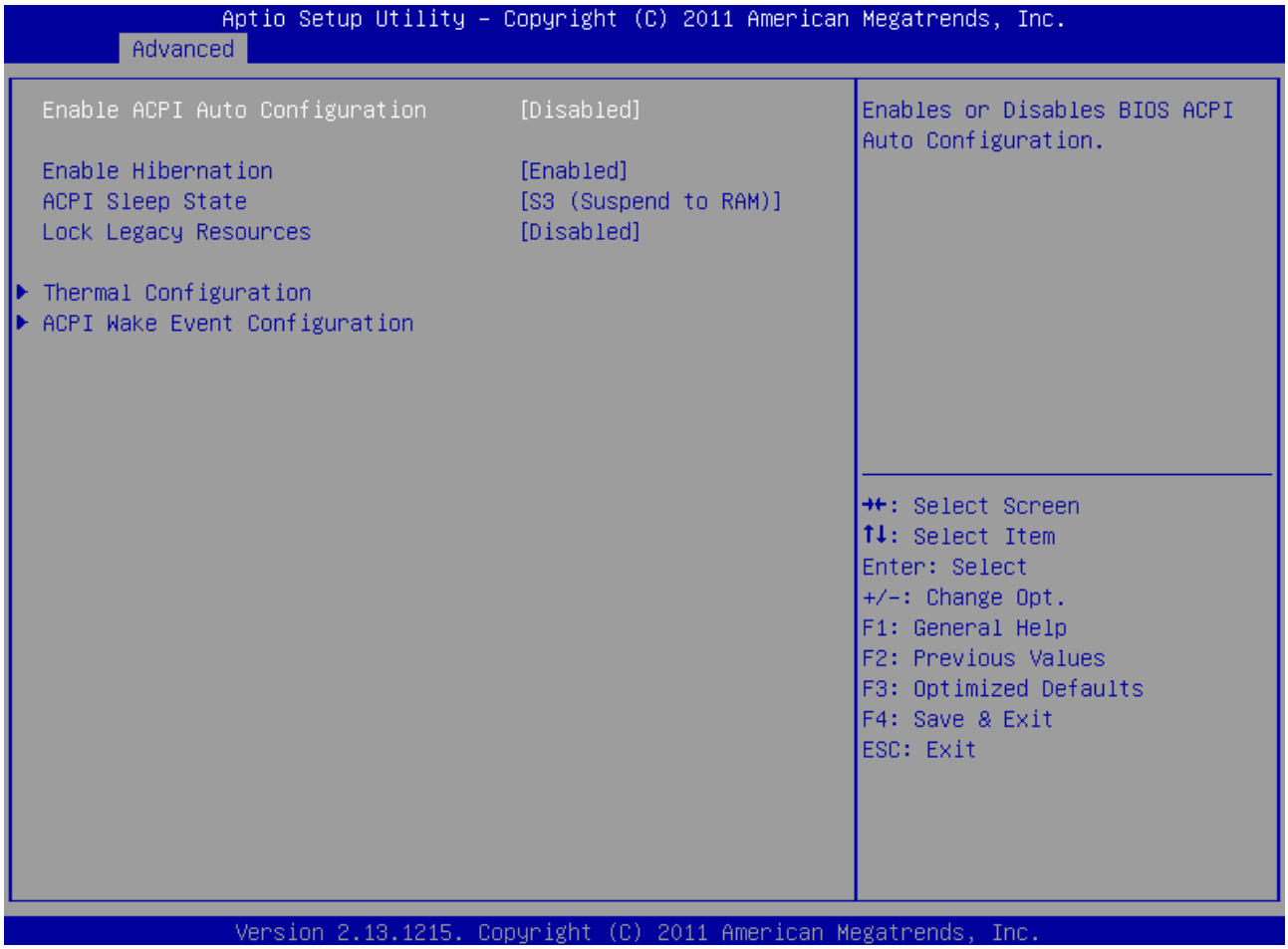
Feature	Options	Description
PCI ROM Priority	Legacy ROM **EFI Compatible ROM**	In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch
PCI Latency Timer	**32** ... 248 PCI Bus Clocks	Value to be programmed into PCI Latency Timer Register
VGA Palette Snoop	**Disabled** Enabled	Enables or Disables VGA Palette Registers Snooping
PERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate PERR#
SERR# Generation	**Disabled** Enabled	Enables or Disables PCI Device to Generate SERR#

PCI Express Settings



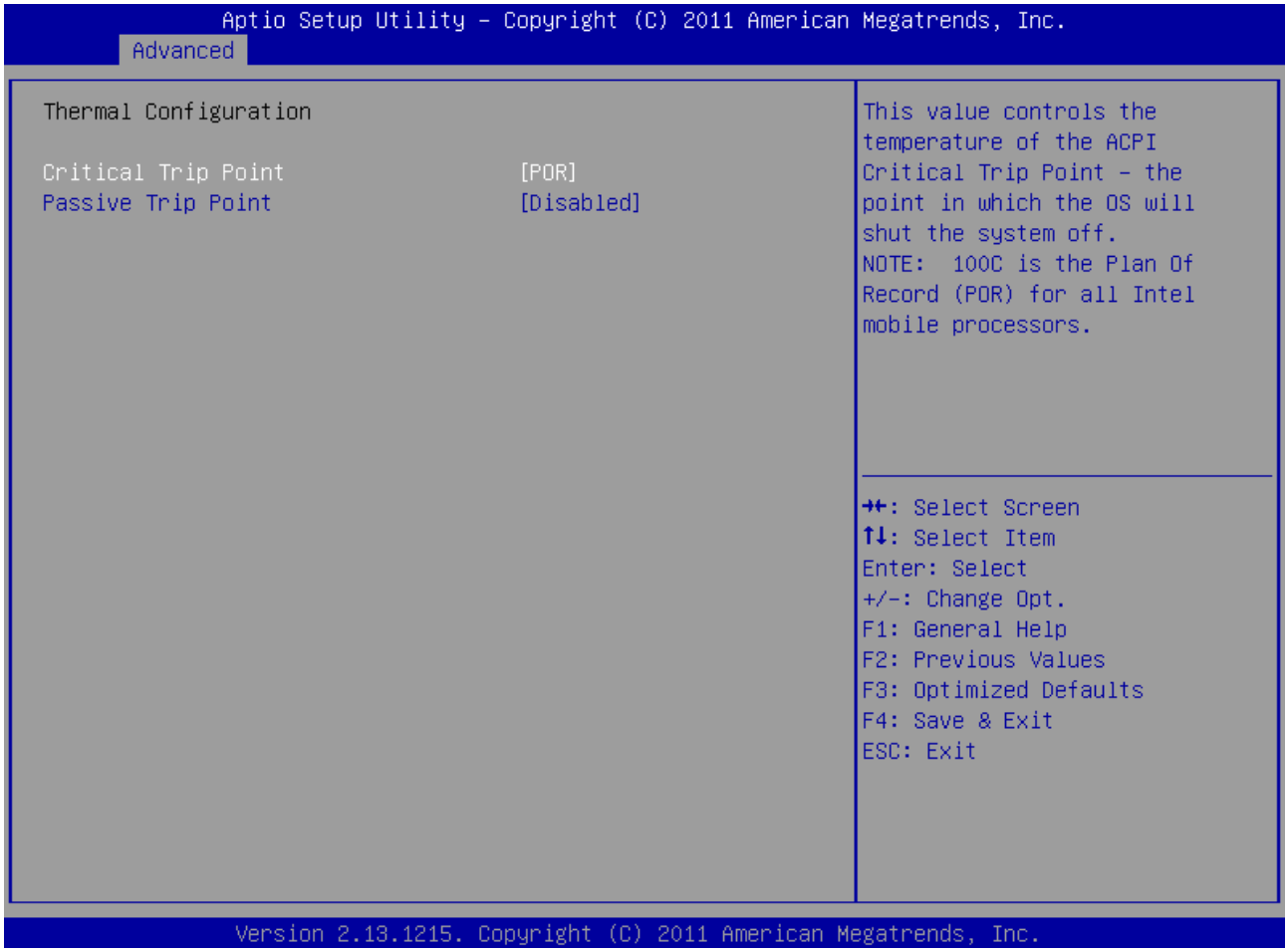
Feature	Options	Description
Relaxed Ordering	**Disabled** Enabled	Enables or Disables PCI Express Device Relaxed Ordering
Extended Tag	**Disabled** Enabled	If Enabled allows device to use 8-bit Tag field as a requester
No Snoop	Disabled **Enabled**	Enables or Disables PCI Express Device No Snoop option
Maximum Payload	**Auto** 128 ... 4096 Bytes	Set Maximum Payload of PCI Express Device or allow System BIOS to select the value
Maximum Read Request	**Auto** 128 ... 4096 Bytes	Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value
ASPM Support	**Disabled** Auto Force L0s	Set the ASPM Level: Force L0s - Force all links to L0s State. Auto - BIOS auto configure. Disable - Disables ASPM
Extended Sync	**Disabled** Enabled	If Enabled allows generation of Extended Synchronization patterns
Link Training Retry	Disabled 2 3 **5**	Defines number of Retry Attepmts software will take to retrain the link if previous training attempt was unsuccessful
Link Training Timeout (uS)	**100**	Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 1 to 100uS
Unpopulated Links	**Keep Link ON** Disable Link	In order to save power, sofware will disable unpopulated PCI Express links, if this option set to 'Disable Link'

ACPI Settings



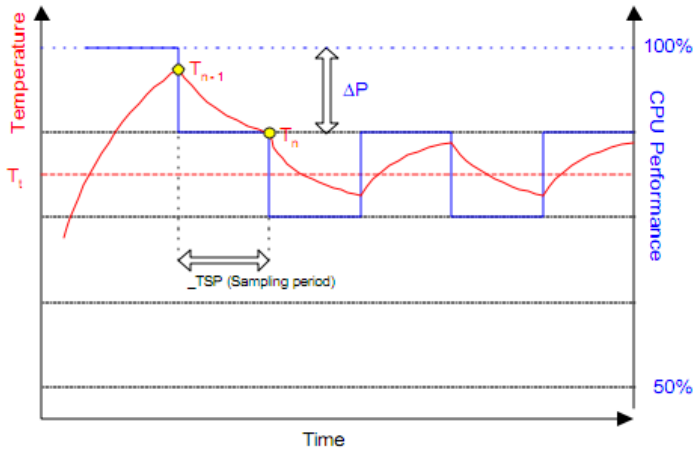
Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enables or Disables BIOS ACPI Auto Configuration
Enable Hibernation	**Disabled** Enabled	Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Suspend Disabled **S3 (StR)**	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed
Lock Legacy Resources	**Disabled** Enabled	Enables or Disables Lock of Legacy Resources

Thermal Configuration



Feature	Options	Description
Critical Trip Point	**POR** 30°C ... 95°C	This value controls the temperature of the ACPI Critical Trip Point - the point in which the OS will shut the system off. Note: 100°C is the Plan Of Record (POR) for all Intel mobile processors
Passive Trip Point	**Disabled** 30°C ... 100°C	This value controls the temperature of the ACPI Passive Trip Point - the point in which the OS will begin throttling the processor
- Passive TC1 Value	**1**	This value sets the TC1 value for the ACPI Passive Cooling Formula. Range 1 - 16
- Passive TC2 Value	**5**	This value sets the TC2 value for the ACPI Passive Cooling Formula. Range 1 - 16
- Passive TSP Value	**10**	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenth of a second how often the OS will read the temperature when passive cooling is enabled. Range 2 - 32

Passive Cooling



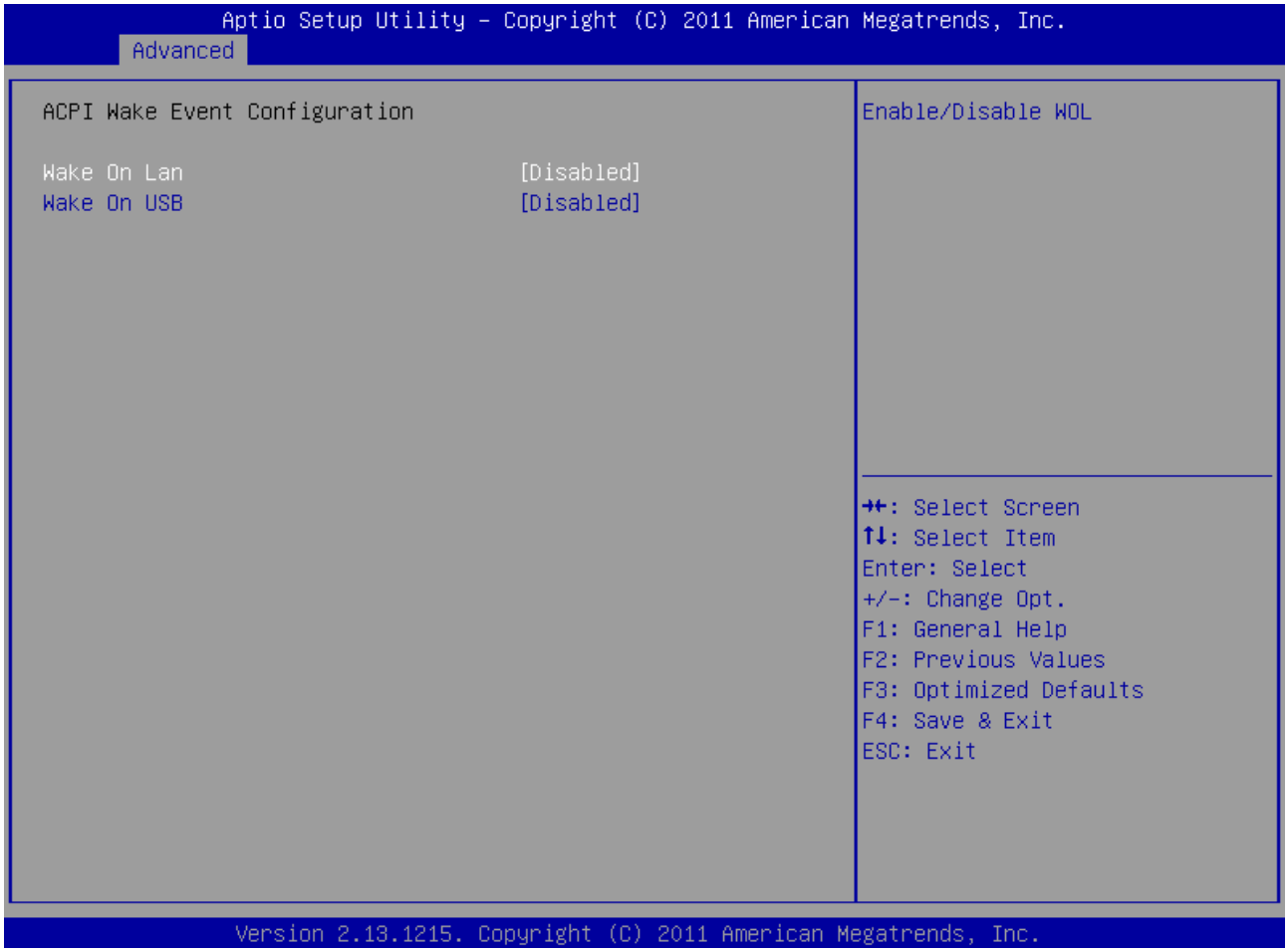
The ACPI OS assesses the optimum CPU performance change necessary to lower the temperature using the following equation

$$\Delta P[\%] = TC1(Tn-Tn-1) + TC2(Tn-Tt)$$

ΔP is the performance delta, Tt is the target temperature = passive cooling trip point. The two coefficients TC1 and TC2 and the sampling period TSP are hardware dependent constants the end user must supply. It's up to the end user to set the cooling preference of the system by setting the appropriate trip points in the BIOS setup.

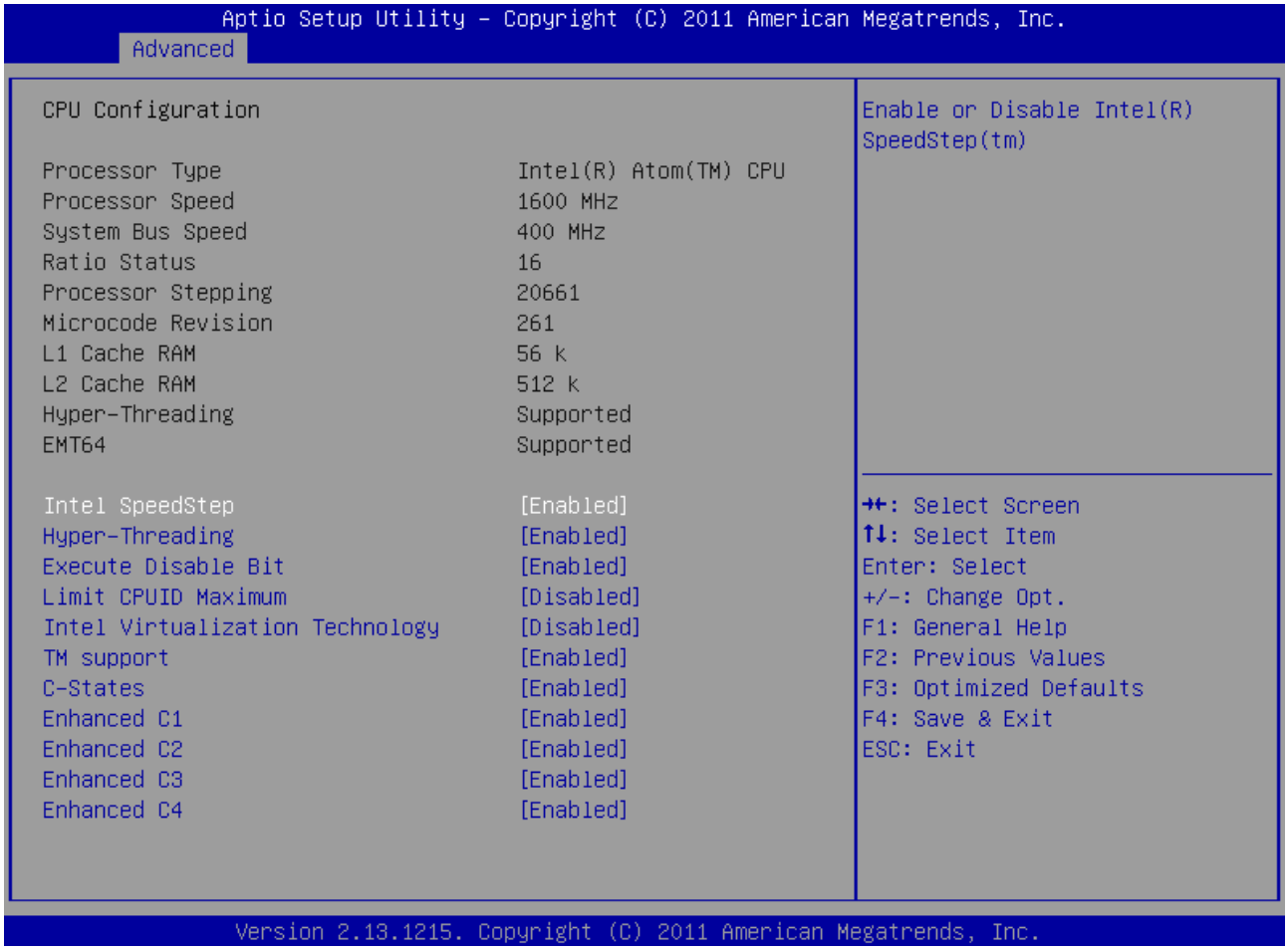
See chapter 12 of the ACPI specification (www.acpi.info) for more details

ACPI Wake Event Configuration



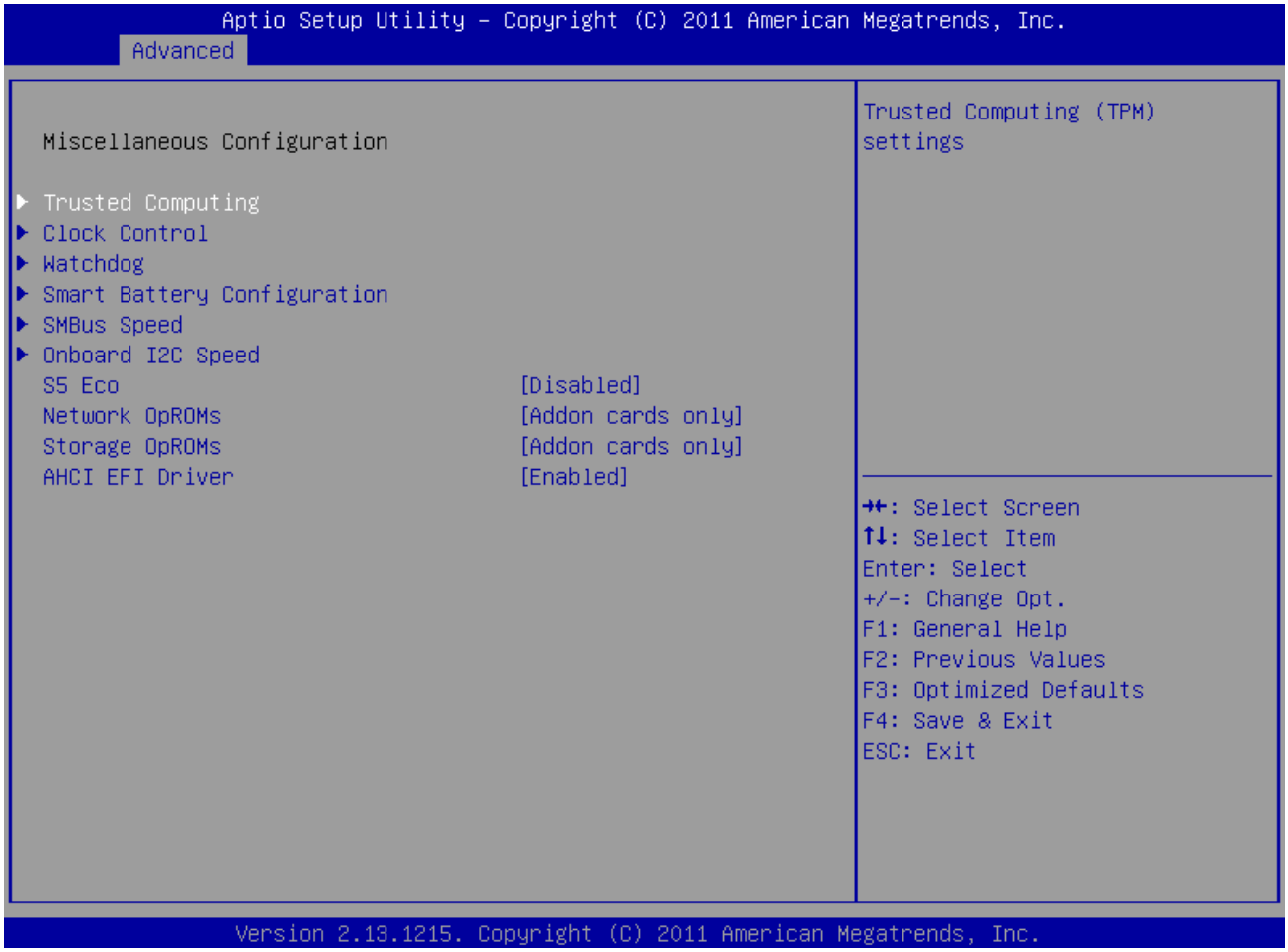
Feature	Options	Description
Wake On Lan	**Disable** Enable	Enable / Disable WOL
Wake On USB	**Disable** Enable	Enable / Disable Wake On USB. This works only on ports powered with standby voltage

CPU Configuration



Feature	Options	Description
Intel SpeedStep	Disabled **Enabled**	Enables/Disables the Intel Speedstep Technology (E)IST
Hyper-Threading	Disabled **Enabled**	Enables/Disables the Intel® Hyper Threading Technology HTT
Execute Disable Bit	Disabled **Enabled**	XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS
Limit CPUID Value Limit	**Disabled** Enabled	Disabled for Windows XP
Intel Virtualization Technology	**Disabled** Enabled	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology
TM support	Disabled **Enabled**	Enable CPU thermal management
C States	Disabled **Enabled**	Enable/Disable CPU Power Management. Allows CPU to to Idle States when it's not 100% utilized
Enhanced C1	Disabled **Enabled**	Enable or Disable Enhanced C1 State
Enhanced C2	Disabled **Enabled**	Enable or Disable Enhanced C2 State
Enhanced C3	Disabled **Enabled**	Enable or Disable Enhanced C3 State
Enhanced C4	Disabled **Enabled**	Enable or Disable Enhanced C4 State

Miscellaneous

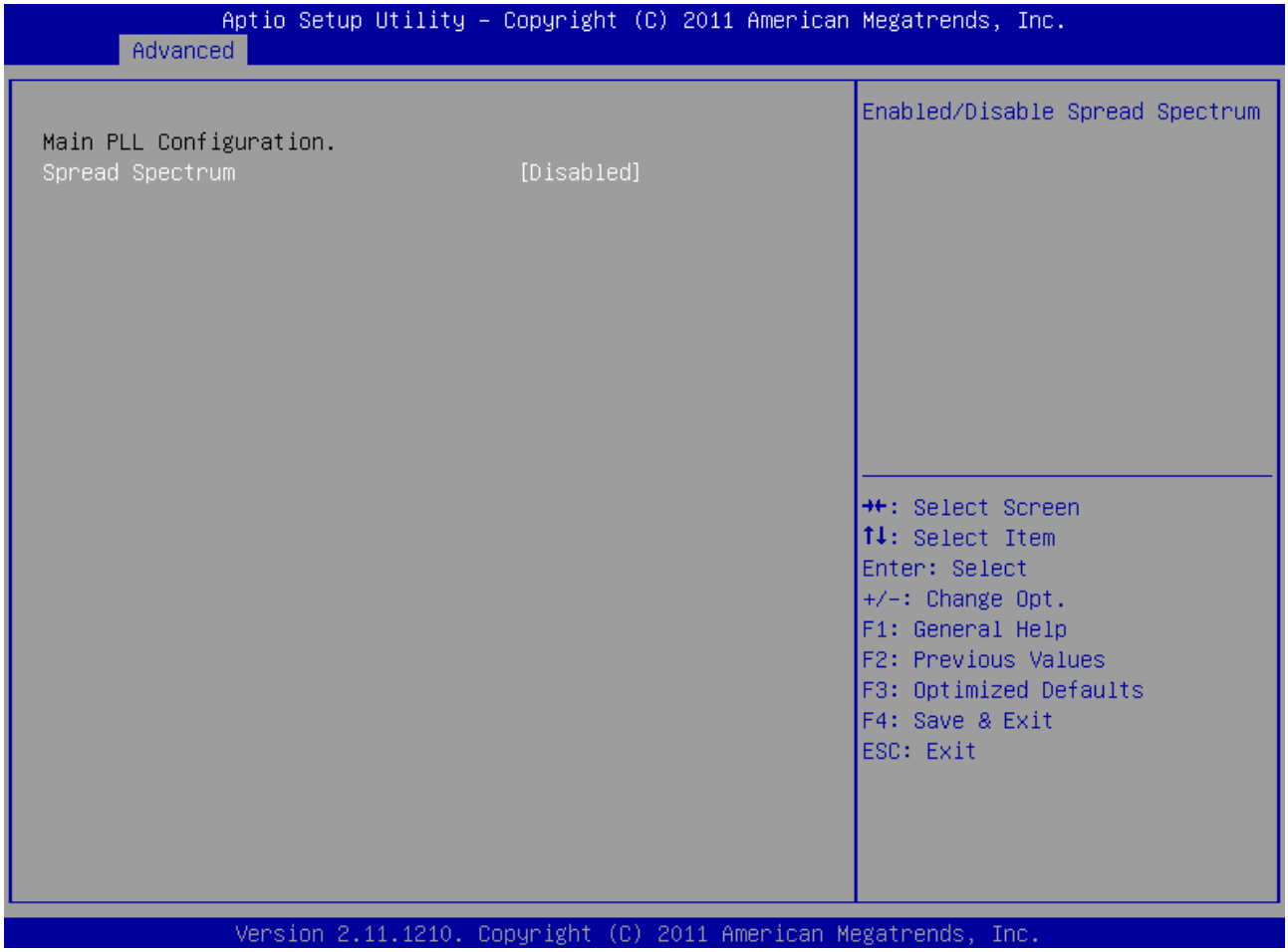


Feature	Options	Description
S5 Eco	**Disabled** Enabled	Reduce supply current in Soft Off State S5 to less than 1mA. If enabled, power button is the only wakeup source in S5. See chapter S5 Eco for more details
Network OpROMs	Disabled Onboard only **Addon cards only** Both	Enable or Disable Legacy Boot Option for Network Devices
Storage OpROMs	Disabled **Onboard only** Addon cards only Both	Enable or Disable Legacy Boot Option for Mass Storage Controllers
AHCI EFI Driver	Disabled **Enabled**	Enable or Disable onboard AHCI EFI driver

Trusted Computing

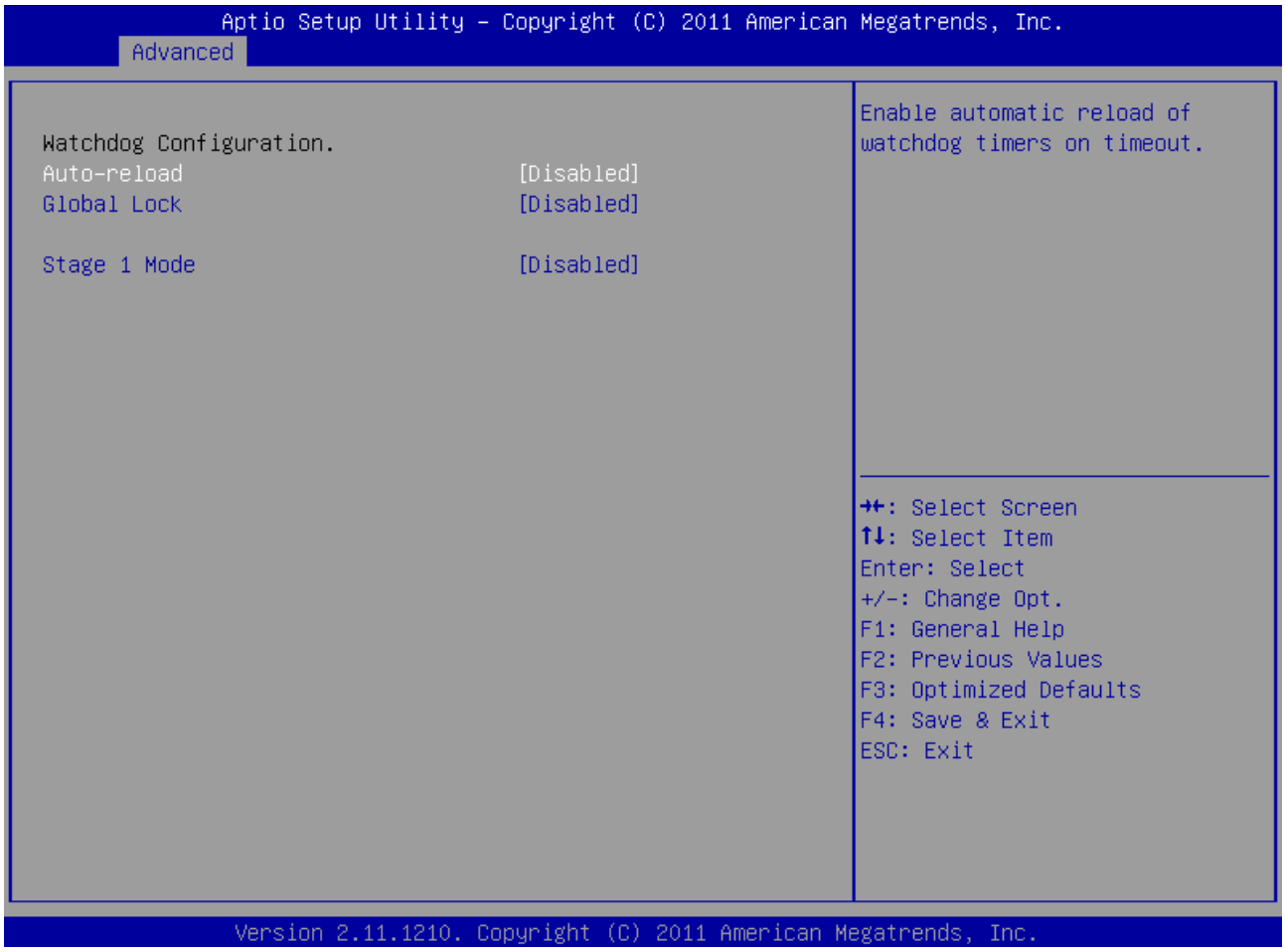
Feature	Options	Description
TPM Support	Disabled **Enabled**	Enables or Disables TPM support. O.S. will not show TPM. Reset of platform is required
TPM State	**Disabled** Enabled	Turn TPM On/Off. NOTE: Your Computer will reboot to change State of TPM

Clock Control



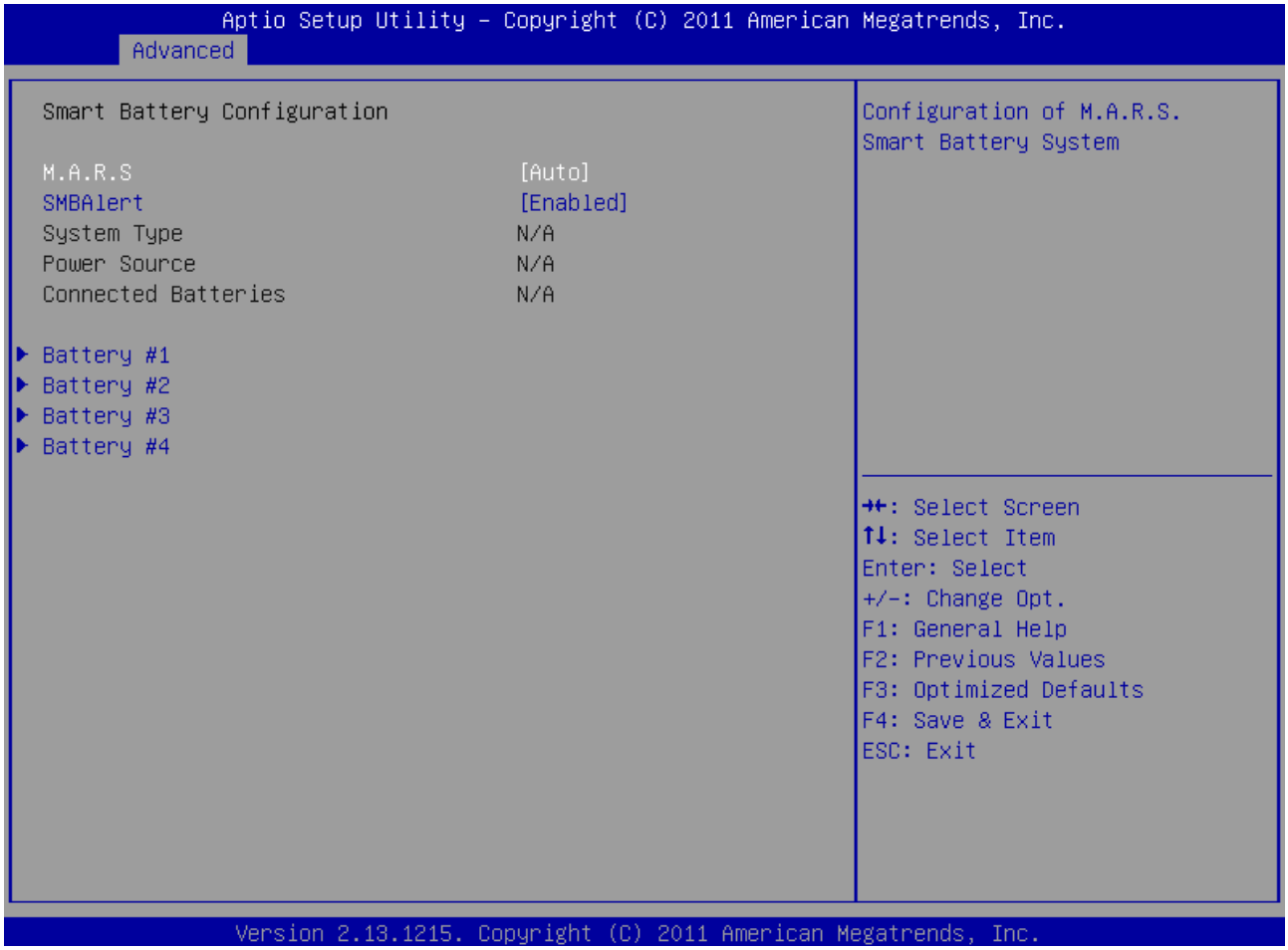
Feature	Options	Description
Spread Spectrum	**Disabled** Enabled	Enable/Disable Spread Spectrum

Watchdog



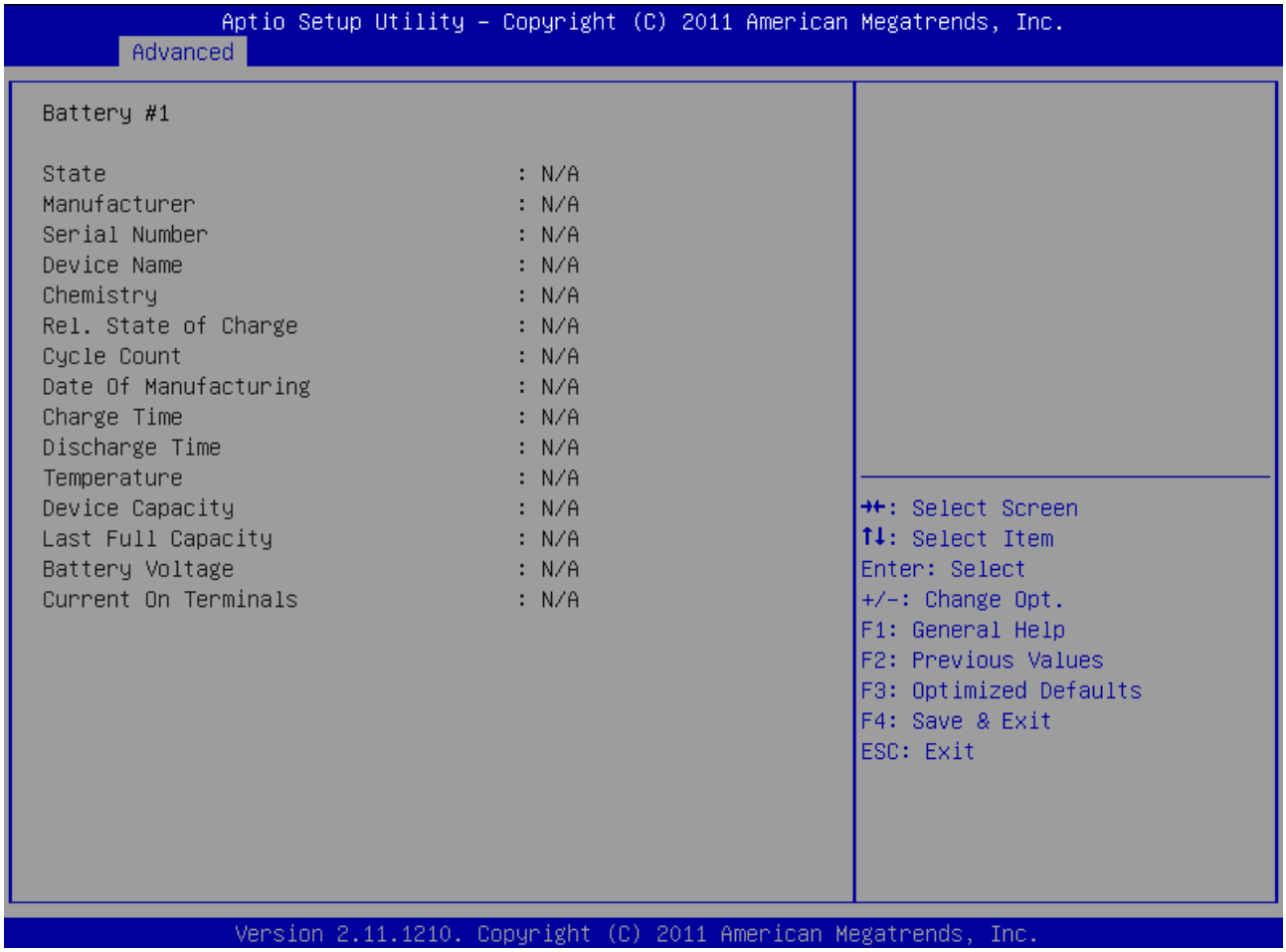
Feature	Options	Description
Auto-reload	**Disabled** Enabled	Enable automatic reload of watchdog timers on timeout
Global Lock	**Disabled** Enabled	If set to enabled, all Watchdog registers (except WD_KICK) become read only until the board is reset
Stage 1 Mode	**Disabled** Reset Delay	Select Action for first Watchdog stage
- Assert WDT Signal	**Disabled** Enabled	Enable/Disable assertion of WDT signal to baseboard on stage timeout
- Stage 1 Timout	1s 5s 10s **30s** 1m 3m 10m 30m	Select Timeout value for first watchdog stage
Stage 2 Mode	**Disabled** Reset	Select Action for second Watchdog stage
- Assert WDT Signal	**Disabled** Enabled	Enable/Disable assertion of WDT signal to baseboard on stage timeout
- Stage 2 Timout	1s 5s 10s **30s** 1m 3m 10m 30m	Select Timeout value for second watchdog stage

Smart Battery Configuration

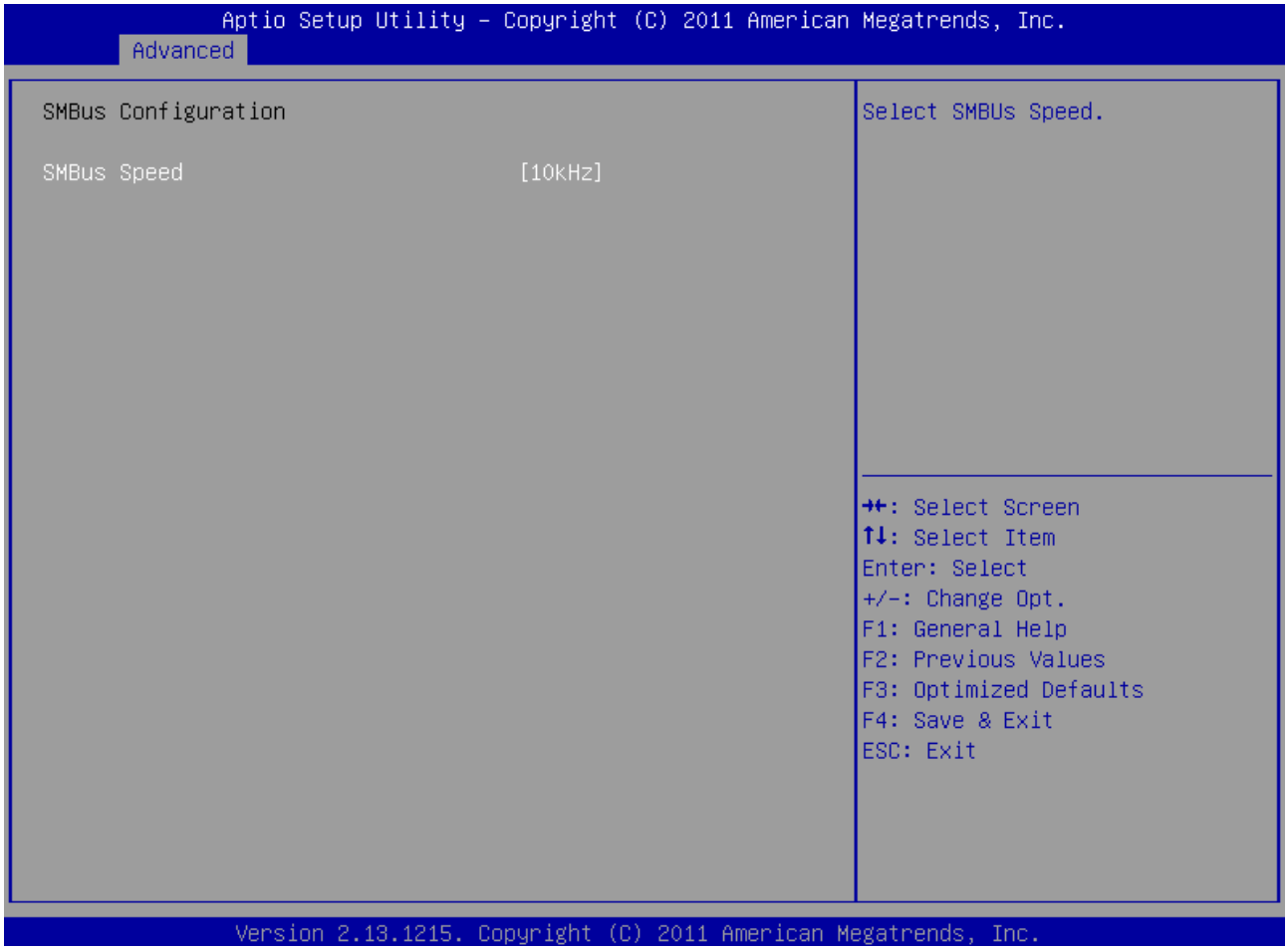


Feature	Options	Description
M.A.R.S.	Disabled **AUTO** Charger Manager	Preset M.A.R.S. Smart Battery System mode. System must be restarted to reflect mode changes
SMBAlert	Disabled **Enabled**	Enable/Disable SMBAlert# handling in chipset

Battery Information



SMBus Speed

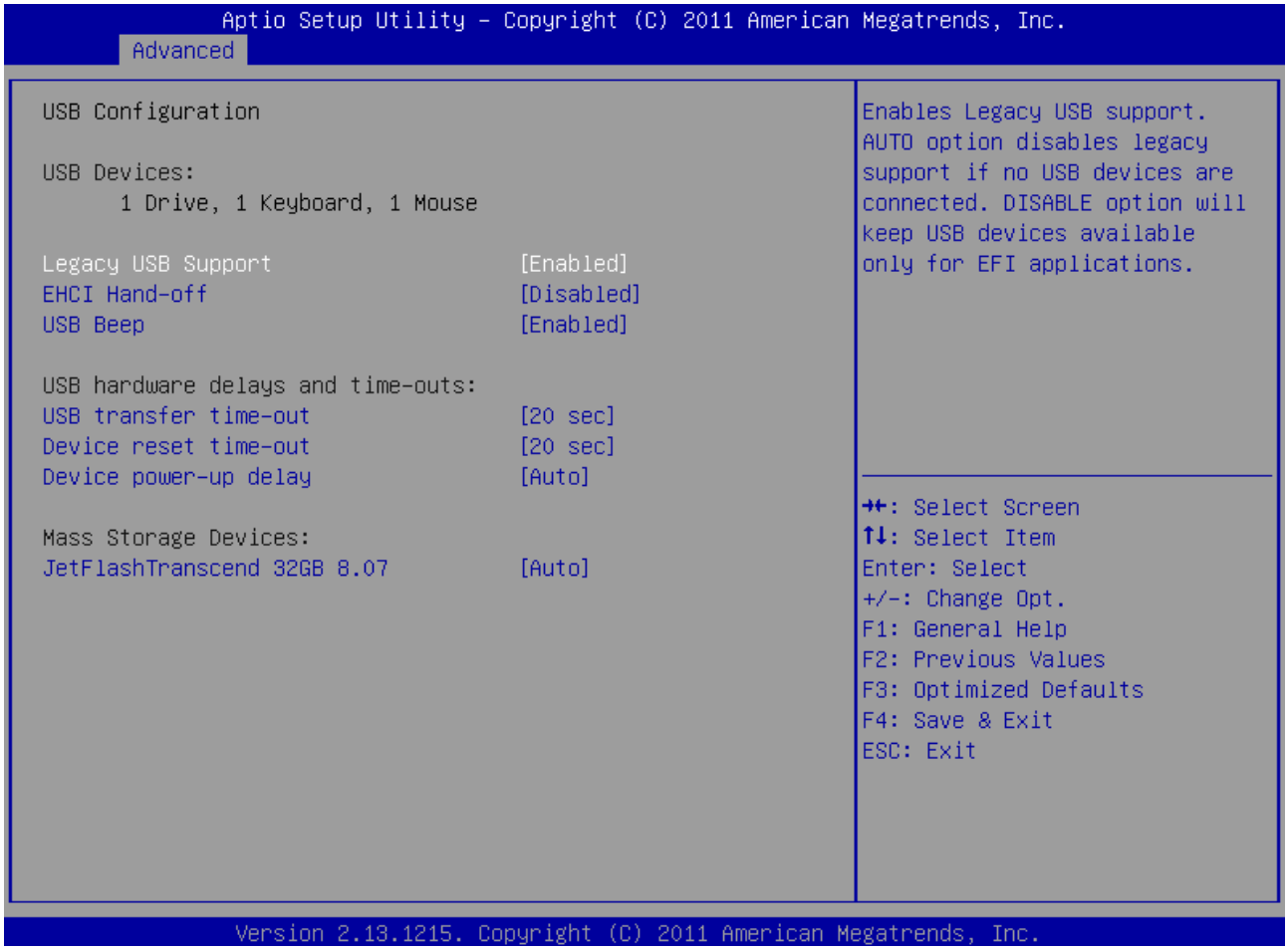


Feature	Options	Description
SMBus Speed	**10kHz** 50kHz 100kHz	Select SMBus Speed

Onboard I2C Speed

Feature	Options	Description
Onboard I2C Speed	1kHz 10kHz 50kHz 100kHz 200kHz **400kHz**	Select Onboard I2C Bus Speed in kHz, min. 1kHz, max. 400kHz

USB Configuration



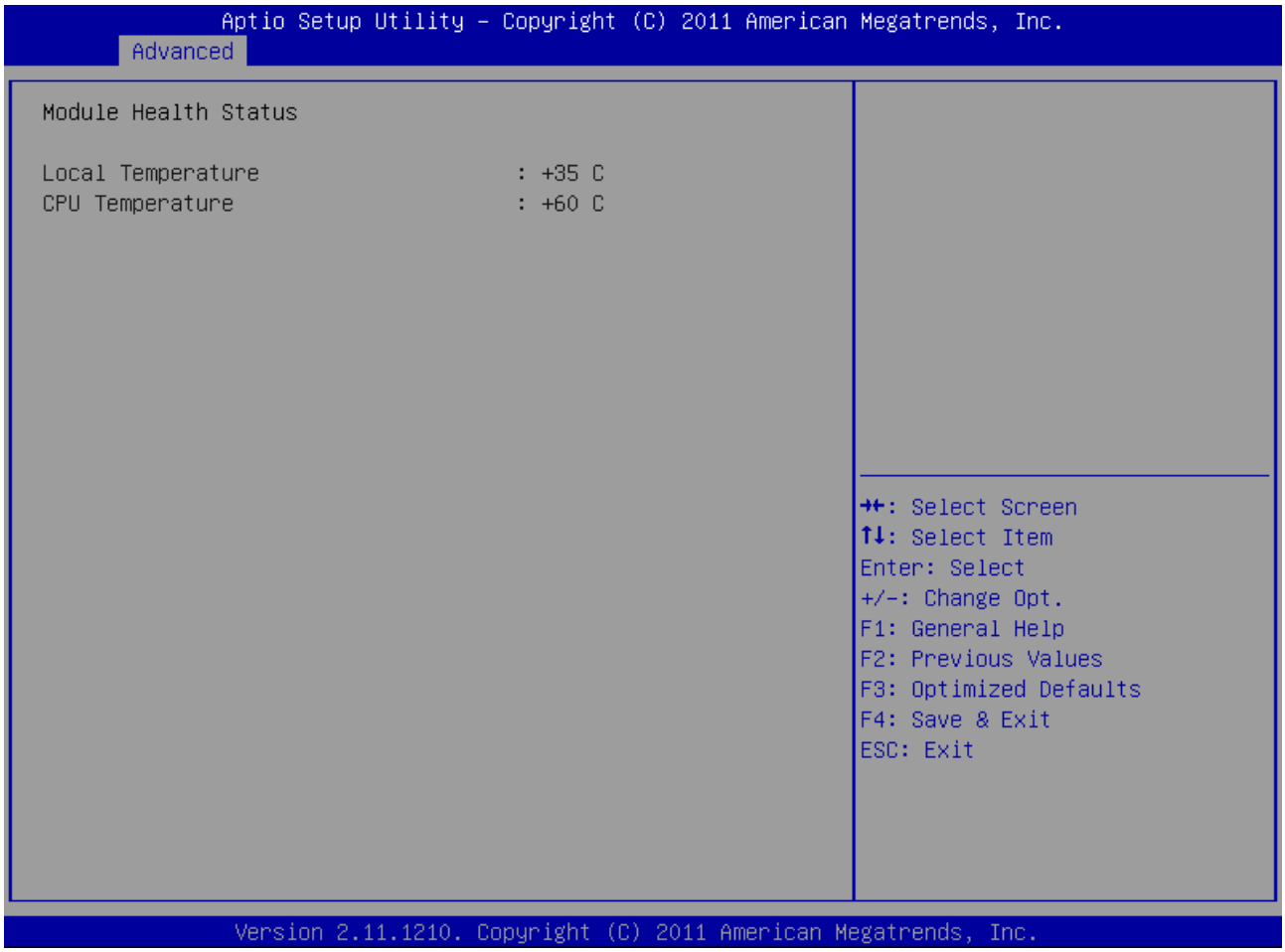
Feature	Options	Description
Legacy USB Support	**Enabled** Disabled AUTO	Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
EHCI Hand-off	**Enabled** Disabled	This is a workaround for OSes without EHCI hand-off Support. The EHCI ownership change should be claimed by EHCI driver
USB Beep	**Enabled** Disabled	Send speaker beep for device attach / detach
Device transfer time-out	1 sec 5 sec 10 sec **20 sec**	The time-out value for Control, Bulk and Interrupt transfers
Device reset time-out	10sec **20sec** 30sec 40sec	USB mass storage device Start Unit command time-out
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor
Device power-up delay in seconds	**5**	Delay range is 1..40 seconds, in one second increments

SDIO Configuration

Feature	Options	Description
SDIO Access Mode	**Auto** DMA PIO	Auto Option: Access SD device in DMA mode if controller supports it, otherwise in PIO mode. DMA Option: Access SD device in DMA mode, PIO Option: Access SD device in PIO mode
External SDIO	**Disabled** Enabled	Enable/Disable external SDIO slot on Acrrier board. If disabled, the SDIO pins for this Slot will be used as GPIOs
Ext. SDIO Clock	**25MHz** 12.5MHz 6.25MHz	Select the maximum allowable speed for the slot. Actual speed may be lower depending on controller capabilities
Onboard SDIO Clock	**25MHz** 12.5MHz 6.25MHz	Select the maximum allowable speed for the slot. Actual speed may be lower depending on controller capabilities
PowerOn Delay	10 **50ms** 200ms 500ms 1s	Select SDIO PowerOn Delay

Module H/W Monitor

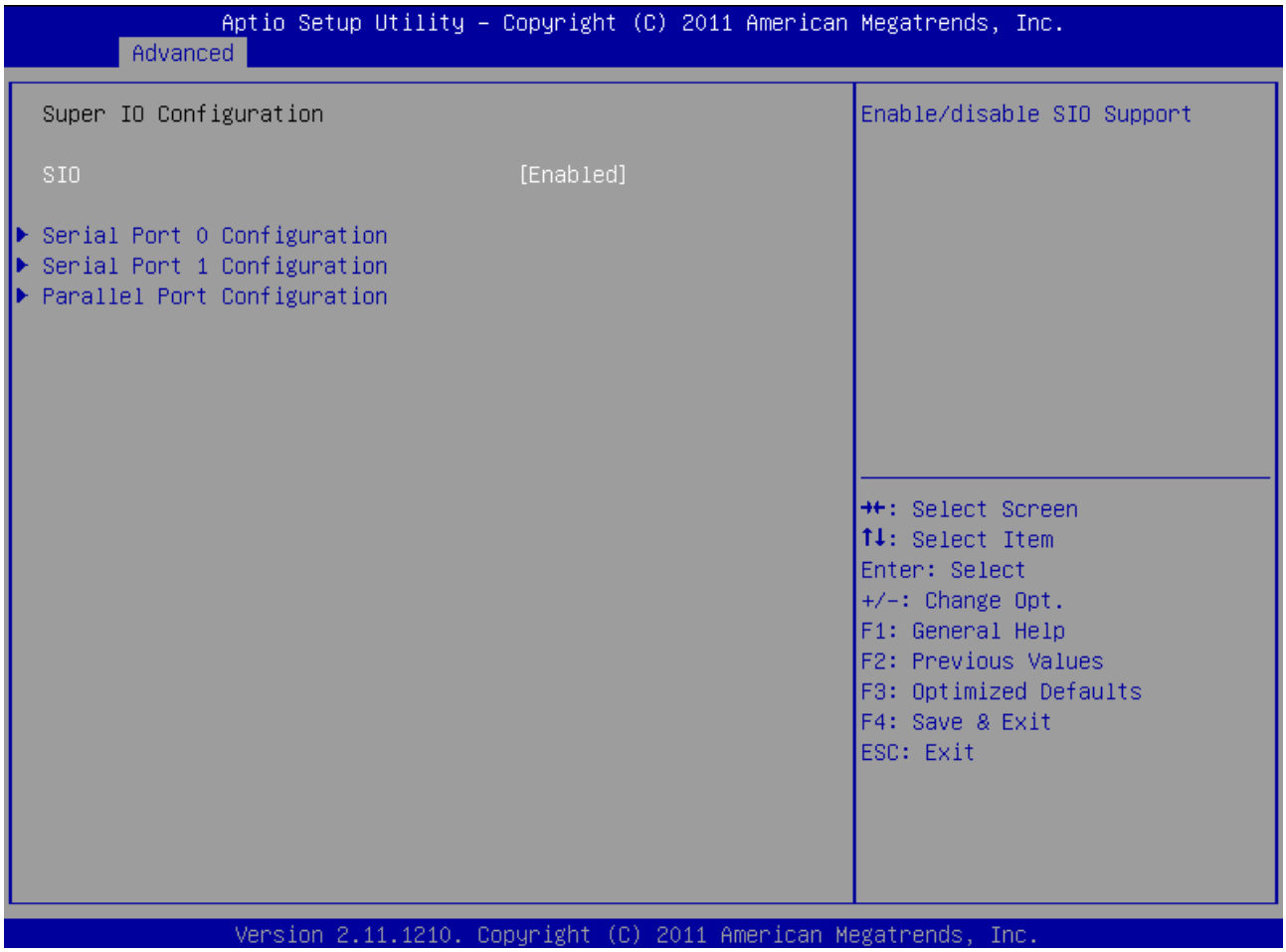
Hardware Monitor measurements and configuration for the onboard WINBOND W83L771W.



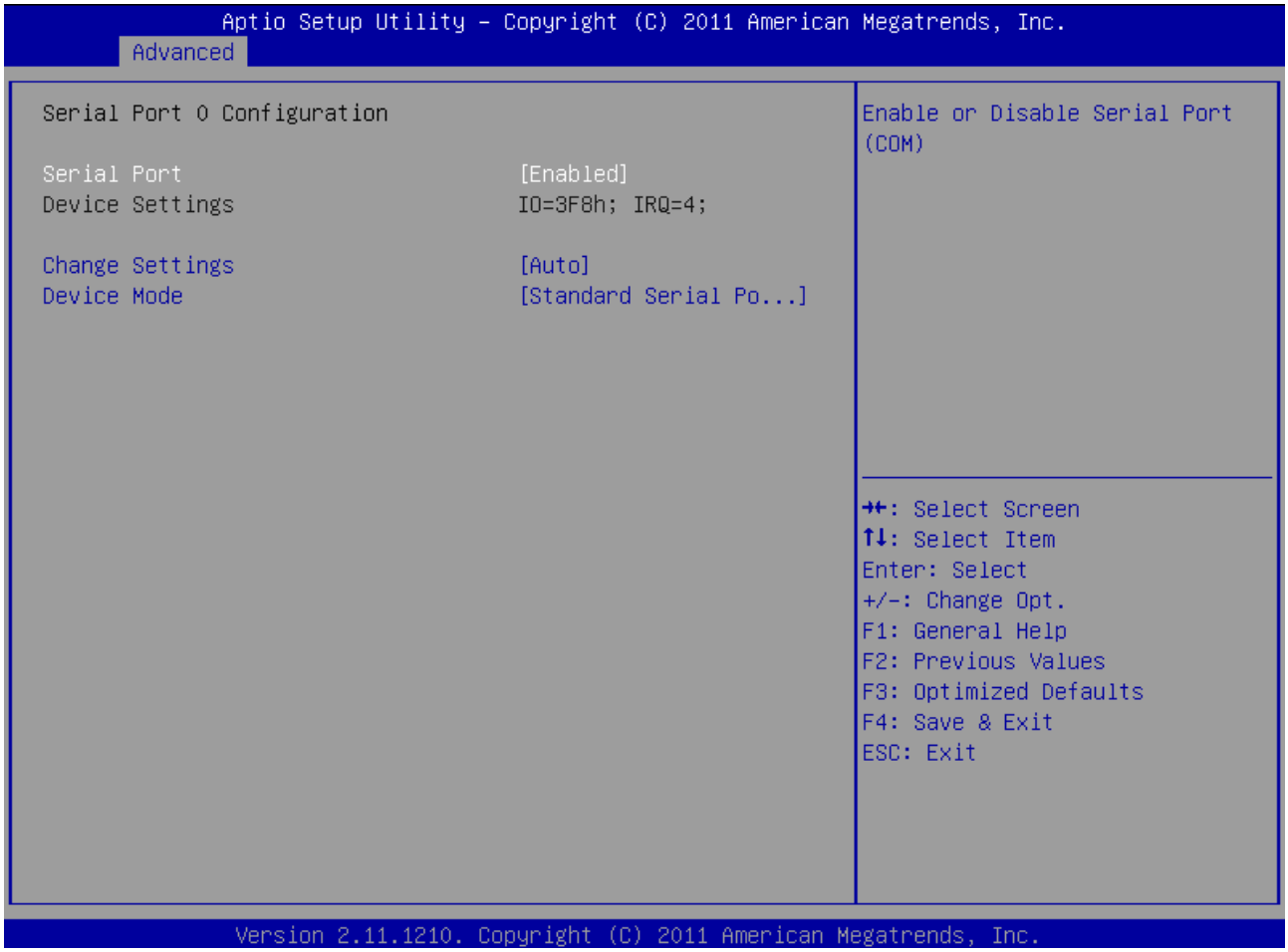
Feature	Value/Options	Description
Local Temperature	xx°C	Shows the internal temperature of onboard HWM
CPU Temperature	xx°C	Shows the measured temperature of the CPU Diode with onboard HWM

Super IO Configuration

This setup option is available if a LPC SuperI/O Nuvoton 83627 is present on the baseboard. By default the COMe-mTT10 supports the legacy interfaces of a 5V 83627HF(J) or 3.3V 83627DHG-P on external LPC. The hardware monitor is not supported in setup.



Serial Port 0 Configuration

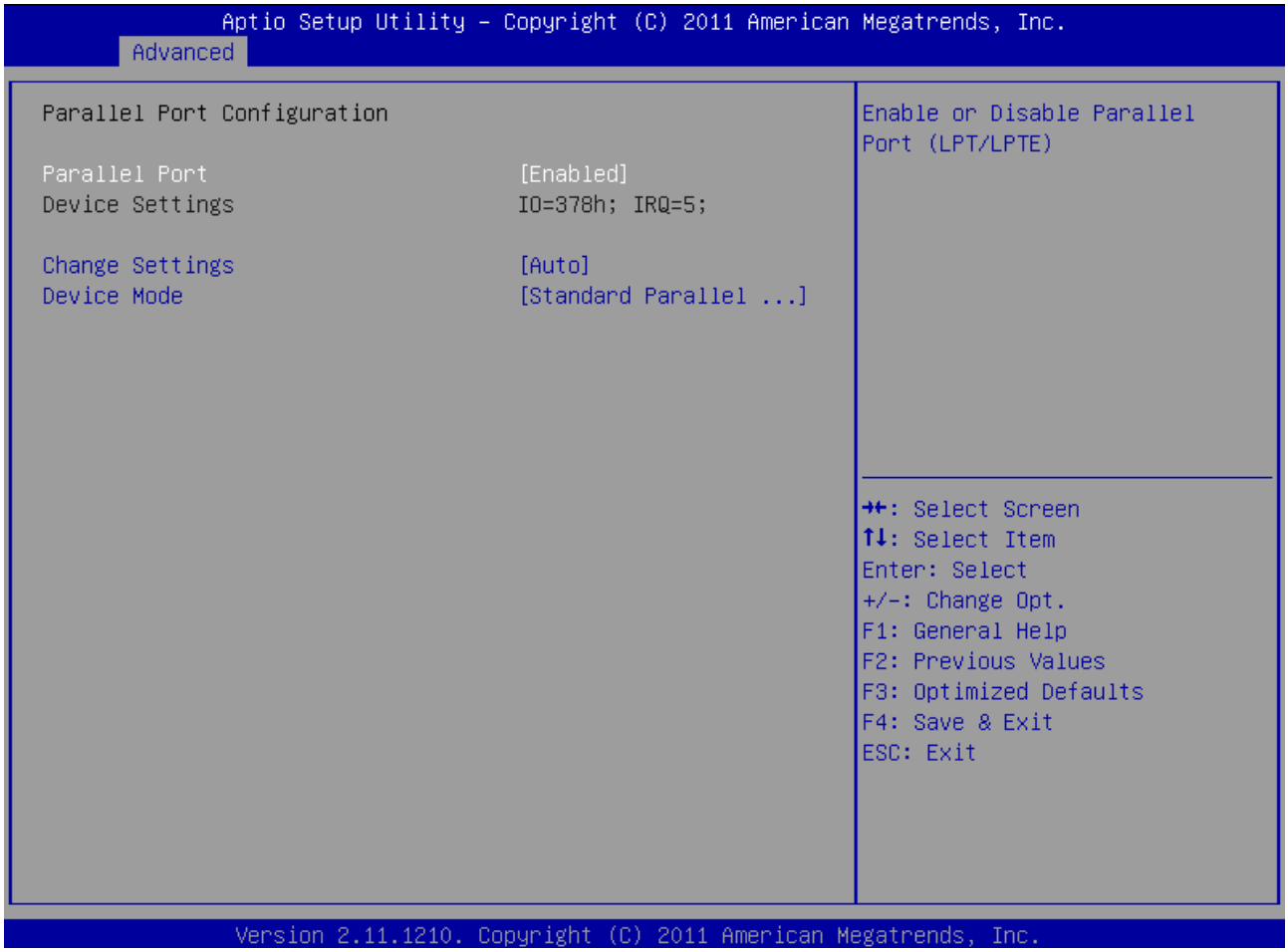


Feature	Options	Description
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM) 0
Change Settings	**AUTO** IO=3F8h; IRQ=4; IO=3F8h, IRQ=3,4,5,6,7,10,11,12; IO=2F8h, IRQ=3,4,5,6,7,10,11,12; IO=3E8h, IRQ=3,4,5,6,7,10,11,12; IO=2E8h, IRQ=3,4,5,6,7,10,11,12;	Select an optimal setting for SuperIO device.
Device Mode	**Standard Serial Port Mode** IrDA 1.0 (HP SIR) Mode ASKIR Mode	Change the Serial Port mode.

Serial Port 1 Configuration

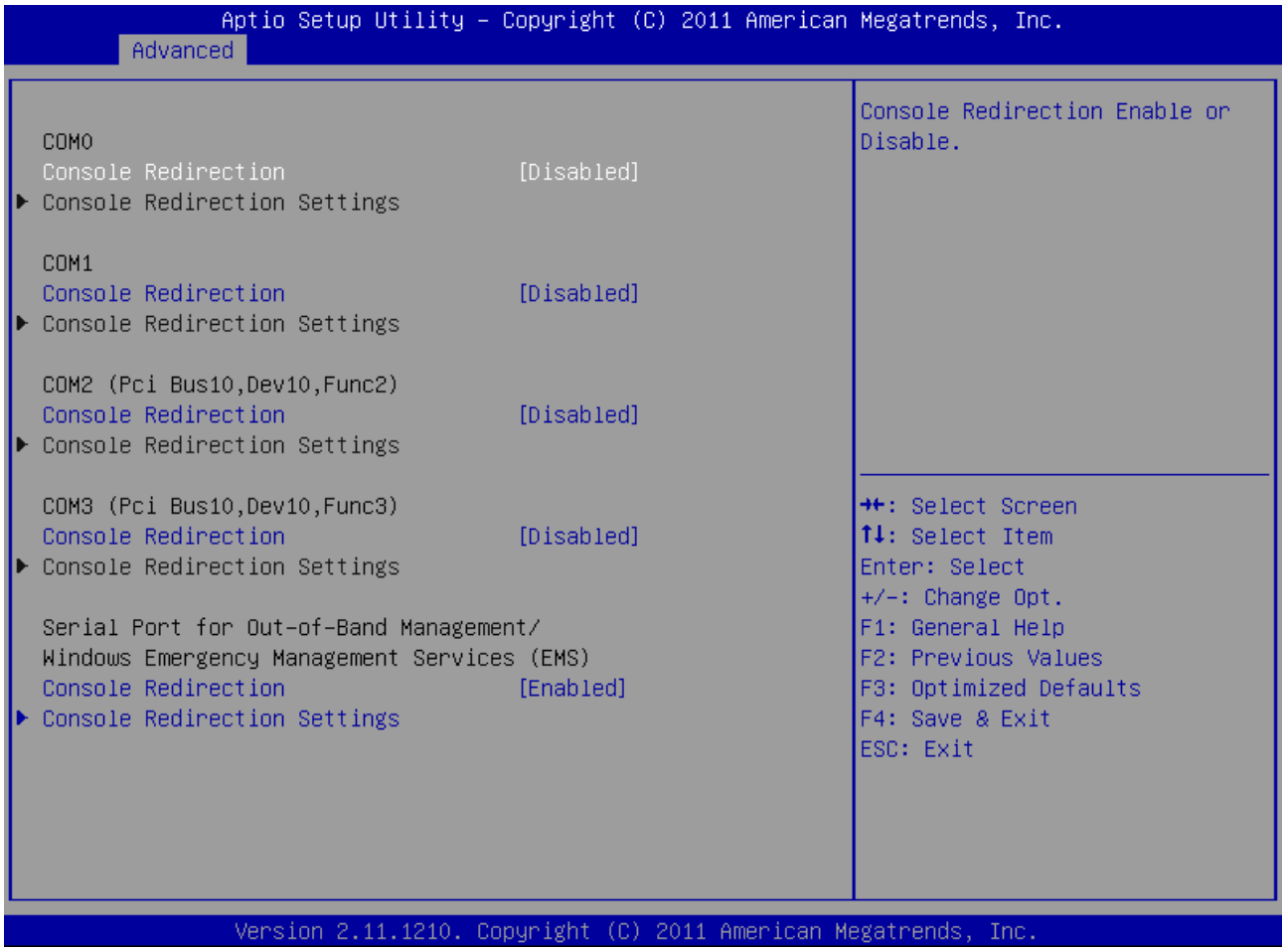
Feature	Options	Description
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM) 1
Change Settings	**AUTO** IO=2F8h; IRQ=3; IO=3F8h, IRQ=3,4,5,6,7,10,11,12; IO=2F8h, IRQ=3,4,5,6,7,10,11,12; IO=3E8h, IRQ=3,4,5,6,7,10,11,12; IO=2E8h, IRQ=3,4,5,6,7,10,11,12;	Select an optimal setting for SuperIO device.
Device Mode	**Standard Serial Port Mode** IrDA 1.0 (HP SIR) Mode ASKIR Mode	Change the Serial Port mode.

Parallel Port Configuration



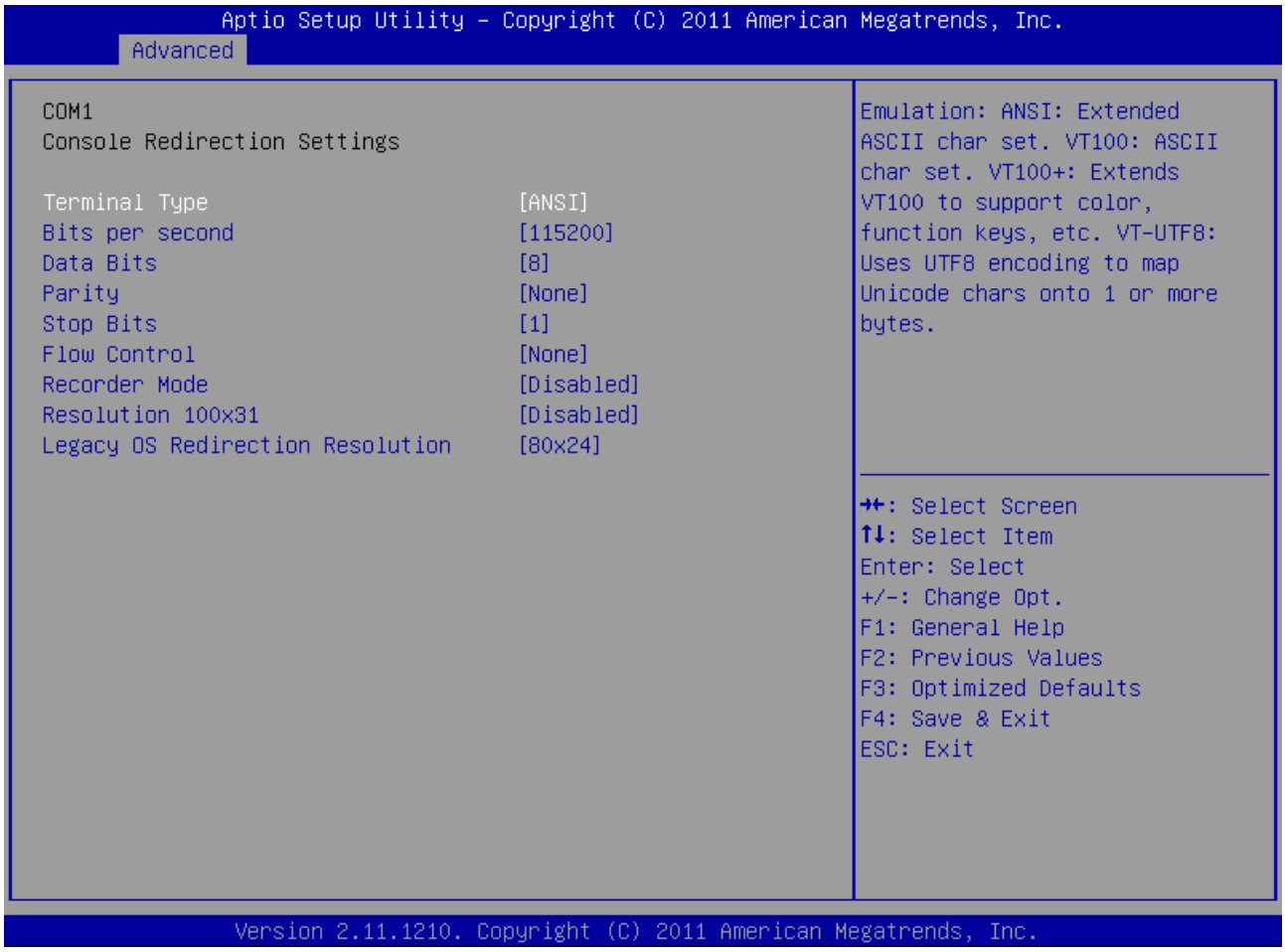
Feature	Options	Description
Parallel Port	Disabled **Enabled**	Enable or Disable the Parallel Port (LPT/LPTE)
Change Settings	**AUTO** IO=378h; IRQ=5; IO=378h, IRQ=5,6,7,10,11,12; IO=278h, IRQ=5,6,7,10,11,12; IO=3BCh, IRQ=5,6,7,10,11,12; IO=378h; IO=278h; IO=3BCh;	Select an optimal setting for SuperIO device.
Device Mode	**Standard Parallel Port Mode** EPP Mode ECP Mode EPP Mode & ECP Mode	Change the Printer Port mode.

Serial Port Console Redirection



Feature	Options	Description
Console Redirection	**Disabled** Enabled	Enable/Disable Serial Port COM0 Console Redirection
Console Redirection	**Disabled** Enabled	Enable/Disable Serial Port COM1 Console Redirection
Console Redirection	**Disabled** Enabled	Enable/Disable Serial Port COM2 Console Redirection
Console Redirection	**Disabled** Enabled	Enable/Disable Serial Port COM3 Console Redirection
Console Redirection	Disabled **Enabled**	Enable/Disable Serial Port for Out-of-Band Management / Windows EMS

COM0-3 Console Redirection Settings

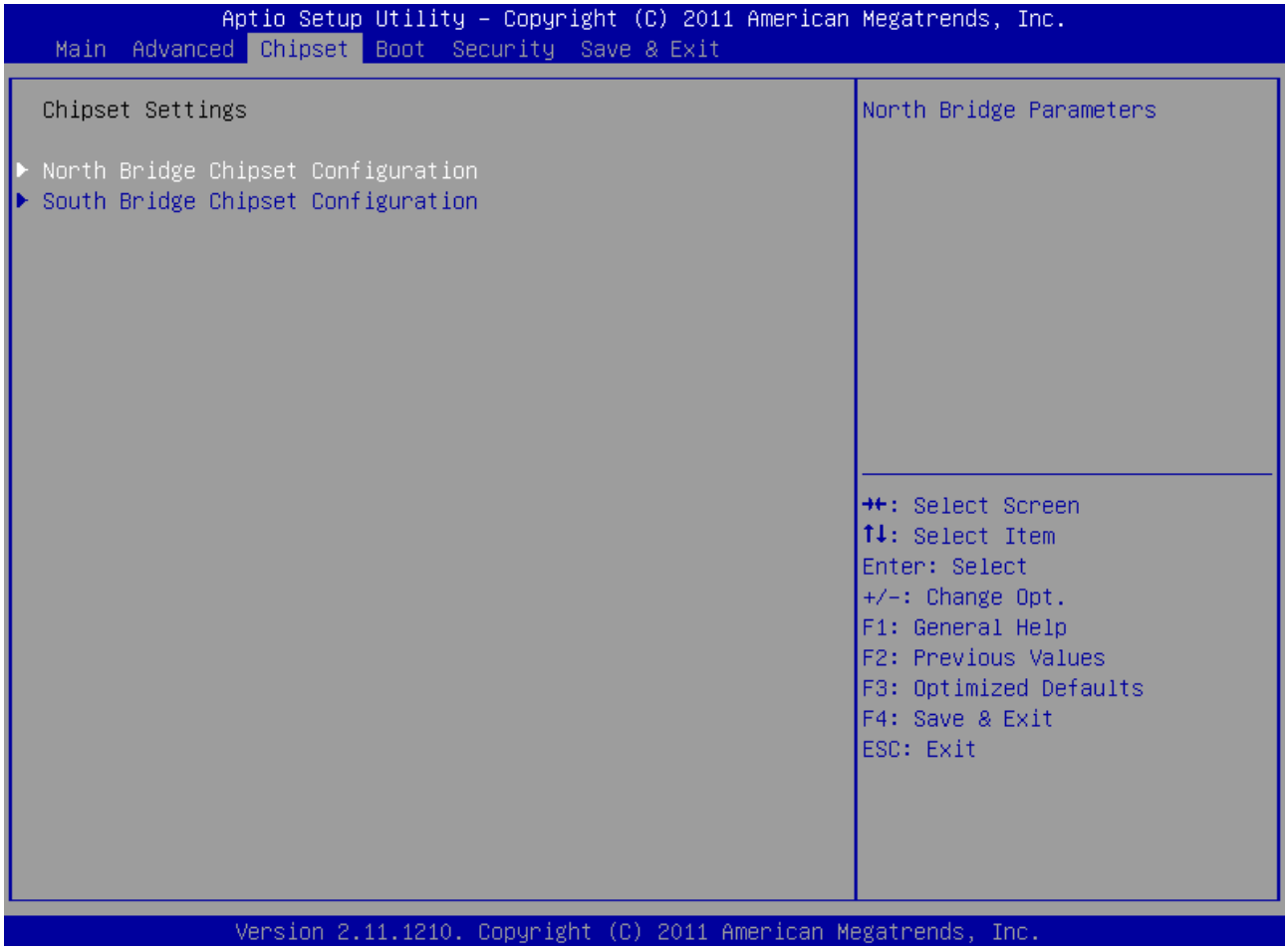


Feature	Options	Description
Terminal Type	VT100 VT100+ VT_UTF8 **ANSI**	VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes ANSI: Extended ASCII char set.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds
Data Bits	7 **8**	Data Bits
Parity	**None** Even Odd Mark Space	A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.
Stop Bits	**1** 2	Stop Bits indicate the end of a serial data packet. (A Start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Flow Control	**None** Hardware RTS/CTS	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals
Recorder Mode	**Disabled** Enabled	With this mode enabled only text will be sent. This is to capture terminal data.
Resolution 100×31	**Disabled** Enabled	Enables or disables extended terminal resolution
Legacy OS Redirection Resolution	**80×24** 80×25	On Legacy OS, the Number of Rows and Columns supported redirection

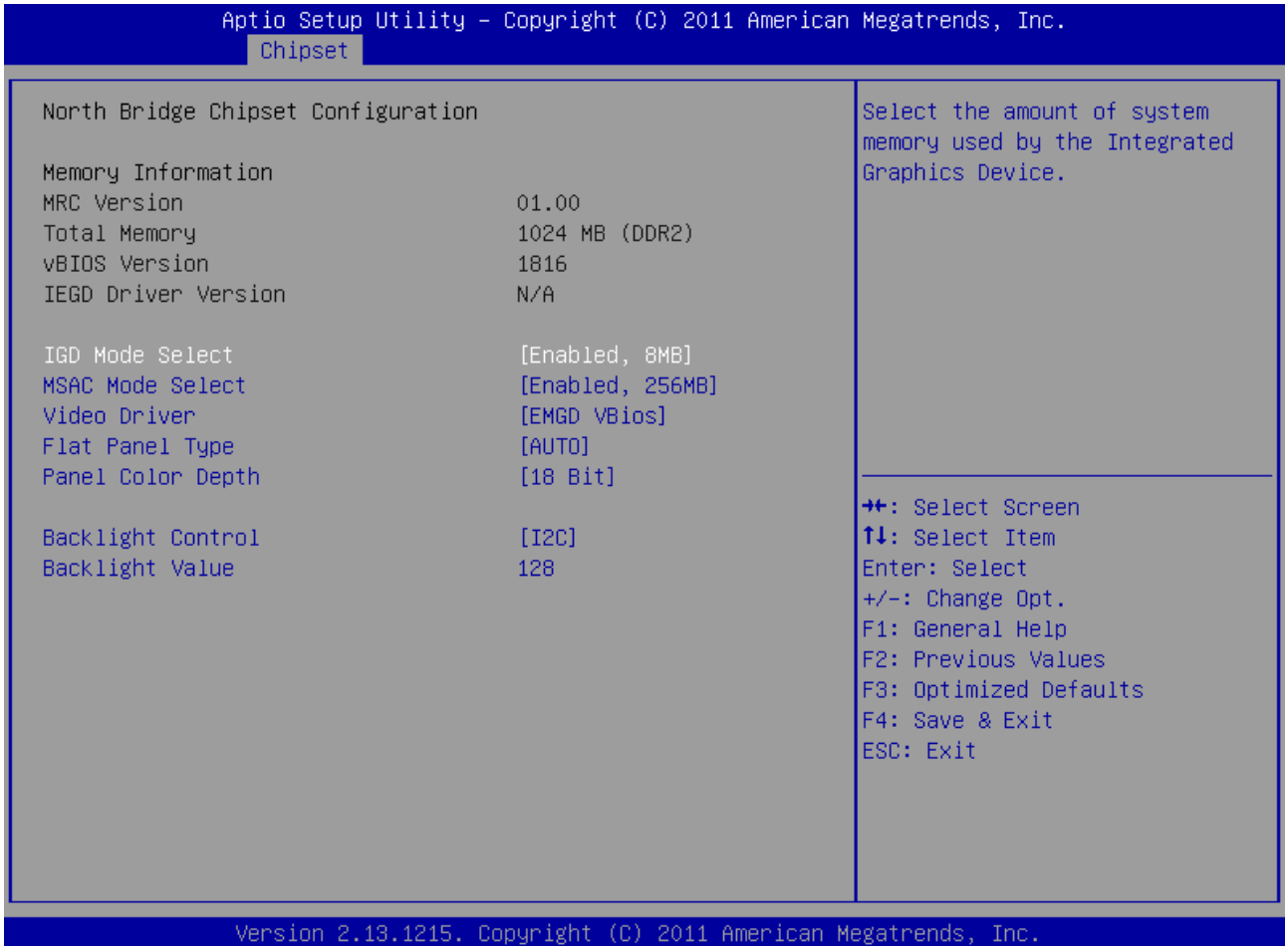
Out-of-Band Management Port Console Redirection Settings

Feature	Options	Description
Out-of-Band Mgmt Port	COM0 COM1 COM2 (PCI Bus10,Dev10,Func2) COM3 (PCI Bus10,Dev10,Func3)	Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port
Terminal Type	VT100 VT100+ VT_UTF8 **ANSI**	VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes ANSI: Extended ASCII char set.
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds
Flow Control	**None** Hardware RTS/CTS Software Xon/Xoff	Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals

7.5.3 Chipset


Aptio Setup Utility – Copyright (C) 2011 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Chipset Settings
North Bridge Chipset Configuration
South Bridge Chipset Configuration
North Bridge Parameters
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.11.1210. Copyright (C) 2011 American Megatrends, Inc.

North Bridge Chipset Configuration

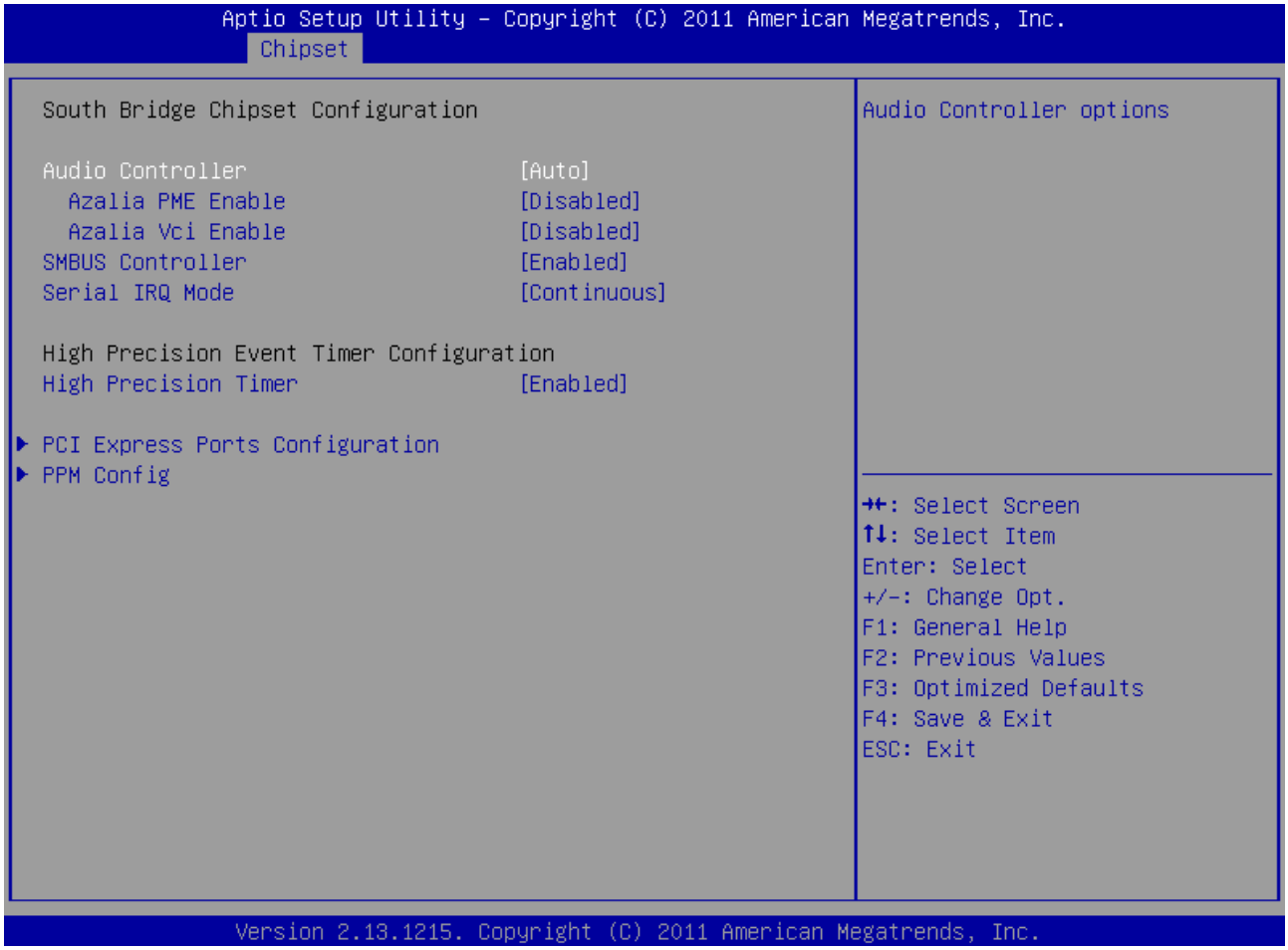


Feature	Options	Description
IGD Mode Select	Disabled Enabled, 1MB Enabled, 4MB **Enabled, 8MB** Enabled, 16MB Enabled, 32MB Enabled, 48MB Enabled, 64MB	Select the amount of system memory used by the Integrated Graphics Device
MSAC Mode Select	Enabled, 512MB **Enabled, 256MB** Enabled, 128MB	Select the size of the graphics memory aperture and untrusted space. Used by the Integrated Graphics Device
Video Driver	**EMGD VBIOS** EMGD GOP	Select VBIOS if legacy support is required, GOP to speed up POST
Flat Panel Type	**AUTO** LVDS 800×600 18Bit	AUTO configuration supports SDVO. If no monitor attached, LVDS will be activated. Use VESA EDID to auto-configure LVDS Panels
Panel Color Depth	**18 Bit** 24 Bit	For internal LVDS EDID detection, select the Panel Color Depth
Backlight Control	None/External PWM I2C	Backlight Control Setting
Backlight Value	**128**	Set LCD backlight brighness

Auto detection is only working with EDID panel data. Set Flat Panel Type to SVGA if your panel is not detected automatically or when using a LVDStoDVI solution with DVI Monitor resolution over 1280x768, 80MHz.

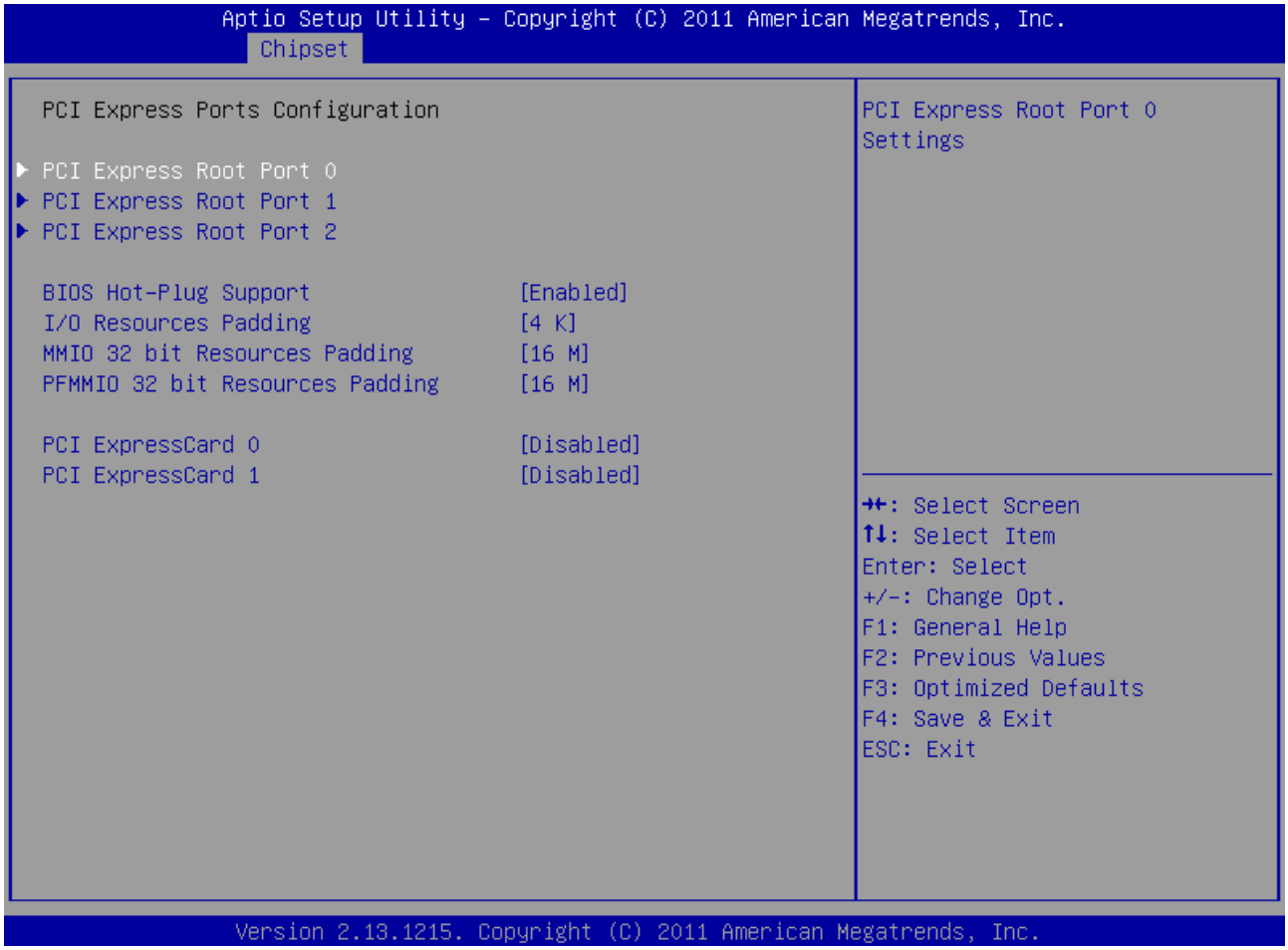
Due to space limitations due to simultaneous SDVO and LVDS support only one manual LVDS resolutions is supported in setup. With Intel® EMGD you can change this resolution and create a new VideoBIOS according your requirements. Please contact your local support to implement your customized VBIOS into the BIOS

South Bridge Chipset Configuration



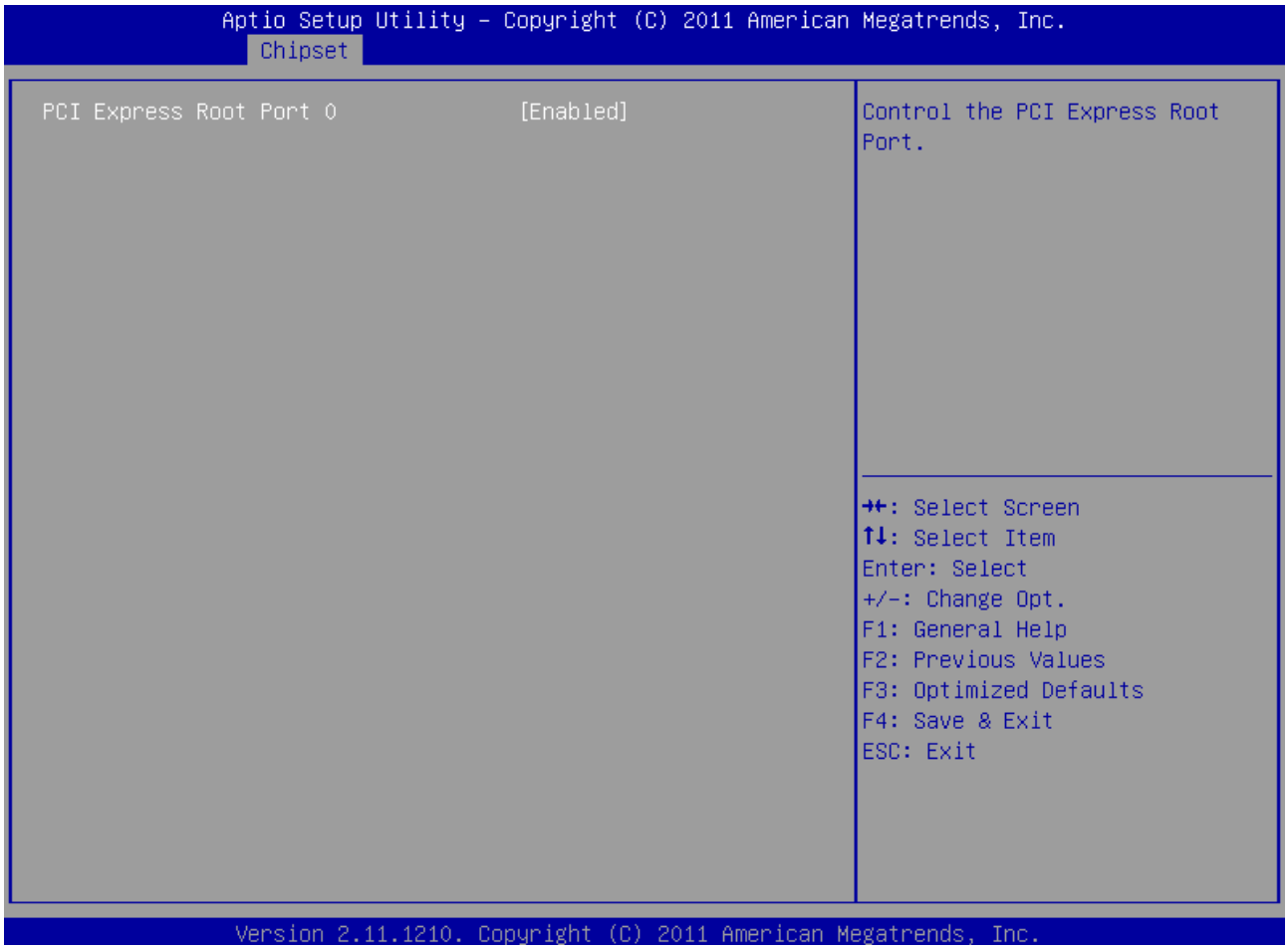
Feature	Options	Description
Audio Controller	Disabled Enabled **Auto**	Control Detection of the High definition audio (Azalia) device. Disabled = HDaudio will be unconditionally disabled. Enabled = HDaudio will be unconditionally enabled. Auto = HDaudio will be enabled if present, disabled otherwise
- Azalia PME Enable	**Disabled** Enabled	Enable/Disable Power Management capability of Audio Controller
- Azalia Vci Enable	**Disabled** Enabled	Enable/Disable Azalia Vci
SMBUS Controller	Disabled **Enabled**	SMBus Controller options
Serial IRQ Mode	Disabled **Enabled**	SMBus Controller options
High Precision Timer	**Continuous** **Quiet**	Set the Serial IRQ Mode

PCI Express Ports Configuration



Feature	Options	Description
BIOS Hot-Plug Support	Disabled **Enabled**	If ENABLED allows BIOS build in Hot-Plug Support. Use this feature if OS does not support PCI Express and SHPC hot-plug natively
I/O Resources Padding	**Disabled** 4 K 8 K 16 K 32 K	Padd PCI I/O Resources bihing the bridge for Hot-Plug
MMIO 32 bit Resources Padding	Disabled 1 M 2 M 4 M 8 M **16 M** 32 M 64 M 128 M	Padd PCI MMIO 32-bit Resources behind the bridge for Hot-Plug
PFMMIO 32 bit Resources Padding	Disabled 1 M 2 M 4 M 8 M **16 M** 32 M 64 M 128 M	Padd PCI MMIO 32-bit Prefetchable Resources behind the bridge for Hot-Plug
PCI Express Card 0	Port 0 Port 1 Port 2 Disabled	Controls PCIe Port for ExpressCard support
PCI Express Card 1	Port 0 Port 1 Port 2 Disabled	Controls PCIe Port for ExpressCard support

PCI Express Root Port 0/1/2

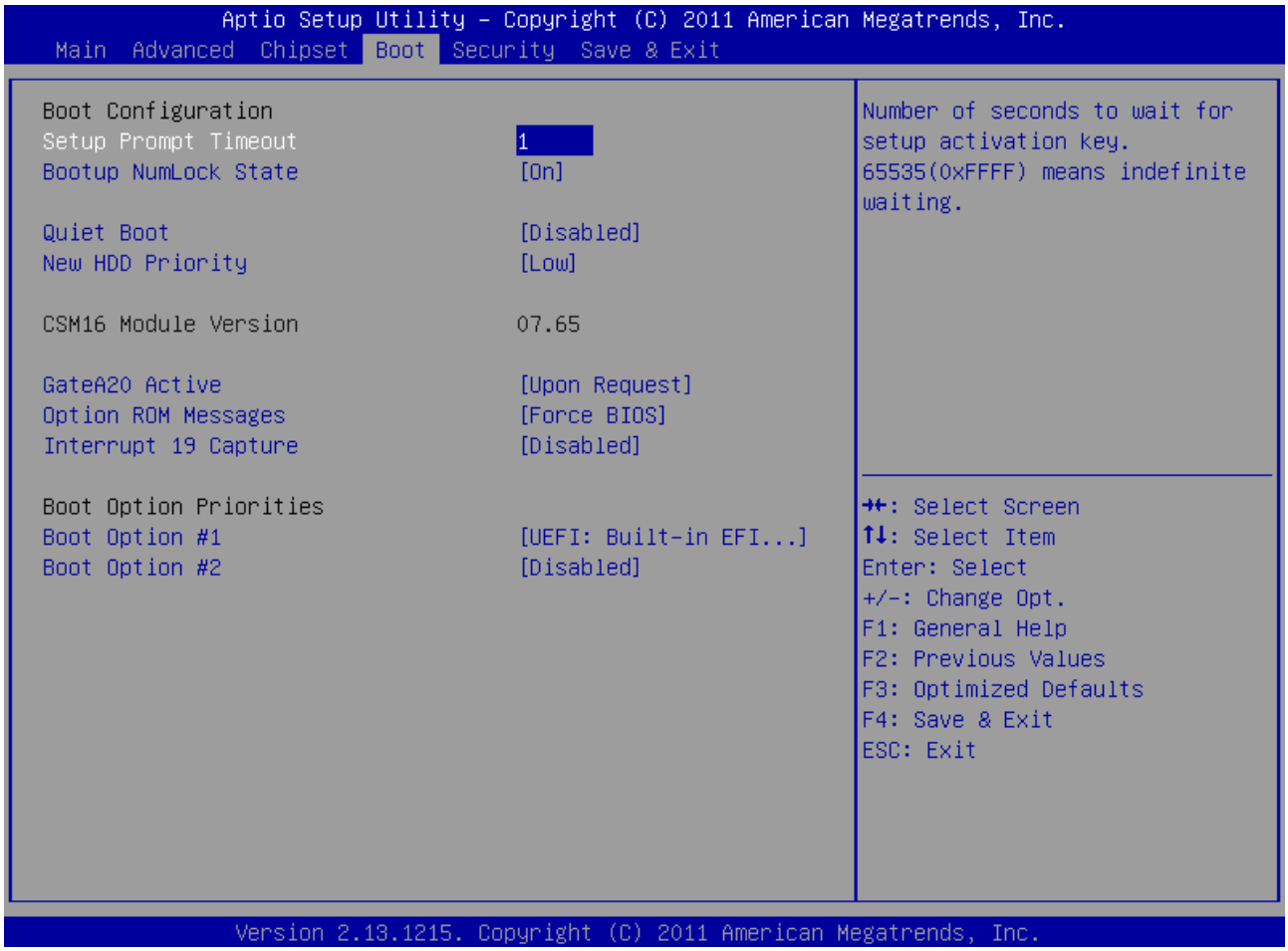


Feature	Options	Description
PCI Express Root Port	Disabled **Enabled**	Control the PCI Express Root Port

PPM Config

Feature	Options	Description
C-State POPUP	Disabled **Enabled**	Enable/Disable C-state POPUP

7.5.4 Boot



Feature	Options	Description
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means idefinite waiting. 0 means no wait (not recommended)
Bootup NumLock State	**On** Off	Select the keyboard NumLock state
Quiet Boot	**Disabled** Enabled	Enables/Disables Quiet Boot option (Boot logo)
New HDD Priority	**Low** High	Boot priority for new connected HDD
GateA20 Active	**Upon Request** Always	Upon Request: GA20 can be disabled using BIOS services. Always: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB
Option ROM Messages	**Force BIOS** Keep Current	Set display mode for Option ROM
Interrupt 19 Capture	**Disabled** Enabled	Enabled: Allows Option ROMs to trap INT19
Boot Option #1 Boot Option #2 Boot Option #3 ...	**Boot Device** Disabled	Set the system boot order by device group
Hard Drive BBS Priorities	-	Set the order of the legacy devices in this group
CD/DVD ROM Drive BBS Priorities	-	Set the order of the legacy devices in this group
Floppy Drive BBS Priorities	-	Set the order of the legacy devices in this group

Boot Option Priority

By default, AMI APTIO uses following boot priority if at least on device of a group is connected:

» Boot Option #1: Prio 1 Hard Disk

» Boot Option #2: Built-in EFI Shell

» Boot Option #3: Prio 1 HDD UEFI boot option

» Boot Option #4: Prio 1 CD/DVD ROM Drive

» Boot Option #5: Prio 1 Floppy UEFI boot option

» Boot Option #6: Prio 1 Floppy Drive

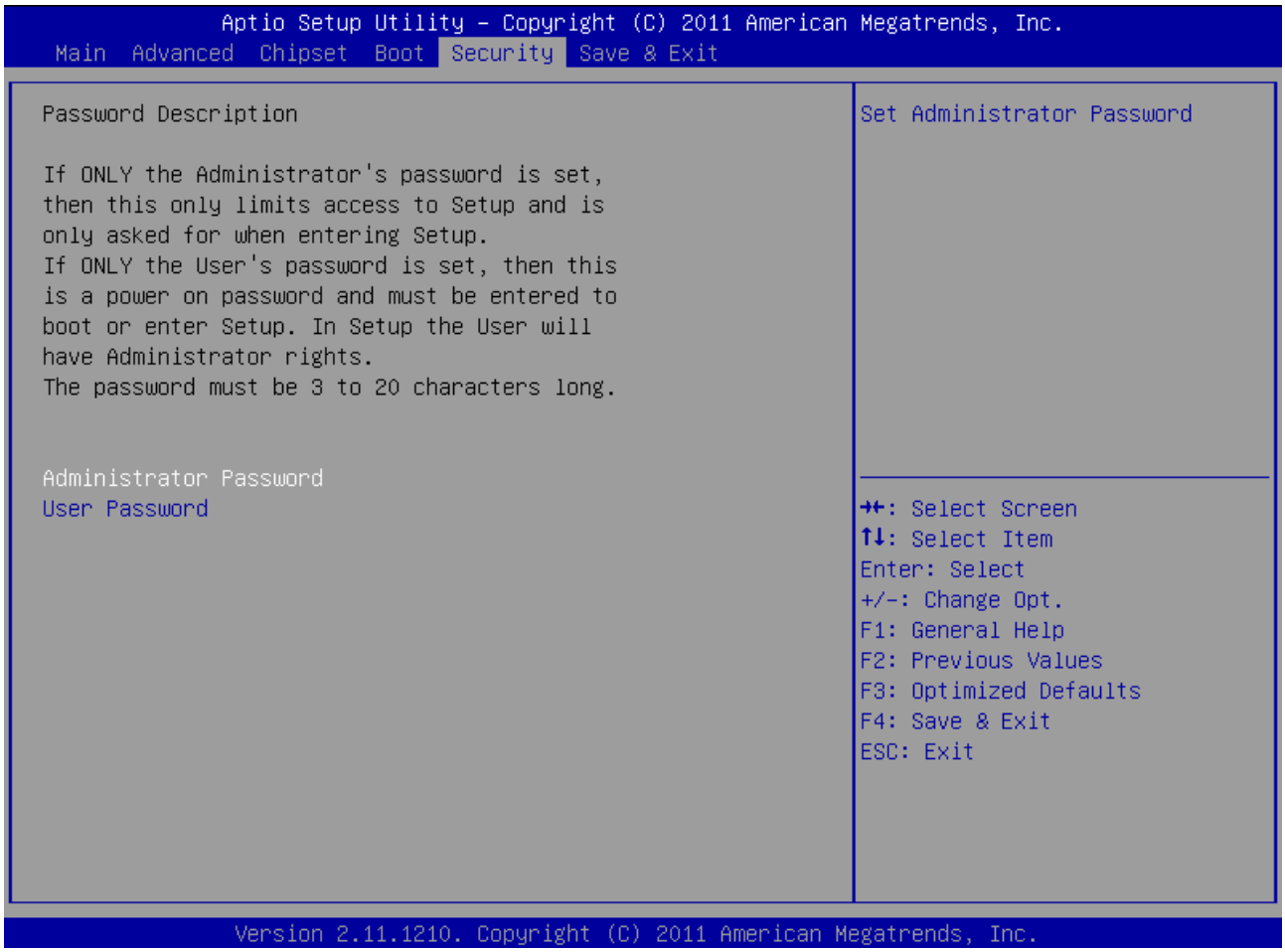
HDD and CD/DVD-ROM group internal drive priority

The internal device priority for Hard Disks and Optical drives is:

» 1. SATA #0/#1

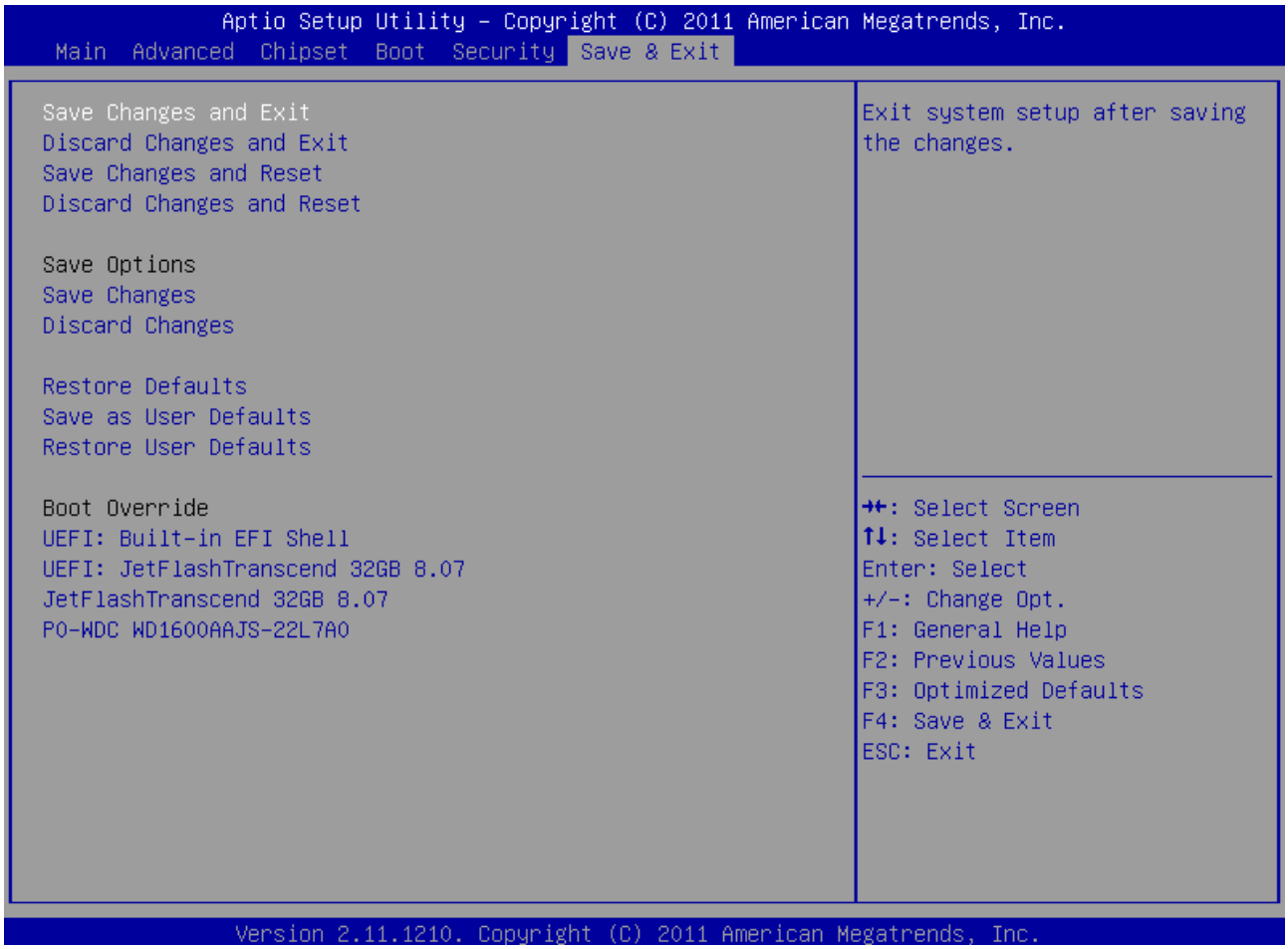
» 2. USB

7.5.5 Security



Feature	Options	Description
Administrator Password	-	Set the Administrator Password for Setup Access
User Password	-	Set User Password

7.5.6 Save & Exit



Feature	Options	Description
Save Changes and Exit	-	Exit system setup after saving the changes
Discard Changes and Exit	-	Exit system setup without saving any changes
Save Changes and Reset	-	Reset system after saving the changes
Discard Changes and Reset	-	Reset system without saving any changes
Save Changes	-	Save changes made so far to any of the setup options
Discard Changes	-	Discard changes made so far to any of the setup options
Restore Defaults	-	Restore/Load Default values for all the setup options
Save as User Defaults	-	Save the changes made so far as User Defaults
Restore User Defaults	-	Restore the User Defaults to all the setup options
Boot Override	List of all boot options	Boot directly from selected device

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