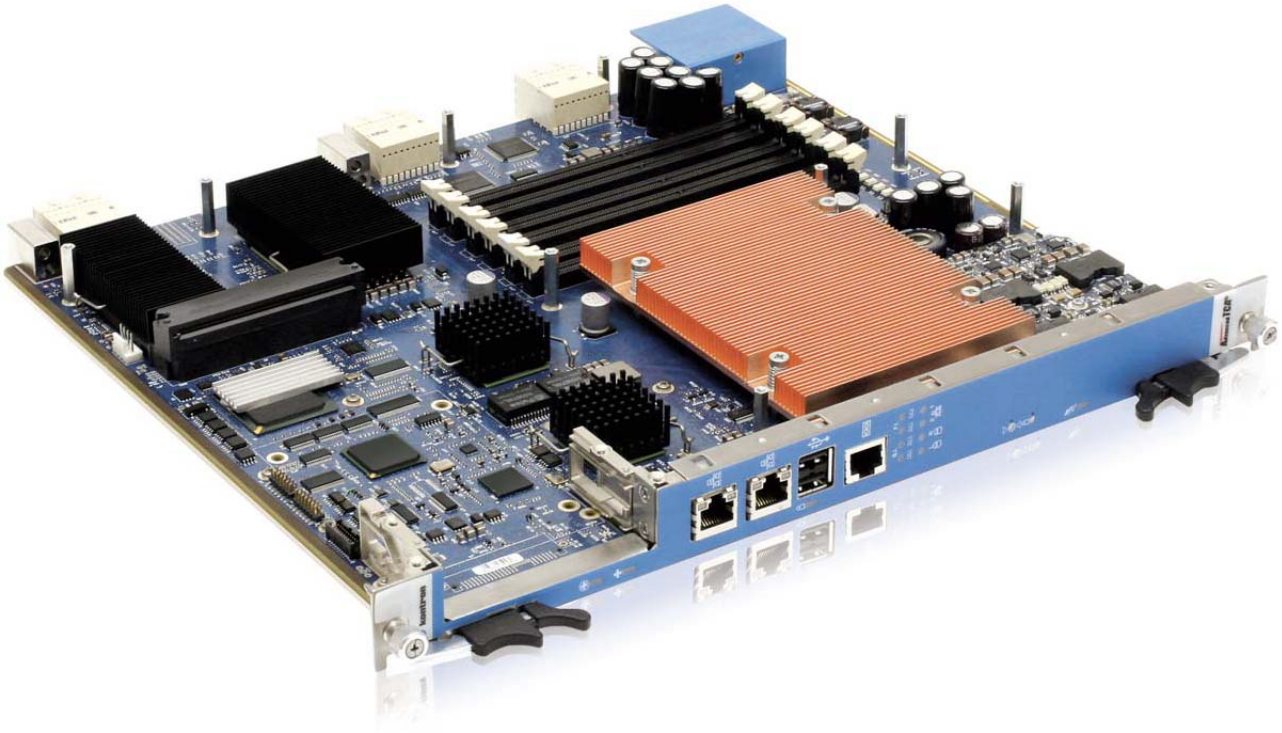
kontron

# »Kontron User's Guide«

AdvancedTCA®



## AT8050

Document Revision 1.10
January 2016

# Revision History

| Rev. Index | Brief Description of Changes | Date of Issue |
|---|---|---|
| 1.0 | First Release | April 2009 |
| 1.1 | Second Release | November 2009 |
| 1.2 | Third Release | April 2010 |
| 1.3 | Fourth Release | September 2011 |
| 1.4 | Fifth Release | October 2013 |
| 1.5 | Sixth Release | January 2014 |
| 1.6 | Sel size corrected | May 2014 |
| 1.7 | Change declaration of FCC Compliance statements from Class B to Class A. | September 2014 |
| 1.8 | OS Compatibility update | July 2015 |
| 1.9 | Watchdog timer sub-menu update | July 2015 |
| 1.10 | OS Compatibility update | January 2016 |
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| | | |

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other publications. Customers may alter this user's guide and publish it only after they remove the Kontron name, cover, and logo.

Kontron reserves the right to make changes without notice in product or component design as warranted by evolution in user needs or progress in engineering or manufacturing technology. Changes that affect the operation of the unit will be documented in the next revision of this user's guide.

# Table of Contents

# List of Figures

# List of Tables

# Safety Instructions

## Before You Begin

Before handling the board, read the instructions and safety guidelines on the following pages to prevent damage to the product and to ensure your own personal safety. Refer to the "Advisories" section in the Preface for advisory conventions used in this user's guide, including the distinction between Warnings, Cautions, Important Notes, and Notes.

- Always use caution when handling/operating the computer. Only qualified, experienced, authorized electronics service personnel should access the interior of the computer. The power supplies produce high voltages and energy hazards, which can cause bodily harm.
- Use extreme caution when installing or removing components. Refer to the installation instructions in this user's guide for precautions and procedures. If you have any questions, please contact Kontron Technical Support

**WARNING**

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.

# Preventing Electrostatic Discharge

Static electricity can harm system boards. Perform service at an ESD workstation and follow proper ESD procedure to reduce the risk of damage to components. Kontron strongly encourages you to follow proper ESD procedure, which can include wrist straps and smocks, when servicing equipment.

Take the following steps to prevent damage from electrostatic discharge (ESD):

- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Don't touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.
- When you want to remove the protective foil (if present), make sure you are properly grounded and that you touch a metalic part of the board.

**CAUTION**

Removing the protective foil from the top and bottom cover might create static.
When you remove those protections, make sure you follow the proper ESD procedure.

# Preface

## How to Use This Guide

This user's guide is designed to be used as step-by-step instructions for installation, and as a reference for operation, troubleshooting, and upgrades.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

The following is a summary of chapter contents:

- Chapter 1, Product Description
- Chapter 2, Board Features
- Chapter 3, Installing the board
- Chapter 4, Hardware Management
- Chapter 5, Software Setup
- Chapter 6, Thermal Considerations
- Appendix A, Memory & I/O Maps
- Appendix B, Connector Pinout
- Appendix C, BIOS Setup Error Codes
- Appendix D, Software Update
- Appendix E, Getting Help
- Appendix F, Glossary

# Customer Comments

If you have any difficulties using this user's guide, discover an error, or just want to provide some feedback, please send a message to: Tech.Writer@ca.kontron.com. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user's guide on our Web site. Thank you.

# Advisory Conventions

Seven types of advisories are used throughout the user guides to provide helpful information or to alert you to the potential for hardware damage or personal injury. They are Note, Signal Paths, Jumpers Settings, BIOS Settings, Software Usage, Cautions, and Warnings. The following is an example of each type of advisory. Use caution when servicing electrical components.

**Note:**
Indicate information that is important for you to know.

**Signal Path:**
Indicate the places where you can fin the signal on the board.

**Jumper Settings:**
Indicate the jumpers that are related to this sections.


**BIOS Settings:**
Indicate where you can set this option in the BIOS.

**Software Usage:**
Indicates how you can access this feature through software.

**CAUTION**
Indicate potential damage to hardware and tells you how to avoid the problem.

**WARNING**
Indicates potential for bodily harm and tells you how to avoid the problem.

**ESD Sensitive Device:**
This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.
Please read also the section "Special Handling and Unpacking Instructions".

**CE Conformity:**
This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section "Regulatory Compliance Statements" in this manual.

Disclaimer: We have tried to identify all situations that may pose a warning or a caution condition in this user's guide. However, Kontron does not claim to have covered all situations that might require the use of a Caution or a Warning.

# Unpacking

Follow these recommendations while unpacking:

- Remove all items from the box. If any items listed on the purchase order are missing, notify Kontron customer service immediately.
- Inspect the product for damage. If there is damage, notify Kontron customer service immediately.
- Save the box and packing material for possible future shipment.

# Powering Up the System

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

If you encounter a problem, verify the following items:

- Make sure that all connectors are properly connected.
- Verify your boot devices.
- If the system does not start properly, try booting without any other I/O peripherals attached, including AMC adapters.

Make sure your system provides the minimum DC voltages required at the board's slot, especially if DC power is carried by cables.

If you are still not able to get your board running, contact our Technical Support for assistance.

# Adapter Cables

Because adapter cables come from various manufacturers, pinouts can differ. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

# Storing Boards

Electronic boards are sensitive devices. Do not handle or store device near strong electrostatic, electromagnetic, magnetic or radioactive fields.

# Regulatory Compliance Statements

## *FCC Compliance Statement for Class A Devices*

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experience radio/TV technician for help.

**WARNING**

This is a Class A product. If not installed in a properly shielded enclosure and used in accordance with this User's Guide, this product may cause radio interference in which case users may need to take additional measures at their own expense.

## *Safety Certification*

All Kontron equipment meets or exceeds safety requirements based on the IEC/EN/UL/CSA 60950-1 family of standards entitled, "Safety of information technology equipment." All components are chosen to reduce fire hazards and provide insulation and protection where necessary. Testing and reports when required are performed under the international IECEE CB Scheme. Please consult the "Kontron Safety Conformity Policy Guide" for more information. For Canada and USA input voltage must not exceed -60Vdc for safety compliance.

## *CE Certification*

The product(s) described in this user's guide complies with all applicable European Union (CE) directives if it has a CE marking. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques. Although Kontron offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. Kontron does not offer engineering services for designing cabling systems. In addition, Kontron will not retest or recertify systems or components that have been reconfigured by customers.

# Limited Warranty

Kontron grants the original purchaser of Kontron's products a TWO YEAR LIMITED HARDWARE WARRANTY as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

Kontron warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long- term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

Kontron provides for repair or replacement of any part, assembly or sub-assembly at their own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to Kontron, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by Kontron with the repaired or replaced item.

Kontron will not accept liability for any further claims resulting directly or indirectly from any warranty claim, other than the above specified repair, replacement or refunding. In particular, all claims for damage to any system or process in which the product was employed, or any loss incurred as a result of the product not functioning at any given time, are excluded. The extent of Kontron liability to the customer shall not exceed the original purchase price of the item for which the claim exists.

Kontron issues no warranty or representation, either explicit or implicit, with respect to its products reliability, fitness, quality, marketability or ability to fulfil any particular application or purpose. As a result, the products are sold "as is," and the responsibility to ensure their suitability for any given task remains that of the purchaser. In no event will Kontron be liable for direct, indirect or consequential damages resulting from the use of our hardware or software products, or documentation, even if Kontron were advised of the possibility of such claims prior to the purchase of the product or during any period since the date of its purchase.

Please remember that no Kontron employee, dealer or agent is authorized to make any modification or addition to the above specified terms, either verbally or in any other form, written or electronically transmitted, without the company's consent.

*Chapter 1*

# Product Description

# 1. Product Description

## 1.1 Product Overview

The Kontron AT8050 AdvancedTCA processor board redefines the design possibilities with a new Intel® microarchitecture processor, which offers greater efficiency and performance.

The AT8050 is a single-socket design with two featurerich processor options: an Intel Xeon Quad-Core L5518 (45nm) processor; or an Intel Xeon Six-Core L5638 (32nm) processor (BIOS 3.00 and highier). Both feature an Integrated Memory Controller, Turbo Boost Technology, Intel® QuickPath interconnect, and Intel® Hyper-Threading Technology (SMT). The Intel L5638 offers new hardware security features including the Intel® Advanced Encryption Standard - New Instructions (Intel® AES-NI) which enables fast and secure data encryption and decryption in AES-based communications cryptographic workloads, and offers a significant increase in performance compared to the current pure-software implementations.

The overall performance of the Kontron AT8050 will handle even the most demanding storage, medical imaging, security, and communications infrastructure applications.

With the available AdvancedMC bay, wireless/telecom equipment manufacturers can add multiple functionality with an assortment of Kontron AMC modules such the Kontron AM42xx series of Intelligent packet processor AMC modules, designed with the OCTEON Plus 5650 Network Service MIPS Processor from Cavium Networks.

## 1.2 What's Included

This board is shipped with the following items:

- One AT8050 board
- One RJ45-DB9 serial adaptor (1015-9404)
- One AMC filler panel
- Cables that have been ordered

If any item is missing or damaged, contact the supplier.

# 1.3 Board Specifications

Table 1-1: Board Specifications

| Features | Description |
|---|---|
| Processors | • Intel® Xeon® Quad-Core L5518 Processor (2.13 GHz, 8MB cache) (BIOS 3.00 and highier) or Intel® Xeon® Six-Core L5638 Processor (2 GHz, 12MB cache)<br>• Passive heatsink<br>• Virtualization Technology supported |
| Chipset | • Intel 5520 I/O Hub (IOH 36D) & Intel I/O Controller Hub (ICH10R) |
| Bus Interface | • CPU QuickPath Interconnect delivering up to 5.86 GT/s /lane<br>• PCIe |
| Expansion Slot | • 1 Mid-size AdvancedMC bay<br>• x4 PCI Express<br>• 2x1000Base-BX Ports common option<br>• Dual port SAS(with RTM)/SATA<br>• 1 RS232 link to RTM |
| System Memory | • Up to 48 GB on 6 latching sockets of VLP DDR-3 1066MHz RDIMM SDRAM<br>• ECC support, support S4EC/D4ED<br>• 3 DDR-3 channels, 2 DIMM per channel |
| Flash Memory | • Two redundant 1MB BIOS (Field software upgradeable)<br>• Roll back functionality controlled by IPMC |
| Storage | • 4 ports SAS/SATA available using RTM with the LSISAS1064e<br>• USB SSD Flash (many avaialble sizes) daughter board<br>• iSCSI<br>• SATA AMC with ICH10 controller |
| I/O | • Front Panel: Serial (RJ-45), 2 i82576 Management LAN (RJ-45), 2 USB<br>• PCIe Gen2 5Gb/s in Update Channel (AMC Carrier ATCA blade)<br>• Intel i82599 10Gb/s or 1Gb/s Ethernet Controller to Fabric Interface<br>• Intel i82576 1Gb/s to the Base Interface<br>• Management LAN can be used to provide 1000Base-BX interface to AMC P0 & P1, RTM SFPs or to the Fabric Interface P0s<br>• Synchronisation Clocks Interface support |
| Board Specifications | • PICMG 3.0R3 / 3.1 option 9, option 2<br>• PICMG AMC.0R2 / AMC.1 type 4 / AMC.2 type E2 & type 4 / AMC.3<br>• PICMG HPM.1<br>• IPMI 2.0 |
| BIOS Features | • AMI BIOS<br>• Warm reset support with memory protection for post-mortem analysis<br>• Save CMOS in SEEPROM option<br>• Boot from Ethernet PXE (Base and Fabric interfaces and management Lan)<br>• Boot from Ethernet iSCSI (Base and Fabric interfaces)<br>• Boot from SAS/SATA; and boot from USB 2.0 (Floppy, CD-ROM, Hard Disk)<br>• Diskless, Keyboard less, and battery less operation extensions<br>• System, video and LAN BIOS shadowing<br>• Robust BIOS flash Update with rollover capability (HPM.1)<br>• Field updateable BIOS<br>• Advanced Configuration and Power Interface (ACPI 1.0, 2.0 & 3.0)<br>• Console redirection to serial port (VT100)with CMOS setup access, and SOL (Serial over LAN)<br>• Event (correctable/uncorrectable ECC, POST errors); log support to IPMC |

| Features | Description |
|---|---|
| IPMI Features | • Management Controller compliant IPMI v2.0 and design to meet CP-TA v1.1 compliancy.<br>• Remote control capability (power on-off /clean shutdown/warm reset/cold reset) via any IPMI channels including LAN.<br>• Full speed 115200 bps Serial Over LAN (+LAN access to BIOS menu setup) and IPMI Over LAN (IPMI v2.0) always available.<br>• Serial data caching and replay to ease software application troubleshooting and post mortem analysis.<br>• BIOS Post Code error sent to chassis manager System Event Logging.<br>• Configurable automatic “clean ACPI shutdown” policy on disk storage deactivation (AMC or RTM).<br>• Standard PCIe Hot Plug operation embedded with PICMG AMC/RTM activation.<br>• Robust IPMI firmware Update with rollover capability, without any payload impact (HPM.1).<br>• Override configuration for activation of the board/AMC/RTM without Shelf Manager Intervention. |
| Supervisory | • Supports a system management interface (KCS interrupt driven) via an IPMI V2.0 compliant controller.<br>• Standard IPMI Watchdog for all CPU running phase (BIOS execution / OS loading and running).<br>• IPMI Hardware system monitor (power/voltages), memory and all critical components temperature is monitored.<br>• Extensive sensors monitoring (around 100 IPMI sensors) and event generation base on thresholds and discrete reading. |
| OS Compatibility | • Validated with: Red Hat Enterprise Linux V.5.2, 7.1 & 7.2, WindRiver PNE Linux 2.0 |
| Power Requirements | 120 W* -38V @ -72V with 12GB of memory, no RTM & no AMC. Maximum of 225W<br>* The power consumption will vary depending on your product configuration (AMC, RTM & extra memory) |
| Environmental Temperature* | Operating: 0-55°C/32-131°F with 30CFM airflow<br>Storage and Transit: -40 to +70°C/-40 to 158°F |
| Environmental Humidity* | Operating: 15% to 90% @55°C/131°F non-condensing<br>Storage and Transit: 5% to 95% @ 40°C/104°F non-condensing |
| Environmental Altitude* | Operating: 4,000 m / 13,123 ft<br>Storage and Transit: 15,000 m / 49,212 ft |
| Environmental Shock* | Operating: 3G each axis<br>Storage and Transit: 18G each axis |
| Environmental Vibration* | Operating: 5-200Hz. 0.2G, each axis<br>Storage and Transit: 5Hz to 20Hz @ 1 m2/s3 (0.01g2 /Hz) (flat)<br>20Hz to 200Hz @ -3dB/oct (slope down) |
| Reliability | • Whole board protected by active breaker<br>• USB voltage protected by an active breakers |
| Safety / EMC | Meet or exceed:<br>• Safety: UL 60950-1; CSA C22.2 No 60950-1-03; EN 60950-1:2001; IEC60950-1<br>• EMI/EMC: FCC 47 CFR Part 15, Class A; CE Mark to EN55022/EN55024/EN300386 |
| Warranty | Two years limited warranty |

* Designed to meet or exceed

# 1.4 Compliance

This product conforms to the following specifications:

- PICMG3.0 R3.0(Advanced TCA Base Specification)
- PICMG3.1 R1.0 (Ethernet/Fiber Channel over AdvancedTCA)
- AMC.0 R2.0 (Advanced Mezzaninne Card Base Specification)
- AMC.1 R1.0 (Advanced Mezzaninne Card PCI-Express)
- AMC.2 R1.0 (Advanced Mezzaninne Card Ethernet)
- AMC.3 R1.0 (Advanced Mezzaninne CardStorage)
- ACPI rev 2.0
- HPM.1
- IPMI 2.0

# 1.5 Hot-Plug Capability

The AT8050 supports Full Hot Swap capability as per PICMG3.0R3.0 for the board itself and AMC bay. It can be removed from or installed in the system while it is on (without powering-down the system). Please refer to the PICMG3.0R3.0 specification for additional details about Hot Swap.

The AT8050 supports PCI-Express Hotplug on AMC B1. The IPMC uses the standard PCI Express Hotplug Controller on the CPU board allowing hot insertion and removal of an AMC.1 module within the OS.

The AT8050 supports also the RTM Hotplug and the RTMDISK Hotplug.

# 1.6 Interfacing with the Environment

## 1.6.1 RTM (rear transition module)

The RTM8050 is a single slot (6HP) AdvancedTCA Rear Transition Module. This module provides additional connectivity for AT8050 CPU front blade.

### *1.6.1.1 Standard Compliance*

- PICMG3.0 R3.0 - Advanced Telecommunication Computing Architecture
- SFF-8470 (T10 Technical Committee and SCSI Trade Association)

#### 1.6.1.2 Serial Port Feature

- One serial ports available on the RTM face plate through a RJ-45 connector.
- RS-232 signal levels at RTM face plate connector.
- Serial port speed capability is: 9.6kbits/s to 115.2kbits/s.

#### 1.6.1.3 Hot Swap

The RTM8050 supports hot swapping by using the switch connected to the face plate lower ejector. This switch indicates the coming hot swap action. The insertion of the RTM to a slot is always done over a non powered connector. During the extraction procedure, the management power is disabled only when the RTM8050 is removed. This procedure meets the AdvancedTCA AMC behavior.

##### 1.6.1.3.1 Inserting the RTM8050 into the slot

The presence of the RTM is indicated by one signal. The front blade IPMC recognizes the RTM insertion when the signal is low. After recognizing the RTM, the IPMC turns the blue LED ON and enables the management power to the RTM. Once the IPMB-L link is working, the IPMC accesses the MMC to retrieve FRU data. After knowing the type of RTM inserted, the IPMC negotiates with the shelf manager in order to activate the +12V payload power. After RTM local voltages have been ramped up, the RTM's MMC enables the RTM Link.

After this the front board IPMC informs the shelf manager there is a functional RTM blade present.

##### 1.6.1.3.2 Removing the RTM8050 from the slot

The RTM_EJECT signal goes HIGH by opening the RTM lower ejector handle. This indicates to the front blade IPMC that a hot swap action is going to take place. The IPMC then negotiates the removal with the System manager and if it is granted, it proceeds with the removal process.

The IPMC proceeds to the deactivation by disabling ekey governed links, the IPMC then disables the RTM Link and turns OFF the payload +12V power. When it is safe to remove the RTM blade from the slot, the IPMC turns the Blue / Hot Swap LED ON. Front Blade IPMC turns OFF the management power only when there is no RTM detected. (RTM8050 removed from the slot)

## 1.6.2 Advanced Mezzanine Card

The AT8050 has one AMC bay. Using a mezzanine allows to add storage or I/O not provided on board.

### *1.6.2.1 AMC Expansion*

The AMC slot provides an AMC.1 type 4, AMC.2 Type E2 and 4, AMC.3 Dual Port SAS. This means that the following signaling are supported:

- PCI-Express X4 on AMC ports 4-7
- PCI-Express clock on FCLKA
- Gigabit Ethernet on AMC port 0 and 1
- Telco clocks on TCLKA, B, C, D
- SAS on AMC port 2 and 3
- OEM RS232 connection on port 15
- Gigabit Ethernet on AMC port 8, 9, 10 and 11.

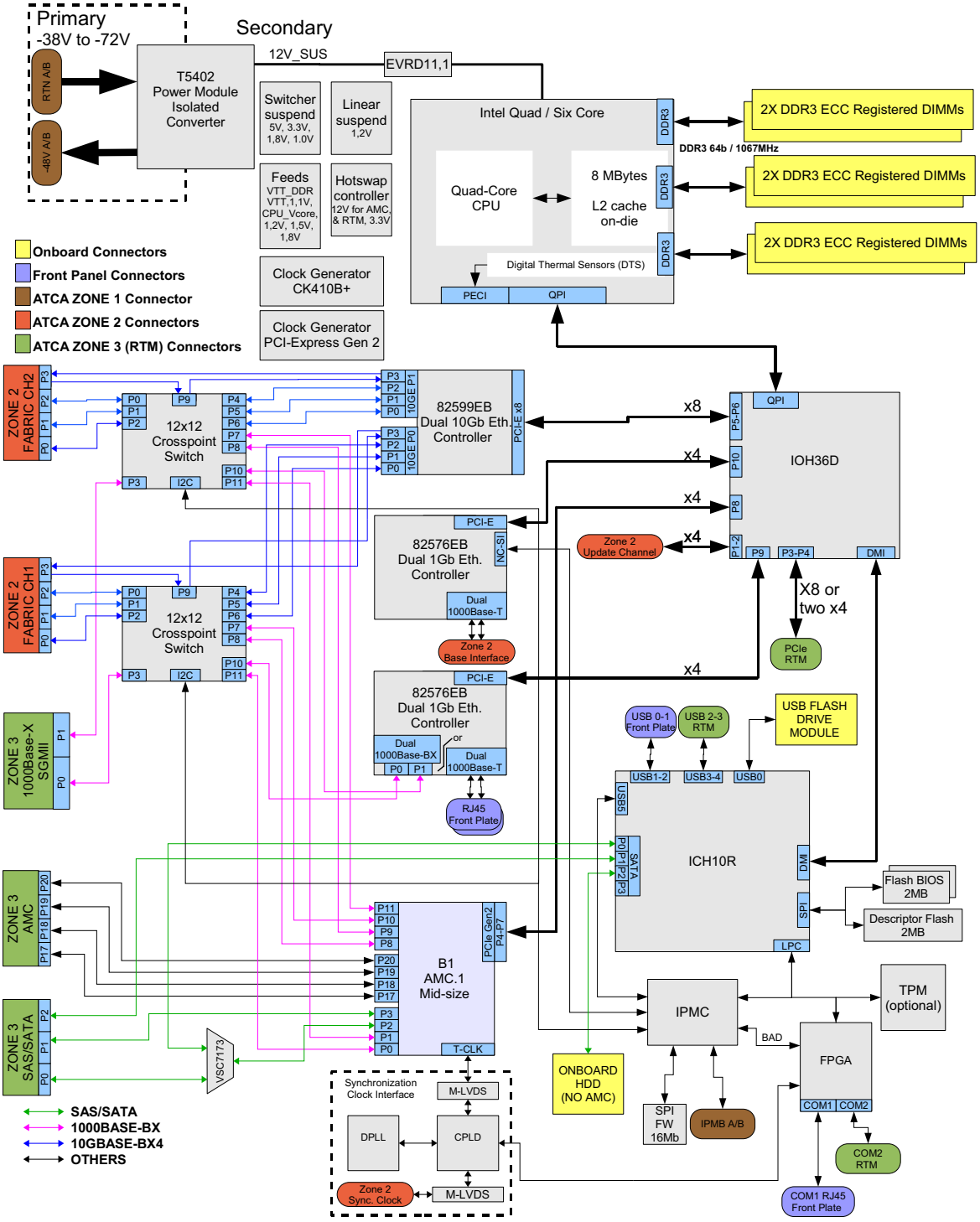
*Chapter 2*

# Board Features

# 2. Board Features

## 2.1 Block Diagram

Figure 2-1:Block Diagram



## 2.2 System Core

### 2.2.1 Processor

- Built on 45/32 nanometer process technology.
- Quad/Six core processor in 1366-land FCLGA.
- On-die, 8 MB/12MB L3 shared cache
- Streaming SIMD Extension 2, 3 and 4 (SSE2, SSE3 and SSE4)
- Integrated 3-channel DDR3 controller, DDR3-1066 memory with ECC
- Intel QuickPath interconnect links, 5.86 GT/s in each direction
- Intel 64 Architecture
- Enhanced Intel SpeedStep Technology
- Intel Virtualization Technology
- Simultaneous Multi-Threading

### 2.2.2 Intel IOH 36D

- QuickPath interconnect to the CPU
- 36 PCI Express 2.0 lanes (5.0Gb/sec/lane/direction)
- Direct Media Interface (DMI,ESI) x4 lanes for communicating with the Intel ICH10

### 2.2.3 ICH10R

- Direct Media Interface (DMI, ESI) x4 lanes for communicating with the Intel IOH
- Real Time Clock
- Serial ATA controller
- Advanced Host Controller Interface
- Intel Matrix Storage Technology
- Low Pin Count (LPC) Interface
- Serial Peripheral Interface

- DMA Controller, Timer/Counters, Interrupt Controller
- Universal Serial Bus (USB)
- GPIOs
- Enhanced Power Management
- System Management Bus 2.0 (SMBus)

## 2.3 USB 2.0 Interfaces

The board embeds a USB controller. This controller is compliant to USB 2.0. It provides two USB ports on the face plate and two on the RTM. Those ports can be used for external storage and for booting.

USB features include:

- Capability to daisy chain as many as 127 devices per interface
- Fast bi-directional
- Isochronous/asynchronous interface
- 480 Mbs transfer rate
- Standardization of peripheral interfaces into a single format
- Retro compatible with USB 1.1 devices

USB supports Plug and Play and hot-swapping operations (OS level). These features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

Table 2-1:USB Connector Pinout

| Pin | Signal |
|---|---|
| 1 | VCC |
| 2 | DATA- |
| 3 | DATA+ |
| 4 | GND |

**Signal Path:**
- 2 USB 2.0 on front panel (J10)
- 2 USB 2.0 on the RTM front panel

**BIOS Settings:**
Advanced --> USB Configuration

# 2.4 USB Flash Module

The AT8050 supports Solid State Drive. It is a NAND flash disk module with a USB 2.0 interface. The module is socketed on a 2x5 header attached to the AT8050 PCB. Here are the main features:

- Many available sizes
- Mean-Time Between Failures (MTBF) of 5 millions hours
- 5 Years Useful Life under specific conditions
- Read throughput of 28MB/second
- Write throughput of 20MB/second
- I/O Operations per second of 100 (4KB random 2 Read + 1 Write)
- 5V operating voltage
- 0 to 70 Celsius operating temperature

**Signal Path:**
USB Flash Module Connector is available on J22

**BIOS Settings:**
Advanced --> USB Configuration
Boot --> USB drives (to deactivate)

**Note:**
During the installation of an OS on a HDD, the USB Flash Module must be deactivated. If the USB Flash Module remains active, the Master Boot Record will be installed on it by default. This can not be avoided and will cause the OS to be unable to boot when booting from the HDD.

# 2.5 Serial ATA/Serial Attached SCSI

## 2.5.1 Serial Attached SCSI (LSISAS1064e is PCI-e rev 1.1)

This option is only available through a combination of the RTM8050 and AT8050, on which the controller resides. Two SAS ports are routed from the RTM8050 to the AMC Bay (more details in the AMC Mezzanine section below).

The RTM8050 features a SAS controller (the LSISAS1064e is PCI-e rev 1.1) which interfaces with the AT8050 by a dedicated PCI Express connection or through the Update Channel Interface such as the Kontron carrier AMC AT8402. If the RTM controller is used, a SAS or SATA hard drive can be located in the AT8050 AMC bay or in the RTM8050 Hard Disk tray, but thermal restrictions on the type of supported hard drives applies (standard 15mm SAS drives with 60 Celsius maximum Tcase are not supported over specified operating

temperature). The SAS controller can be on a AMC carrier blade connected to the AT8050 through x4 PCIExpress in the Update Channel Interface. See the AMC carrier blade's specification for more information about its storage capabilities and restrictions.

### 2.5.2 Serial ATA (ICH10R)

SATA ports are locally available from the AT8050.

One ICH10R SATA port is connected to the AMC Port 2 through a multiplexer.

The ICH10R SATA host controller supports independent DMA operation and supports data transfer rates of up to 3.0 Gb/s (300 MB/s). The SATA controller contains two modes of operation - a legacy mode using I/O space, and an AHCI mode using memory space. When configured in legacy mode, the SATA controller doesn't provide AHCI capabilities. The ICH10R supports the Serial ATA Specification, Revision 1.0a. The ICH10 also supports several optional sections of the Serial ATA II: Extensions to Serial ATA 1.0 Specification, Revision 1.0 (AHCI support is required for some elements).

## 2.6 Update Channel

The AT8050 update channel can be used to interface with an AMC carrier blade, such as the AT8402 Kontron AMC carrier, via x4 PCI-Express link. This feature offer additional application possibilities to the AT8050. Consult the AMC carrier blade's technical reference manual for more information about these possibilities or contact your local technical support team for further details about the update channel.

## 2.7 Real Time Clock & NVRAM

The AT8050 is a battery less board. The real time clock and non-volatile RAM integrated in the ICH are powered by the suspend power when available. A SuperCap provides sufficient power to retain the real time clock for a typical duration of 2hrs. The real time clock precision is 100ppm or better.

Although it is possible to save the CMOS setup in NVRAM (or CMOS RAM), the default configuration saves the setup in flash. So, when the AT8050 is unpowered for too long, only the time and date will be lost.

## 2.8 Redundant BIOS Flash

Two BIOS SPI flash are present on the AT8050. If for some reason a BIOS update corrupts a flash and it prevents the CPU from completing the boot sequence, the IPMC will swap the active SPI flash and force a reboot.

**Note:**
Since the CMOS setup is saved in flash, this will also restore the previous BIOS setup.


**BIOS Settings:**
Management --> System Information --> BIOS In Use
Exit --> Exit and Execute BIOS Swap

# 2.9 Ethernet Interfaces

## 2.9.1 Fabric Interface

The fabric interface can be either 10GbE or 1GbE. An E-Keying configuration is required to properly route the desired connection speed.

The AT8050 has boot from LAN capability (PXE) or iSCSI support on these ports. Enable the option from the BIOS Setup Program. Please refer to Section 5.1, AMI BIOS Set-up Program.

### *2.9.1.1 10GbE (i82599EB) connectivity :*

The AT8050 has one dual port 10GbE controller (i82599EB) connected to the Fabric Interface. This controller can also be used as a dual 1Gb.

### *2.9.1.2 1GbE (i82576EB) connectivity :*

While normally connected to the front panel, the i82576EB (1GbE) controller can be connected to the Fabric interface instead of the i82599EB(10GbE). 10GbE connectivity will no longer be available.

### *2.9.1.3 i82599EB (Fabric Interface)*

Features high performance with TCP/IP and UDP/IP checksum offloading for IPv4 and IPv6, packet filtering, and jumbo frame up to 15.5K.

See http://www.intel.com for additional details on the i82599EB.

### *2.9.1.4 i82576EB (Base Interface and Management Interface)*

Features high performance with TCP/IP and UDP/IP checksum offloading for IPv4 and IPv6, packet filtering, and jumbo frame up to 16K.

See http://www.intel.com for additional details on the i82576EB.

**Signal Path:**
The two ports are available on the Fabric Interface.

**BIOS Settings:**
Advanced --> Expansion ROM Configuration

**BIOS Settings:**
System Management --> Oem E-keying configuration --> Management LAN Setting

## 2.9.2 Base Interface

An i82576EB dual port 1Gb Ethernet controller is features on the Base Interface.

Boot from LAN capability (PXE) or iSCSI is supported on these ports. Enable the option from the BIOS Setup Program. Please refer to Section 5.1, AMI BIOS Set-up Program.

**Signal Path:**
The two ports are available on the Base Interface.

**BIOS Settings:**
Advanced --> Expansion ROM Configuration

## 2.9.3 Management Interface

The management interface is featured by the second i82576EB dual port 1Gb Ethernet controller. By means of cross-point switch, it can achieve the following connectivity:

- front panel with two 10/100/1000Base-T RJ45 interfaces
- AMC (port 0-1)
- RTM
- The Fabric Interface (disables 10GbE connectivity)

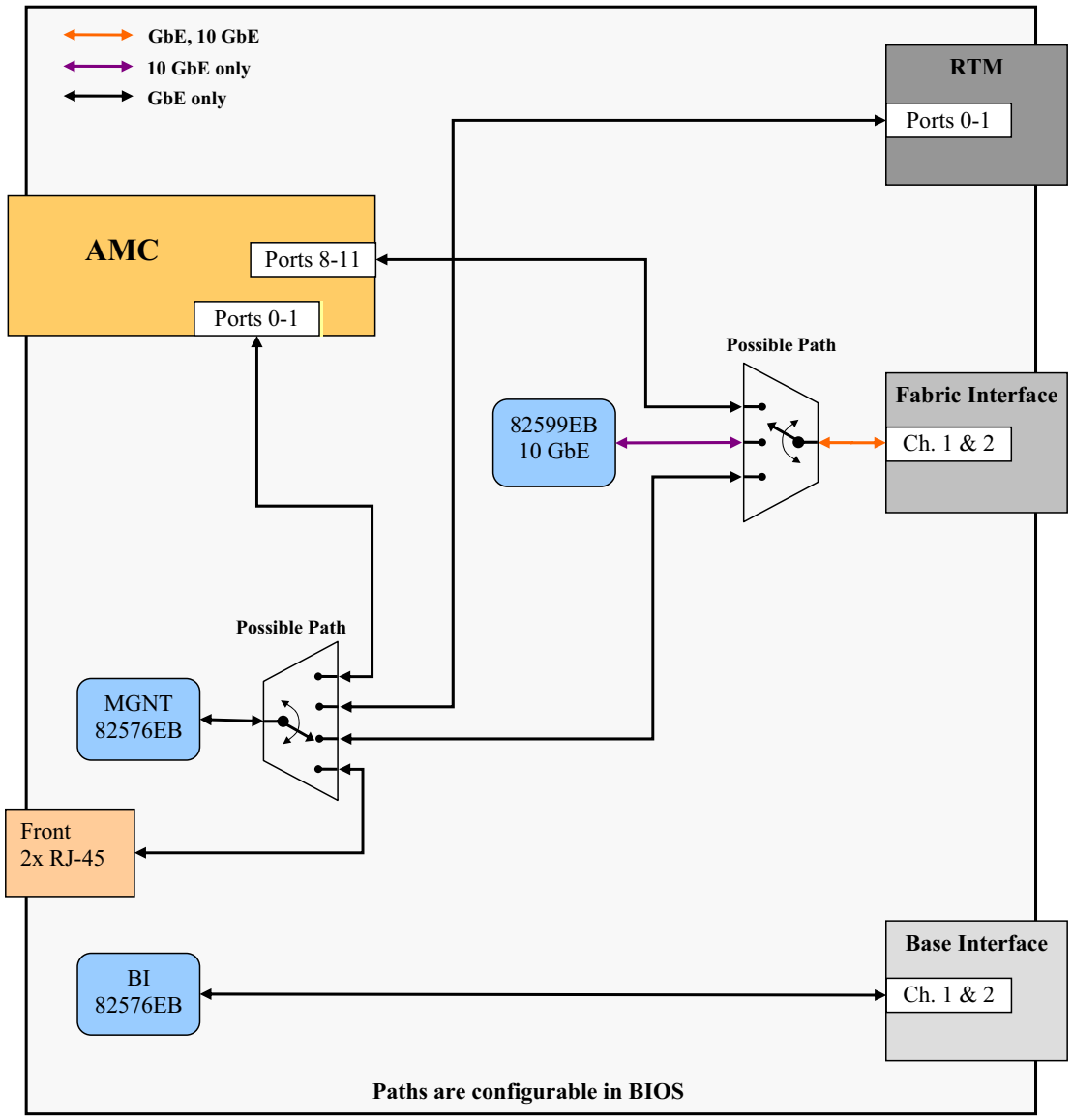
**Signal Path:**
The front panel, or on the AMC, or on the RTM.

**BIOS Settings:**
Advanced --> Expansion ROM Configuration
System Management --> OEM E-Keying Configuration

## 2.9.4 Ethernet Interfaces Configuration

Many Ethernet configurations are available with the crosspoint switch. Below is a block diagram that shows all the supported crosspoint switch configurations.

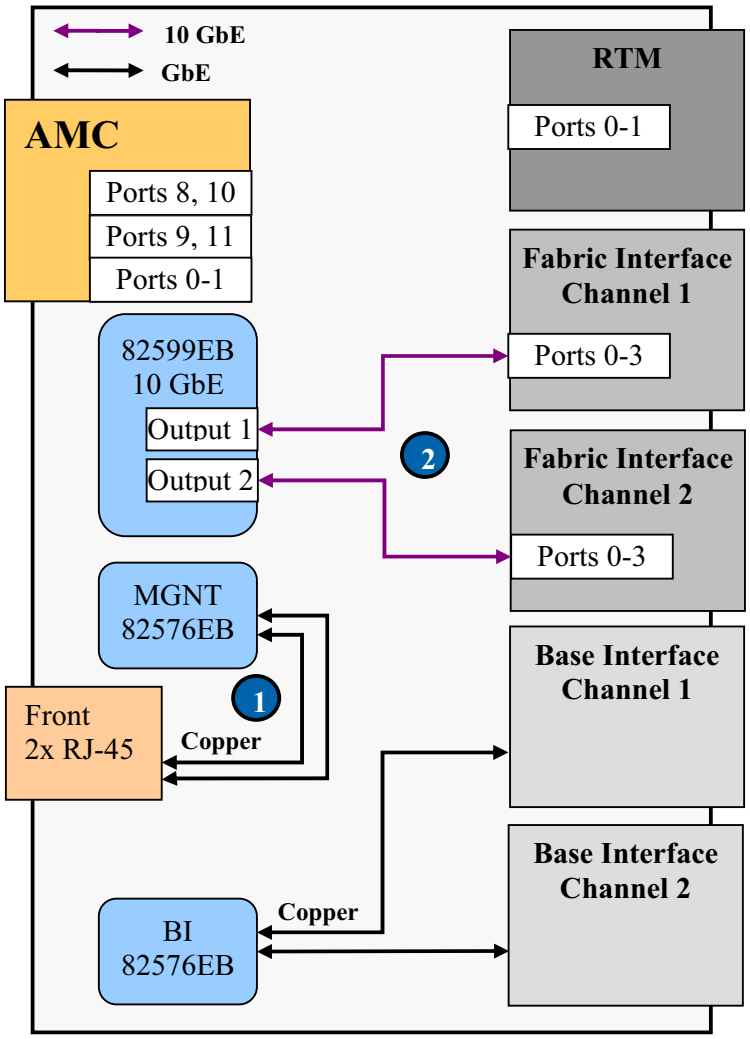
Figure 2-2:Available Ethernet Interfaces Configurations




**Note:**
- The AMC must be able to support GbE on ports 8-11
- Connection from AMC to the Fabric Interface is either PICMG3.1 option 2 (2x1GbE) or PICMG3.1 option 1 (1xGbE).

### 2.9.4.1 10GbE and Management to Front Panel Configuration

Figure 2-3: 10GbE and Management to Front Panel



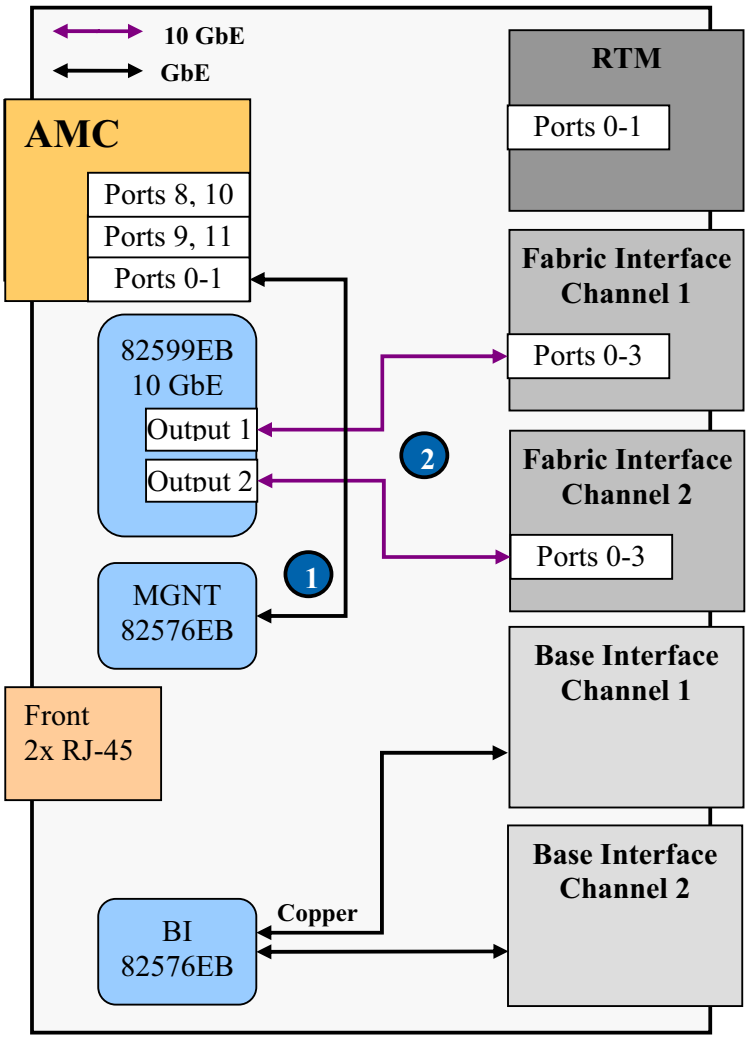

**BIOS Settings:**

1) System Management --> OEM E-Keying Configuration --> Management LAN Setting: Front Panel

2) System Management --> OEM E-Keying Configuration --> AMC P8-11 Setting: Disabled

### 2.9.4.2 10GbE and Management to AMC Configuration

Figure 2-4: 10GbE and Management to AMC



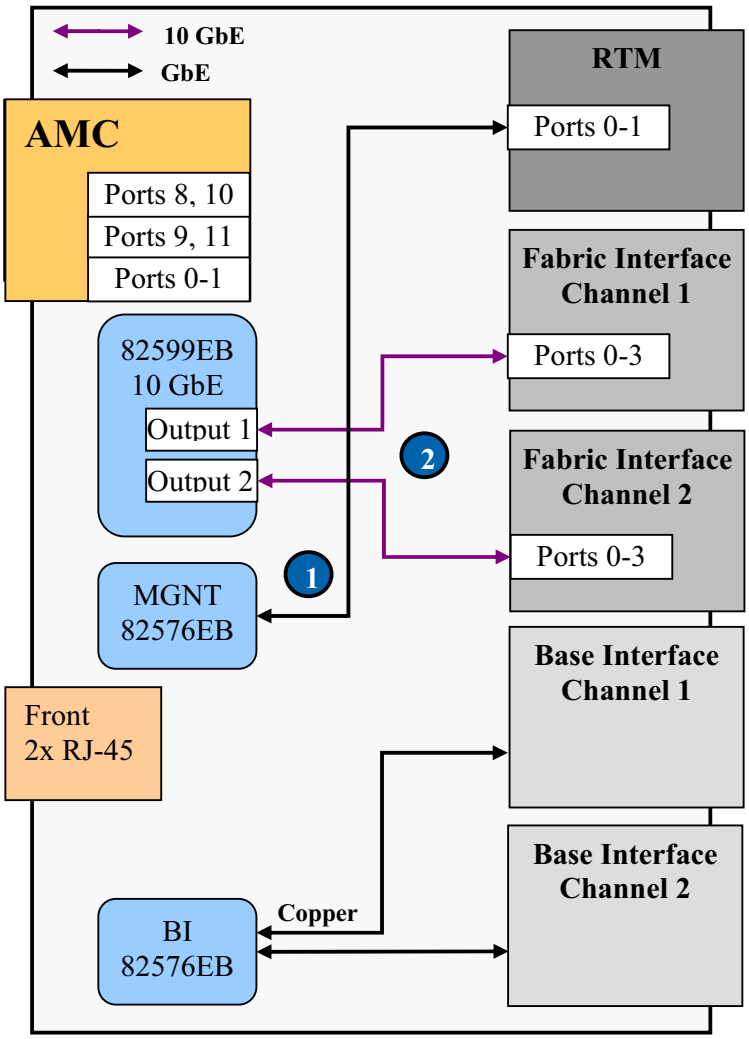

**BIOS Settings:**

1)System Management --> OEM E-Keying Configuration --> Management LAN Setting: AMC.2 Module

2)System Management --> OEM E-Keying Configuration --> AMC P8-11 Setting: Disabled

### 2.9.4.3 10GbE and Management to RTM Configuration

Figure 2-5: 10GbE and Management to RTM

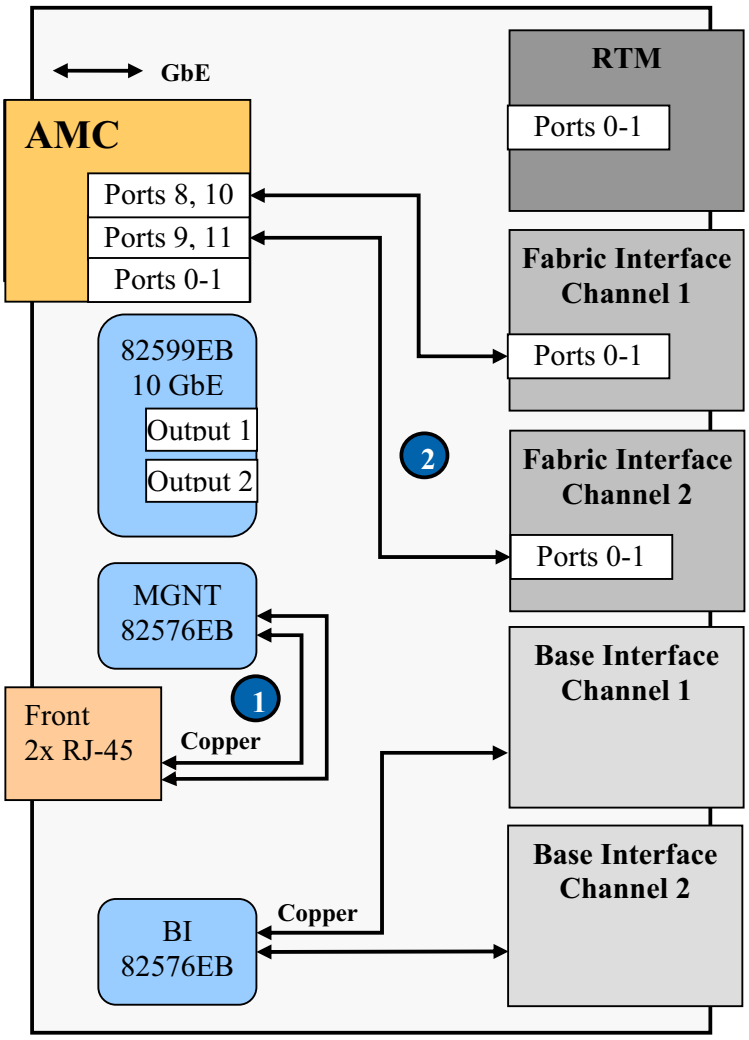



**BIOS Settings:**

1) System Management --> OEM E-Keying Configuration --> Management LAN Setting: RTM
2) System Management --> OEM E-Keying Configuration --> AMC P8-11 Setting: Disabled

### 2.9.4.4 AMC to Fabric Interface and Management to Front Panel Configuration

Figure 2-6: AMC to Fabric Interface and Management to Front Panel

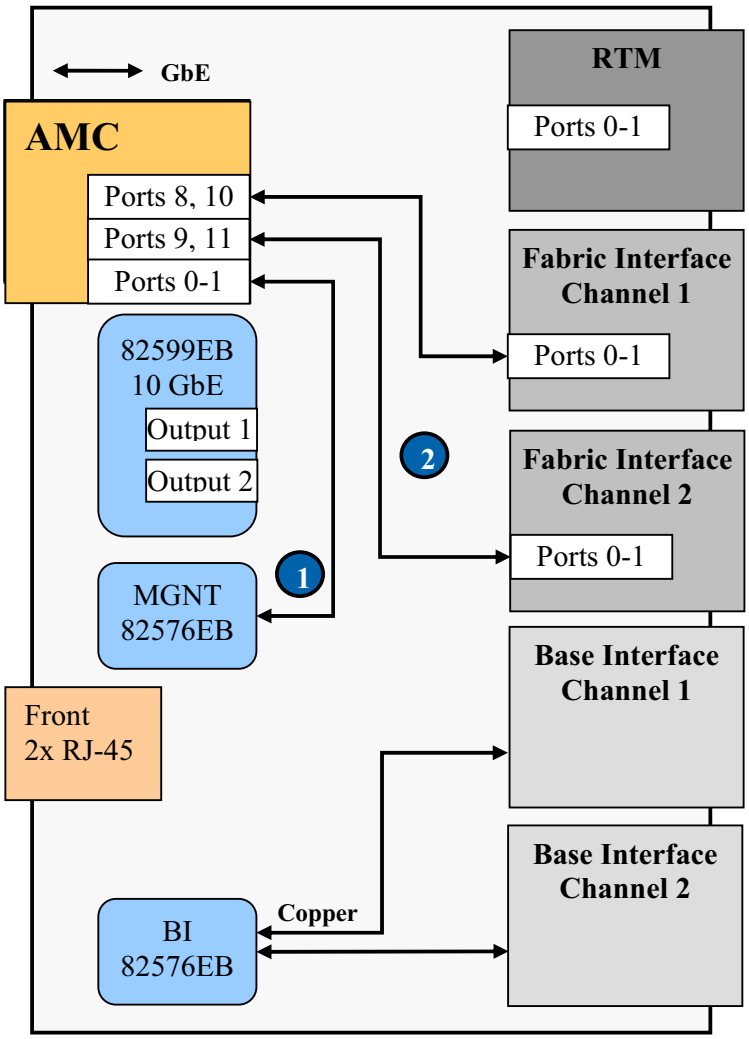



**Note:**
- The AMC must be able to support GbE on ports 8-11
- Connection from AMC to the Fabric Interface is either PICMG3.1 option 2 (2x1GbE) or PICMG3.1 option 1 (1xGbE).

**BIOS Settings:**
1) System Management --> OEM E-Keying Configuration --> Management LAN Setting: Front Panel
2) System Management --> OEM E-Keying Configuration --> AMC P8-11 Setting: Fabric Interface
In this configuration, it is not possible to boot from the Fabric Interface

### 2.9.4.5 AMC to Fabric Interface and Management to AMC Configuration

Figure 2-7: AMC to Fabric Interface and Management to AMC

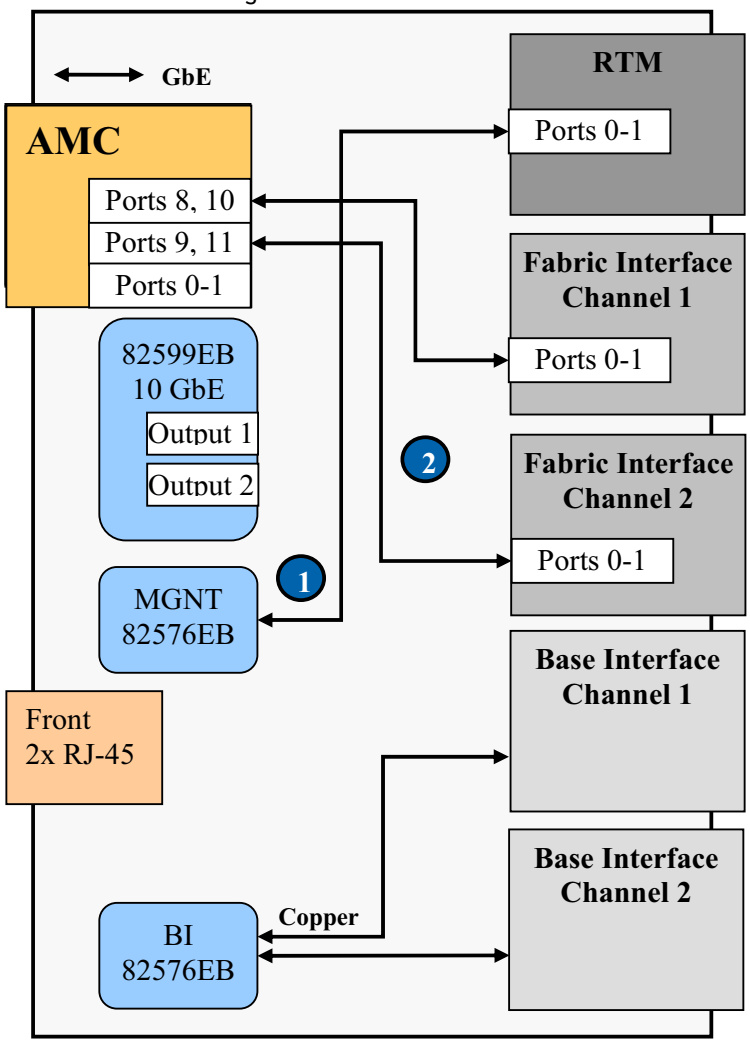



**Note:**
- The AMC must be able to support GbE on ports 8-11
- Connection from AMC to the Fabric Interface is either PICMG3.1 option 2 (2x1GbE) or PICMG3.1 option 1 (1xGbE).

**BIOS Settings:**
1) System Management --> OEM E-Keying Configuration --> Management LAN Setting: AMC.2 Module
2) System Management --> OEM E-Keying Configuration --> AMC P8-11 Setting: Fabric Interface
In this configuration, it is not possible to boot from the Fabric Interface

### 2.9.4.6 AMC to Fabric Interface and Management to RTM Configuration

Figure 2-8: AMC to Fabric Interface and Management to RTM

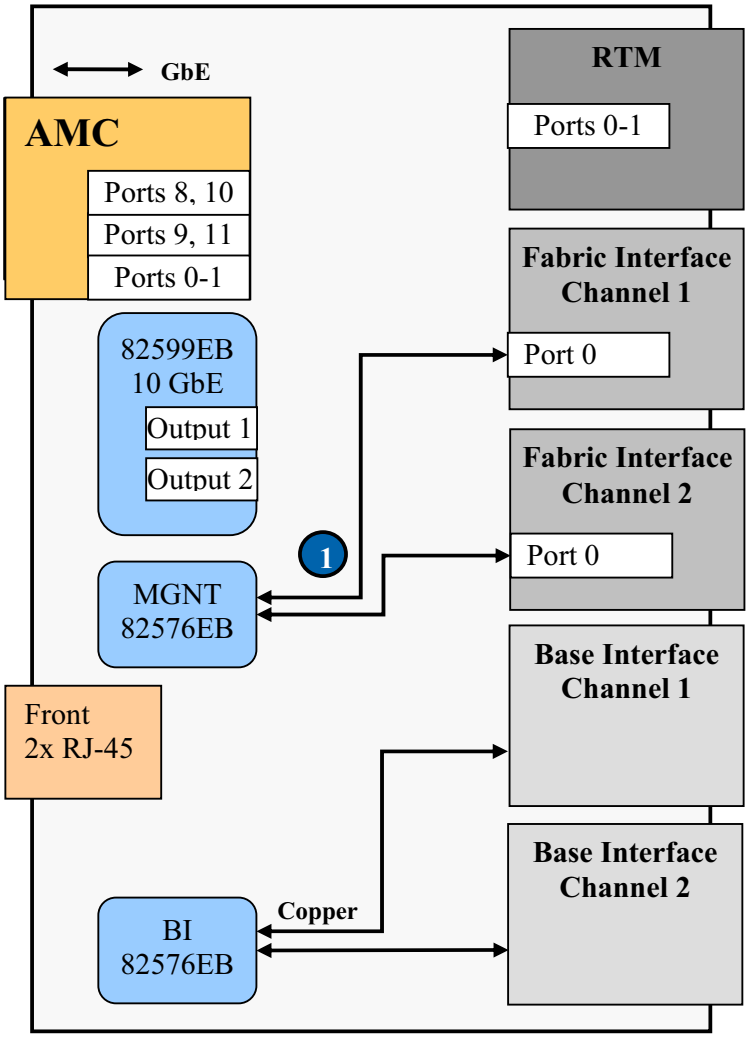



**Note:**
- The AMC must be able to support GbE on ports 8-11
- Connection from AMC to the Fabric Interface is either PICMG3.1 option 2 (2x1GbE) or PICMG3.1 option 1 (1xGbE).

**BIOS Settings:**
1) System Management --> OEM E-Keying Configuration --> Management LAN Setting: RTM
2) System Management --> OEM E-Keying Configuration --> AMC P8-11 Setting: Fabric Interface
In this configuration, it is not possible to boot from the Fabric Interface

### 2.9.4.7 Management to Fabric Interface Configuration

Figure 2-9: Management to Fabric Interface




**BIOS Settings:**

1)System Management --> OEM E-Keying Configuration --> Management LAN Setting: Fabric Interface

System Management --> OEM E-Keying Configuration --> AMC P8-11 Setting: Disabled

# 2.10 Serial Interfaces

The AT8050 uses serial interfaces to manage the CPU. Since no video interface is provided on board, the only way to get visual information on the board is the serial console. Serial ports are provided on the faceplate and on the RTM faceplate for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 9,6Kbps to 115,2Kbps.

Table 2-2:Serial Interface connector Pinout

| Pin | Signal |
|---|---|
| 1 | RTS |
| 2 | DTR |
| 3 | TX# |
| 4 | GND |
| 5 | GND |
| 6 | RX# |
| 7 | DSR |
| 8 | CTS |

**Note:**
Standard product uses a RJ-45 8 pins connector. RI (ring indicator) and DCD (data carrier detect) signals are not available.
The pinout is a custom one, not the same as RS-232D TIA/EIA-561.

**Signal Path:**
COM1 is routed to a RJ45 on the frontplate or to the IPMC for SOL.
COM2 is routed to the RTM or the AMC serial interface port is routed directly to the RTM.


**BIOS Settings:**
System Management --> Remote Access Configuration
System Management --> OEM E-Keying Configuration

# 2.11 AMC Mezzanine

The AMC slot supports AMC.1 (PCIe), AMC.2 (Gigabit Ethernet) and AMC.3 (SAS/SATA) in addition to the AMC.0 base specification. The AMC is hot swappable according to PICMG 3.0 Rev. 2.0 and supports mid-size AMC units.

One AMC site is available.  Characteristics of the AMC are as follow:

- Type B+
- Support mid-size single width mechanical format
- PCI-Express X4 (GEN2 2.5GTs or 5.0GTs) with reference clock on AMC FCLKA

- Fully compliant PCI-Express hot plug support
- Provision for telecom clocks on TCLKA, B, C, D
- SAS link from RTM connector
- Compliant to AMC.0, AMC.1, AMC.2 and AMC.3
- Serial Port (AMC port 15)
- 50W maximum power budget

As per AMC.1 R2.0, the carrier board is required to provide PCIe 100MHz reference clock to the AMC on FCLKA. However, modules are not required to use it. Kontron recommends using AMC-Express modules that use the reference clock on FCLKA. If the module makes its own reference clock, then the spread spectrum of PCI-Express clock synthetizer will be disabled by e-keying; otherwise the behavior of the PCI-Express link will be erratic.

**Note:**
All electromagnetic compatibility testing has been done with spread spectrum. Disabling the spread spectrum can complicate EMC.

The SAS interface on port 2 allows to use a SAS AMC storage mezzanine on the AT8050 and also accommodates SATA drives. AMC SATA/SAS electrical path are properly design for Hot Swap operation but special care must be taken to ensure proper un-mount sequence within the operating system.

AMC port 3 is supplied by the RTM for SAS connectivity.

The telco clock signals allow the AT8050 to provide clocks to the AMC on TCLKA and TCLKC. It also allows an AMC to retrieve a clock and to provide it to the system through TCLKB and TCLKD. For possible clock frequency and connection with the backplane, refer to section Telecom Clock Option.

**BIOS Settings:**
Advanced --> Drives Configuration
Advanced --> Expansion ROM Configuration
Advanced --> PCI Express Configuration
System Management --> OEM E-Keying Configuration

**Software Usage:**
To access the SAS BIOS press “CTRL-C” when the board boots.
You can also access the SAS controller by using the LSI Util (Linux Tool)

**Software Usage:**
AMC serial port is available on port 15.
AMC serial port GUID : 471C5D14-2AE7-42B9-A9B0-0628546B42CC

**Signal Path:**
To use the SAS interface, an RTM8050 must be installed.

**Note:**
The maximum power budget is 50W for an Advanced Mezzanane Card.

## 2.12 FPGA

The FPGA has many functions. One of them is to act as a companion chip to the IPMC. The states of all the critical signals controlled by the IPMC are memorized in the FPGA and are preserved while the IPMC firmware is being updated.

The FPGA is a RAM-based chip that is preloaded from a separate flash memory at power-up. Two such flash memory devices are provided; one that can only be programmed in factory and the other one that can be updated in the field. The factory flash is selected by inserting jumper JP1 pins 3-4. Field updates require to cycle the power of the board. The IPMI LED2 will blink if the factory flash is being used.

The FPGA update complies to PICMG HPM.1 specification and is remotely updatable via any IPMC channel.

## 2.13 Telecom Clock Option

The telecom clock option is not shown on the main block diagram. The circuit is made of MLVDS buffers, a PLD and a multi-service line card PLL. The PLD is hooked to the main FPGA with a fast serial link and from there, to the IPMC via a proprietary bus.

The PLD receives 19.44MHz clocks from the backplane (CLK2A and CLK2B) and use it as a reference to the DPLL. Anyone of the PLL clock outputs can be used to feed the AMC's TCLKA using the FPGA interface. If a backplane clock is lost, the circuit will automatically switch to the redundant clock. If all backplane clocks are lost, the PLL will switch to holdover mode until a clock reappears. If both copies of the 19.44MHz from CLK2A and CLK2B are lost, the clock control circuitry activates an alarm to the IPMC as long as the telecom sync option is enabled in the shelf.

The PLD is field upgradeable. If upgrade is necessary for this device, an appropriate procedure will be provided with the code update.

Refer to the register description in appendix and to the ZL30108 datasheet available on Zarlink's web site (www.zarlink.com)for further details on possible clock speed and configuration.

## 2.14 Redundant IPMC Firmware & BootBlock

The IPMC runs a firmware from its internal 512KB flash. The IPMC Boot Block saves the last two copies of the IPMC firmware image in dedicated SPI flash memory. The Boot Block manages the IPMC reprogramation and can rollback to the previous firmware image in the IPMC internal flash in case of update problem.

**Note:**
The IPMC has an external hardware watchdog

# 2.15 LEDs Description

The following table lists the LED on the faceplate (not counting the RJ-45 Ethernet LED).

Table 2-3:Faceplate LEDs

| LED Name | Color | Controlled by | Description |
|---|---|---|---|
| ATCA0 | Blue | IPMC | Blade Hot Swap status |
| ATCA1 | Amber/Red | IPMC | Blade OOS (out-of-service) |
| ATCA2 | Amber/Green | IPMC | Healthy status |
| ATCA3 | Amber/Green | IPMC/CPU | Application specific |
| Strip1-L0 | Amber/Green | FPGA | Base Interface Channel 1 Status |
| Strip1-L1 | Amber/Green | FPGA | Base Interface Channel 2 Status |
| Strip1-L2 | Amber/Green | FPGA | Fabric Interface Channel 1 Status |
| Strip1-L3 | Amber/Green | FPGA | Fabric Interface Channel 2 Status |
| Strip2-L0 | Amber/Green | FPGA | SAS/SATA local disks activity |
| Strip2-L1 | Amber/Green | FPGA | SAS external disk activity |
| Strip2-L2 | Amber/Green | FPGA | Alternate LAN configuration |
| Strip2-L3 | Amber/Green | FPGA | Alternate LAN configuration |

## 2.15.1 Hot Swap LED (LED0)

The Blue / Hot Swap LED indicates the hot swap status of the RTM. The LED is ON when it is safe to remove the RTM from the slot. During normal operation, this LED is OFF.

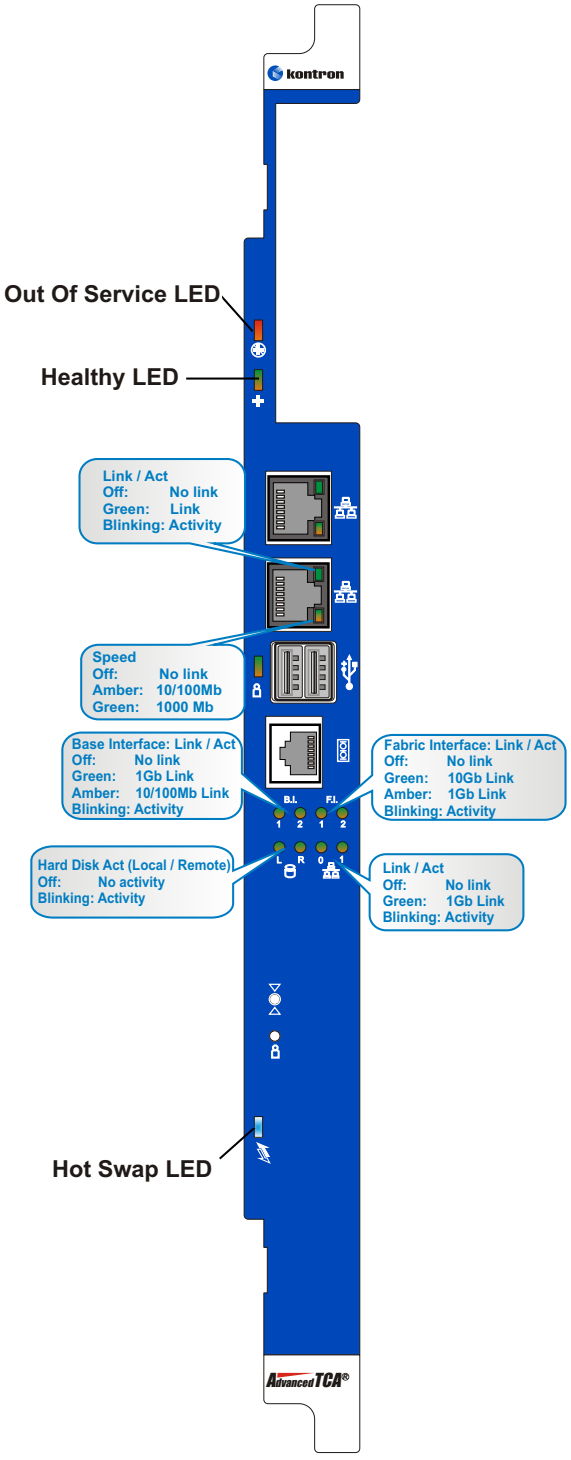
## 2.15.2 Out Of Service (LED1)

The AdvancedTCA LED1 is red or amber and indicates an Out-of-Service (OOS) condition. During normal operation, the OOS LED is OFF. This LED is ON during firmware upgrade and is user configurable if needed by a customer application.

## 2.15.3 Healthy LED (LED2)

The AdvancedTCA LED2 is green or amber and indicates a healthy condition. The healthy LED indicates if the blade is powered up and all voltages and temperatures are within specifications. During normal operation, this LED is ON (green). This LED is also ON (amber) when one of the RTM8050 voltage or temperature fails.

Figure 2-10: Faceplate LEDs




**Note:**
Disk activity is obtained directly from the ICH for SATA and from RTM-Link for SAS links of the SAS controller located on the RTM.
If the SAS controller is accessed through the Update Channel it doesn't provide any activity status.

*Chapter 3*

# Installing the Board

# 3. Installing the Board

## 3.1 Setting Jumpers

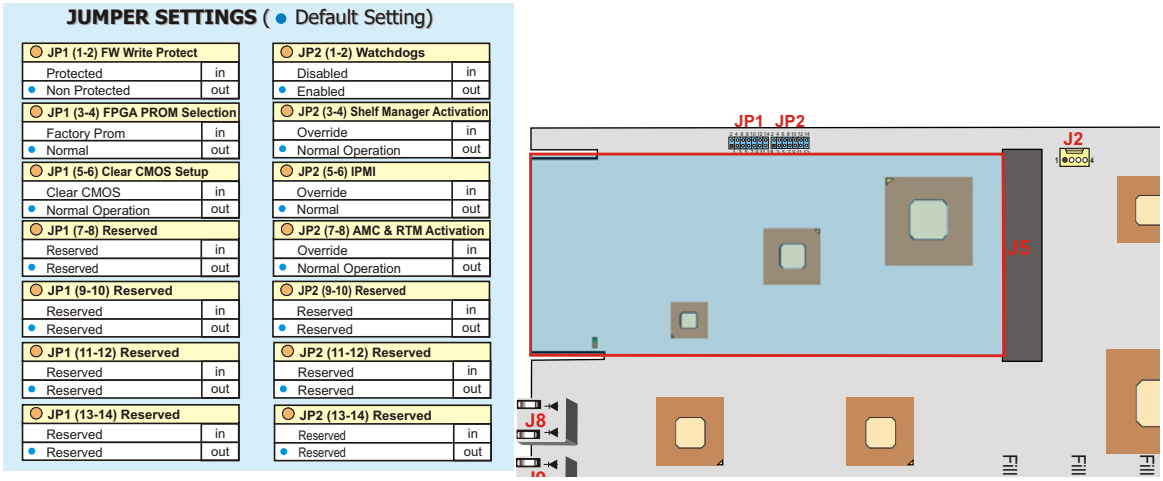
### 3.1.1 Jumper Description

Table 3-1: Jumper Description

| Name | Description | Jumper |
|---|---|---|
| FW Write Protect | When On, it enables the firmware write protect | JP1 (1-2) |
| FPGA PROM Selection | When On, it selects the factory prom | JP1 (3-4) |
| Clear CMOS Setup | When On, it clears the CMOS Setup | JP1 (5-6) |
| Reserved | Reserved | JP1 (7-8) |
| Reserved | Reserved | JP1 (9-10) |
| Reserved | Reserved | JP1 (11-12) |
| Reserved | Reserved | JP1 (13-14) |
| Watchdogs | When On, it disables the watchdogs | JP2 (1-2) |
| Shelf Manager Activation | When On, it overrides the Shelf Manager activation | JP2 (3-4) |
| IPMI | When On, it resets the IPMC | JP2 (5-6) |
| AMC & RTM Activation | When On, it overrides the AMC & RTM activation | JP2 (7-8) |
| Reserved | Reserved | JP2 (9-10) |
| Reserved | Reserved | JP2 (11-12) |
| Reserved | Reserved | JP2 (13-14) |

### 3.1.2 Setting Jumper & Locations

Figure 3-1: Jumper Settings and Locations




**Note:**
More details about the jumper settings can be found on the Quick Reference Sheet.

## 3.2 Processor

This product ships with the CPUs and a thermal solution installed. The thermal solution is custom and critical for passive cooling. Cooling performance can greatly be affected if manipulation is not handled within Kontron facility. Do not attempt any heat sink removal.

## 3.3 Memory

The AT8050 has 3 memory channels connected to the main CPU. There are 2 DIMMs per memory channels for a total of 6. The AT8050 accepts DDR3, VLP(very low-profile) (0.72 inch; 18.29mm), 1.5V typical, registered, ECC, x4 or x8 memory with up to 4 ranks per DIMM. The DDR3 memory channels run at 1066MHz with the 60W Nehalem. A minimum memory size of 2 Gbyte is supported using a single DIMM. The maximum DDR3 SDRAM size is 8GBytes per DIMM for a populated 48GBytes maximum. Memory modules shall have a validated thermal solution (heatsink) and may necessitate a certain class of chassis. It is recommended that modules have thermal sensors for accurate temperature monitoring and to throttle the memory interface in case of overheating. Memory can perform double refresh rate to get higher maximum operating temperature.

The content of the SDRAM is not affected by a warm reset.

Always populate DIMM0(J14, J16 & J18) first, then DIMM1(J13, J15 & J17) on each channel.

Only use validated memory with this product. Thermal issues or other problems may arise if you don't use recommended modules. At the time of publication of this user guide, the following memories have been qualified and approved. As the memory market is volatile, this list is subject to change, please consult your local technical support for an up to date list.

## 3.3.1 Memory List and Characteristics

Table 3-2:Approved Memory List

| Manufacturer Part Number | Description | Company |
|---|---|---|
| VL33B5663F-F8M | DIMM DDR3-1066 2GB256M*72 REG ECC 0.70" | VIRTIUM |
| SG572568FH8P6LC2 | DIMM DDR3-1066 2GB256M*72 REG ECC 0.70" | Smart modular |
| VL33B5168F-F8M | DIMM_DDR3-1066_4GB_512M*72_REG_ECC_0.70" | VIRTIUM |
| VL33B5168F-F8S | DIMM_DDR3-1066_4GB_512M*72_REG_ECC_0.70" | VIRTIUM |
| VL33B5663F-F8S-H | DIMM DDR3-1066 2GB256M*72 REG ECC 0.733" | VIRTIUM |
| VL33B5663E-F8M | DIMM DDR3-1066 2GB256M*72 REG ECC 0.733" | VIRTIUM |

Memory should have the following characteristics:

- DDR3 1066
- 1.5V typical
- Single or dual-rank modules are supported
- x4 or x8 memory with up to 4 ranks per DIMM
- Registered & ECC
- Only very low profiles (VLP) 0.72inches maximum heights (18.3mm)

**WARNING**

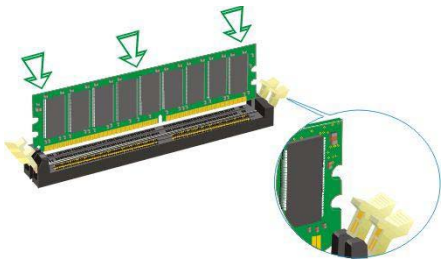
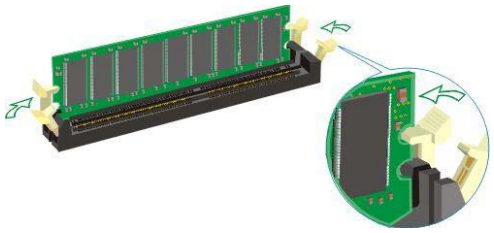
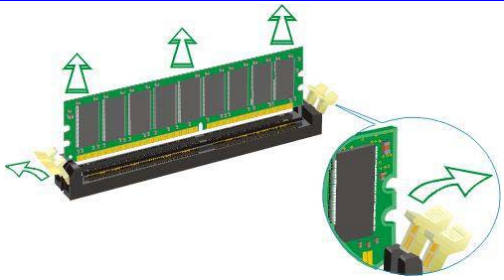
Because static electricity can cause damage to electronic devices, take the following precautions:

Keep the board in its anti-static package, until you are ready to install memory.

Wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.

Handle the board by the faceplate or its edges.

## 3.3.2 Installing Memory

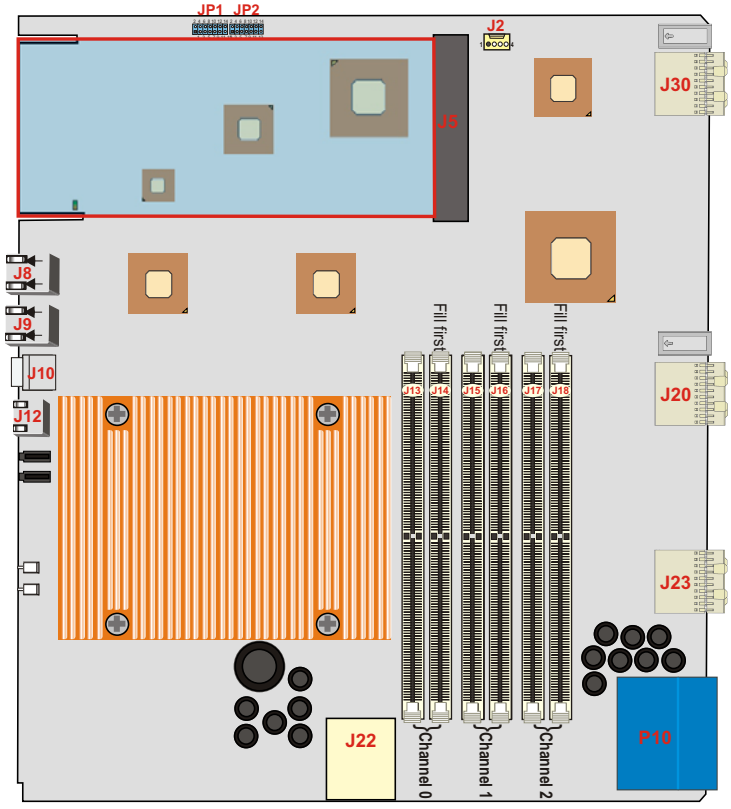
| | |
|---|---|
| On an anti-static plane, place the board so that you are facing the front plate connectors | |
| Remove the memory protection top cover. | |
| Insert the memory module into any available socket, aligning the notches on the module with the socket's key inserts. |  |
| 1- Insert the memory module in the connector using your thumbs.<br>2- Eject partially the memory module, using the connector latches while applying some pressure on the top to avoid the full removal of the modules.<br>3- Fully Reseat the modules in the connector using your thumbs.<br>4- Repeat steps 2 and 3 a second time.<br>5- Push down the memory module until the retaining clips lock on each side. |  |
| Repeat these steps to populate the other socket. | |
| To remove a memory module from a socket, push sideway the retaining clips on each side of the socket, to release the module. Pull out the memory from the socket. |  |

# 3.4 Onboard Connectors and Headers

Table 3-3:Onboard Connectors and Headers

| Description | Connector | Comments |
|---|---|---|
| Post Codes | J2 | Post Code Connector |
| AMC | J5 | AMC Connector |
| Ethernet Port 1 | J8 | RJ-45 Ethernet Connector |
| Ethernet Port 0 | J9 | RJ-45 Ethernet Connector |
| USB (2x Stacked) | J10 | Two stacked USB connectors |
| Serial Port (COM1) | J12 | RJ-45 Serial Port connector |
| DDR3 Memory Sokcets | J13-J18 | Memory Sockets |
| Synchronisation Clcocks, Update Channel | J20 | |
| USB Flash Drive | J22 | 9 pins header for the USB Flash Drive Mezzanine |
| Base Interface & Fabric Interface | J23 | |
| RTM | J30 | |
| Power & IPMB | P10 | |

Figure 3-2:Onboard Connectors and Headers Locations



# 3.5 Board Hot Swap and Installation

Because of the high-density pinout of the hard-metric connector, some precautions must be taken when connecting or disconnecting a board to/from a backplane:

1 Rail guides must be installed on the enclosure to slide the board to the backplane.

2 Do not force the board if there is mechanical resistance while inserting the board.

3 Screw the frontplate to the enclosure to firmly attach the board to its enclosure.

4 Use ejectorr handles to disconnect and extract the board from its enclosure.

**WARNING**

Always use a grounding wrist wrap before installing or removing the board from a chassis.

## 3.5.1 Installing the Board in the Chassis

To install a board in a chassis:

1 Remove the filler panel of the slot or see "Removing the Board" below.

2 Ensure the board is configured properly.

3 Carefully align the PCB edges in the bottom and top card guide.

4 Insert the board in the system until it makes contact with the backplane connectors.

5 Using both ejector handles, engage the board in the backplane connectors until both ejectors are locked.

6 Fasten screws at the top and bottom of the faceplate.

## 3.5.2 Removing the Board

If you would like to remove a card from your chassis please follow carefully these steps:

1 Unscrew the top and the bottom screw of the front panel.

2 Unlock the lower handle latch, depending on the software step; this may initiate a clean shutdown of the operating system.

3 Wait until the blue LED is fully ON, this mean that the hot swap sequence is ready for board removal.

4 Use both ejectors to disengage the board from the backplane.

5 Pull the board out of the chassis.

### 3.5.3 Installing an AMC

To install an AMC:

1 Remove the AMC filler panel.

2 Carefully engage the AMC into the card guide. Push the AMC until it fully mate with its connector. Secure the AMC handle to the locking position.

3 In normal condition, the blue LED shall turn ON as soon as the AMC is fully inserted. It will turn OFF at the end of the hot swap sequence.

### 3.5.4 Removing an AMC

To remove an AMC:

1 Pull out the handle to unlock the AMC.

2 Wait for the blue LED to turn on continuously.

3 Pull out the AMC using the handle.

### 3.5.5 Installing the RTM8050

To install the RTM:

1 Remove the filler panel of the slot.

2 Ensure the board is configured properly.

3 Carefully align the PCB edges in the bottom and top card guide.

4 Insert the board in the system until it makes contact with the CPU board.

5 Using both ejector handles, engage the board in the CPU board connectors until both ejectors are locked.

6 Fasten screws at the top and bottom of the faceplate.

### 3.5.6 Removing the RTM8050

To remove the RTM:

1 Unscrew the top and the bottom screw of the faceplate.

2 Unlock the lower handle latch.

3 Wait until the blue LED is fully ON, this mean that the hot swap sequence is ready for board removal.

4 Use both ejectors to disengage the board from the CPU board.

5 Pull the board out of the chassis.

*Chapter 4*

# Hardware Management

# 4. Hardware Management

## 4.1 Hardware Management Overview

The purpose of the hardware management system is to monitor, control, insure proper operation and provide hot swap support of ATCA Boards. The hardware management system watches over the basic health of the system, reports anomalies, and takes corrective action when needed. The hardware management system can retrieve inventory information and sensor readings as well as receive event reports and failure notifications from boards and other Intelligent FRUs. The hardware management system can also perform basic recovery operations such as power cycle or reset of managed entities.

## 4.2 Hardware Management Functionality

The Front Blade Unit supports an “intelligent” hardware management system, based on the Intelligent Platform Management Interface Specification. The hardware management system of the Front Blade Unit provides the ability to manage the power and interconnect needs of intelligent devices, to monitor events, and to log events to a central repository.

### 4.2.1 IPMC specific features

#### *4.2.1.1 IPMC - ShMC interface*

The principal management-oriented link within a Shelf is a two-way redundant implementation of the Intelligent Platform Management Bus (IPMB). IPMB is based on the inter-integrated circuit (I2C) bus and is part of the IPMI architecture. In AdvancedTCA Shelves, the main IPMB is called IPMB-0. Each entity attached to IPMB-0 does so through an IPM Controller, the distributed management controller of the IPMI architecture. Shelf Managers attach to IPMB-0 through a variant IPM Controller called the Shelf Management Controller (ShMC). AdvancedTCA IPM Controllers, besides supporting dual redundant IPMBs, also have responsibility for detecting and recovering from IPMB faults.

The reliability of the AdvancedTCA IPMB-0 is increased by using two IPMBs, with the two IPMBs referenced as IPMB-A and IPMB-B. The aggregation of the two IPMBs is IPMB-0. The IPM Controllers aggregate the information received on both IPMBs. An IPM Controller that has a message ready for transmit uses the IPMBs in a round robin fashion. An IPM Controller tries to alternate the transmission of messages between IPMB-A and IPMB-B.

If an IPM Controller is unable to transmit on the desired IPMB then it tries to send the message on the alternate IPMB. By using this approach, an IPMB can become unavailable and then available without the IPM Controller needing to take specific action.

#### 4.2.1.2 IPMC - System Manager Interface

The Section 24 of [IPMI 2.0] describes how IPMI messages can be sent to and from the IPMC encapsulated in RMCP (Remote Management Control Protocol) packets datagrams. This capability is also referred to as “IPMI over LAN” (IOL). IPMI also defines the associated LAN-specific configuration interfaces for setting things such as IP addresses other options, as well as commands for discovering IPMI-based systems. The Distributed Management Task Force (DMTF) specifies the RMCP format. This LAN communication path make the Front Blade Unit reachable to the System Manager for any management action (IPMC firmware upgrade, query of all FRU Data, CPU reset etc.) without the need to go through the ShMC.

#### 4.2.1.3 IPMC - System Event Log

The Kontron IPMC implementation includes a Local System Event Log device as specified in the Section 31 of [IPMI 2.0]. The local System Event Log is a nonvolatile repository for the front board and all managed FRU events (AMC/RTM). The local SEL provides space for up to 1023 (0x03ff) entries. However, even if blade events are logged into the local SEL, the IPMI platform event messages are still generated by the IPMC's Event Generator and sent to the centralized SEL hosted by the Shelf Manager through the IPMB-0 communication path - [PICMG 3.0] chapter 3.5; [IPMI 2.0] Section 29. Local SEL is useful for maintenance purposes and provides access to the events when the FRU is extracted from the Shelf.

### 4.2.2 Sensors

For more details about onboard sensors consult the application note: AN09003. This application note is available from the Kontron web site at: www.kontron.com

# 4.3 IPMC

## 4.3.1 Supported commands

The table below lists the IPMI commands supported by the IPMC. This table is identical as the one provided by AMC.0 and PICMG 3.0. The last column states the Kontron support for the specific command.

Table 4-1:IPM Device Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| IPM Device "Global" Commands | | | | M | M | |
| Get Device ID | 20.1 | App | 01h | M | M | Yes |
| Cold Reset | 20.2 | App | 02h | O | O | Yes |
| Warm Reset | 20.3 | App | 03h | O | O | No |
| Get Self Test Results | 20.4 | App | 04h | M | M | Yes |
| Manufacturing Test On | 20.5 | App | 05h | O | O | Yes |
| Set ACPI Power State | 20.6 | App | 06h | O | O | Yes |
| Get ACPI Power State | 20.7 | App | 07h | O | O | Yes |
| Get Device GUID | 20.8 | App | 08h | O | O | Yes |
| Broadcast "Get Device ID" | 20.9 | App | 01h | O/M | M | Yes |

Table 4-2:Watchdog Timer Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| BMC Watchdog Timer Commands | | | | M | M | |
| Reset Watchdog Timer | 27.5 | App | 22h | M | M | Yes |
| Set Watchdog Timer | 27.6 | App | 24h | M | M | Yes |
| Get Watchdog Timer | 27.7 | App | 25h | M | M | Yes |

Table 4-3:Device Messaging Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| BMC Device and Messaging Commands[5] | | | | M | O | |
| Set BMC Global Enables | 22.1 | App | 2Eh | M | O/M | Yes |
| Get BMC Global Enables | 22.2 | App | 2Fh | M | O/M | Yes |
| Clear Message Flags | 22.3 | App | 30h | M | O/M | Yes |

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| Get Message Flags | 224 | App | 31h | M | O/M | Yes |
| Enable Message Channel Receive | 22.5 | App | 32h | O | O | Yes |
| Get Message | 22.6 | App | 33h | M | O/M | Yes |
| Send Message | 22.7 | App | 34h | M | M | Yes |
| Read Event Message Buffer | 22.8 | App | 35h | O | O | Yes |
| Get BT Interface Capabilities | 22.10 | App | 36h | M | O/M | No |
| Get System GUID | 22.14 | App | 37h | O | O | Yes |
| Get Channel Authentication Capabilities | 22.13 | App | 38h | O | O | Yes |
| Get Session Challenge | 22.15 | App | 39h | O | O | Yes |
| Activate Session | 22.17 | App | 3Ah | O | O | Yes |
| Set Session Privilege Level | 22.18 | App | 3Bh | O | O | Yes |
| Close Session | 22.19 | App | 3Ch | O | O | Yes |
| Get Session Info | 22.20 | App | 3Dh | O | O | Yes |
| Get AuthCode | 22.21 | App | 3Fh | O | O | No |
| Set Channel Access | 22.22 | App | 40h | O | O | Yes |
| Get Channel Access | 22.23 | App | 41h | O | O | Yes |
| Get Channel Info | 22.24 | App | 42h | O | O | Yes |
| Set User Access | 22.26 | App | 43h | O | O | Yes |
| Get User Access | 22.27 | App | 44h | O | O | Yes |
| Set User Name | 22.28 | App | 45h | O | O | Yes |
| Get User Name | 22.29 | App | 46h | O | O | Yes |
| Set User Password | 22.30 | App | 47h | O | O | Yes |
| Activate Payload | 24.1 | App | 48h | | | Yes |
| Deactivate Payload | 24.2 | App | 49h | | | Yes |
| Get Payload Activation Status | 24.4 | App | 4Ah | | | Yes |
| Get Payload Instance Info | 24.5 | App | 4Bh | | | Yes |
| Set User Payload Access | 24.6 | App | 4Ch | | | Yes |
| Get User Payload Access | 24.7 | App | 4Dh | | | Yes |
| Get Channel Payload Support | 24.8 | App | 4Eh | | | Yes |
| Get Channel Payload Version | 24.9 | App | 4Fh | | | Yes |
| Get Channel OEM Payload Info | 24.10 | App | 50h | | | No |
| Master Write-Read | 22.11 | App | 52h | | | Yes |

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| Get Channel Cipher Suites | 22.15 | App | 54h | | | Yes |
| Suspend/Resume Payload Encryption | 24.3 | App | 55h | | | Yes |
| Set Channel Security Keys | 22.25 | App | 56h | | | Yes |
| Get System Interface Capabilities | 22.9 | App | 57h | | | Yes |

Table 4-4:Chassis Device Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| Chassis Device Commands | | | | O | O | |
| Get Chassis Capabilities | 28.1 | Chassis | 00h | M | O | Yes |
| Get Chassis Status | 28.2 | Chassis | 01h | O/M | O | Yes |
| Chassis Control | 28.3 | Chassis | 02h | O/M | O | Yes |
| Chassis Reset | 28.4 | Chassis | 03h | O | O | No |
| Chassis Identify | 28.5 | Chassis | 04h | O | O | No |
| Set Chassis Capabilities | 28.7 | Chassis | 05h | O | O | No |
| Set Power Restore Policy | 28.8 | Chassis | 06h | O | O | No |
| Get System Restart Cause | 28.11 | Chassis | 07h | O | O | No |
| Set System Boot Options | 28.12 | Chassis | 08h | | | Yes |
| Get System Boot Options | 28.13 | Chassis | 09h | | | Yes |
| Get POH Counter | 22.12 | Chassis | 0Fh | O | O | No |

Table 4-5:Event Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| Event Commands | | | | M | M | |
| Set Event Receiver | 29.1 | S/E | 01h | M | M | Yes |
| Get Event Receiver | 29.2 | S/E | 02h | M | M | Yes |
| Platform Event | 29.3 | S/E | 03h | M | M | Yes |

Table 4-6:PEF and Alerting Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| PEF and Alerting Commands | | | | O | O | |
| Get PEF Capabilities | 30.1 | S/E | 10h | M | M | No |
| Arm PEF Postpone Timer | 30.2 | S/E | 11h | M | M | No |
| Set PEF Configuration Parameters | 30.3 | S/E | 12h | M | M | No |
| Get PEF Configuration Parameters | 30.4 | S/E | 13h | M | M | No |
| Set Last Processed Event ID | 30.5 | S/E | 14h | M | M | No |
| Get Last Processed Event ID | 30.6 | S/E | 15h | M | M | No |
| Alert Immediate | 30.7 | S/E | 16h | O | O | No |
| PET Acknowledge | 30.8 | S/E | 17h | O | O | No |

Table 4-7:Sensor Device Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| Sensor Device Commands | | | | O | M | |
| Get Device SDR Info | 35.2 | S/E | 20h | O | M | Yes |
| Get Device SDR | 35.3 | S/E | 21h | O | M | Yes |
| Reserve Device SDR Repository | 35.4 | S/E | 22h | O | M | Yes |
| Get Sensor Reading Factors | 35.5 | S/E | 23h | O | M | No |
| Set Sensor Hysteresis | 35.6 | S/E | 24h | O | O | Yes |
| Get Sensor Hysteresis | 35.7 | S/E | 25h | O | O | Yes |
| Set Sensor Threshold | 35.8 | S/E | 26h | O | O | Yes |
| Get Sensor Threshold | 35.9 | S/E | 27h | O | O | Yes |
| Set Sensor Event Enable | 35.10 | S/E | 28h | O | O | Yes |
| Get Sensor Event Enable | 35.11 | S/E | 29h | O | O | Yes |
| Re-arm Sensor Events | 35.12 | S/E | 2Ah | O | O | No |
| Get Sensor Event Status | 35.13 | S/E | 2Bh | O | O | No |
| Get Sensor Reading | 35.14 | S/E | 2Dh | M | M | Yes |
| Set Sensor Type | 35.15 | S/E | 2Eh | O | O | No |
| Get Sensor Type | 35.16 | S/E | 2Fh | O | O | No |

Table 4-8:FRU Device Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| FRU Device Commands | | | | M | M | |
| Get FRU Inventory Area Info | 34.1 | Storage | 10h | M | M | Yes |
| Read FRU Data | 34.2 | Storage | 11h | M | M | Yes |
| Write FRU Data | 34.3 | Storage | 12h | M | M | Yes |

Table 4-9:SDR Device Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| SDR Device Commands | | | | M | O | |
| Get SDR Repository Info | 33.9 | Storage | 20h | M | M | No |
| Get SDR Repository Allocation Info | 33.10 | Storage | 21h | O | O | No |
| Reserve SDR Repository | 33.11 | Storage | 22h | M | M | No |
| Get SDR | 33.12 | Storage | 23h | M | M | No |
| Add SDR | 33.13 | Storage | 24h | M | O/M | No |
| Partial Add SDR | 33.14 | Storage | 25h | M | O/M | No |
| Delete SDR | 33.15 | Storage | 26h | O | O | No |
| Clear SDR Repository | 33.16 | Storage | 27h | M | O/M | No |
| Get SDR Repository Time | 33.17 | Storage | 28h | O/M | O/M | No |
| Set SDR Repository Time | 33.18 | Storage | 29h | O/M | O/M | No |
| Enter SDR Repository Update Mode | 33.19 | Storage | 2Ah | O | O | No |
| Exit SDR Repository Update Mode | 33.20 | Storage | 2Bh | M | M | No |
| Run Initialization Agent | 33.21 | Storage | 2Ch | O | O | No |

Table 4-10:SEL Device Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| SEL Device Commands | | | | M | O | |
| Get SEL Info | 31.2 | Storage | 40h | M | M | Yes |
| Get SEL Allocation Info | 31.3 | Storage | 41h | O | O | Yes |
| Reserve SEL | 31.4 | Storage | 42h | O | O | Yes |
| Get SEL Entry | 31.5 | Storage | 43h | M | M | Yes |
| Add SEL Entry | 31.6 | Storage | 44h | M | M | Yes |
| Partial Add SEL Entry | 31.7 | Storage | 45h | M | M | No |
| Delete SEL Entry | 31.8 | Storage | 46h | O | O | Yes |

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| Clear SEL | 31.9 | Storage | 47h | M | M | Yes |
| Get SEL Time | 31.10 | Storage | 48h | M | M | Yes |
| Set SEL Time | 31.11 | Storage | 49h | M | M | Yes |
| Get Auxiliary Log Status | 31.12 | Storage | 5Ah | O | O | No |
| Set Auxiliary Log Status | 31.13 | Storage | 5Bh | O | O | No |

Table 4-11:LAN Device Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| LAN Device Commands | | | | O | O | |
| Set LAN Configuration Parameters | 23.1 | Transport | 01h | O/M | O/M | Yes |
| Get LAN Configuration Parameters | 23.2 | Transport | 02h | O/M | O/M | Yes |
| Suspend BMC ARPs | 23.3 | Transport | 03h | O/M | O/M | Yes |
| Get IP/UDP/RMCP Statistics | 23.4 | Transport | 04h | O | O | Yes |

Table 4-12:Serial/Modem Device Supported Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| Serial/Modem Device Commands | | | | O | O | |
| Set Serial/Modem Configuration | 25.1 | Transport | 10h | O/M | O/M | No |
| Get Serial/Modem Configuration | 25.2 | Transport | 11h | O/M | O/M | No |
| Set Serial/Modem Mux | 25.3 | Transport | 12h | O | O | No |
| Get TAP Response Codes | 25.4 | Transport | 13h | O | O | No |
| Set PPP UDP Proxy Transmit Data | 25.5 | Transport | 14h | O | O | No |
| Get PPP UDP Proxy Transmit Data | 25.6 | Transport | 15h | O | O | No |
| Send PPP UDP Proxy Packet | 25.7 | Transport | 16h | O | O | No |
| Get PPP UDP Proxy Receive Data | 25.8 | Transport | 17h | O | O | No |

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| Serial/Modem Connection Active | 25.9 | Transport | 18h | O/M | O/M | No |
| Callback | 25.10 | Transport | 19h | O | O | No |
| Set User Callback Options | 25.11 | Transport | 1Ah | O | O | No |
| Get User Callback Options | 25.12 | Transport | 1Bh | O | O | No |

Table 4-13:SOL Commands

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| SOL Commands | | | | O | O | |
| SOL Activating | 26.1 | Transport | | 20h | | No |
| Set SOL Configuration Params | 26.2 | Transport | | 21h | | Yes |
| Get SOL Configuration Params | 26.3 | Transport | | 22h | | Yes |

Table 4-14:PICMG 3.0 Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| AdvancedTCA® | PICMG® 3.0 Table | | | | M | |
| Get PICMG Properties | 3-11 | PICMG | 00h | | M | Yes |
| Get Address Info | 3-10 | PICMG | 01h | | M | Yes |
| Get Shelf Address Info | 3-16 | PICMG | 02h | | O | Yes |
| Set Shelf Address Info | 3-17 | PICMG | 03h | | O | No |
| FRU Control | 3-27 | PICMG | 04h | | M | Yes |
| Get FRU LED Properties | 3-29 | PICMG | 05h | | M | Yes |
| Get LED Color Capabilities | 3-30 | PICMG | 06h | | M | Yes |
| Set FRU LED State | 3-31 | PICMG | 07h | | M | Yes |
| Get FRU LED State | 3-32 | PICMG | 08h | | M | Yes |
| Set IPMB State | 3-70 | PICMG | 09h | | M | Yes |
| Set FRU Activation Policy | 3-20 | PICMG | 0Ah | | M | Yes |
| Get FRU Activation Policy | 3-21 | PICMG | 0Bh | | M | Yes |
| Set FRU Activation | 3-19 | PICMG | 0Ch | | M | Yes |
| Get Device Locator Record ID | 3-39 | PICMG | 0Dh | | M | Yes |
| Set Port State | 3-59 | PICMG | 0Eh | | O/M | Yes |
| Get Port State | 3-60 | PICMG | 0Fh | | O/M | Yes |

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| Compute Power Properties | 3-82 | PICMG | 10h | | M | Yes |
| Set Power Level | 3-84 | PICMG | 11h | | M | Yes |
| Get Power Level | 3-83 | PICMG | 12h | | M | Yes |
| Renegotiate Power | 3-91 | PICMG | 13h | | O | No |
| Get Fan Speed Properties | 3-86 | PICMG | 14h | | M<br>if controls Shelf fans | No |
| Set Fan Level | 3-88 | PICMG | 15h | | O/M | No |
| Get Fan Level | 3-87 | PICMG | 16h | | O/M | No |
| Bused Resource | 3-62 | PICMG | 17h | | O/M | Yes |
| Get IPMB Link Info | 3-68 | PICMG | 18h | | O/M | Yes |
| Get Shelf Manager IPMB Address | 3-38 | PICMG | 1Bh | | M | No |
| Set Fan Policy | 3-89 | PICMG | 1Ch | | M | No |
| Get Fan Policy | 3-90 | PICMG | 1Dh | | M | No |
| FRU Control Capabilities | 3-29 | PICMG | 1Eh | | M | Yes |
| FRU Inventory Device Lock Control | 3-42 | PICMG | 1Fh | | M | No |
| FRU Inventory Device Write | 3-43 | PICMG | 20h | | M | No |
| Get Shelf Manager IP Addresses | 3-36 | PICMG | 21h | | M | No |
| Get Shelf Power Allocation | 3-85 | PICMG | 22h | | M | No |
| Get Telco Alarm Capability | 3-93 | PICMG | 29h | | O/M | No |
| Set Telco Alarm State | 3-94 | PICMG | 2Ah | | O/M | No |
| Get Telco Alarm State | 3-95 | PICMG | 2Bh | | O/M | No |
| Get Telco Alarm Location | 3-95 | PICMG | 39h | | O/M | No |
| Set FRU Extracted | 3-25 | PICMG | 3Ah | | M | No |

Table 4-15:AMC.0 Carrier Commands for IPMC

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| AMC | AMC.0 Table | | | | | |
| Set AMC Port State | Table 3-27 | PICMG | 19h | | O/M | Yes |
| Get AMC Port State | Table 3-28 | PICMG | 1Ah | | O/M | Yes |
| Set Clock State | Table 3-44 | PICMG | 2Ch | | O/M | Yes |
| Get Clock State | Table 3-45 | PICMG | 2Dh | | O/M | Yes |

Table 4-16:HPM Commands

| | IPMI Spec. section | NetFn | CMD | IPMI BMC req. | Carrier IPMC req. | Kontron support on IPMC |
|---|---|---|---|---|---|---|
| HPM | | | | | | |
| Get Target Upgrade Capabilities | | | | | | Yes |
| Get Component Properties | | | | | | Yes |
| Abort Firmware Upgrade | | | | | | Yes |
| Initiate Upgrade Action | | | | | | Yes |
| Upload Firmware Block | | | | | | Yes |
| Finish Firmware Upload | | | | | | Yes |
| Get Upgrade Status | | | | | | Yes |
| Activate Firmware | | | | | | Yes |
| Query Self-Test Results | | | | | | Yes |
| Query Rollback Status | | | | | | Yes |
| Initiate Manual Rollback | | | | | | Yes |

## 4.3.2 Sensor Data Records

Information that describes the IPMC capabilities is provided through two mechanisms: capabilities commands and Sensor Data Records (SDRs). Capabilities commands are commands within the IPMI command set that return fields providing information on other commands and functions the controller can handle.

Sensor Data Records are data records containing information about the type and number of sensors in the platform, sensor threshold support, event generation capabilities, and information on what types of readings the sensor provides. The primary purpose of Sensor Data Records is to describe the sensor configuration of the hardware management subsystem to system software.

The IPMC are required to maintain Device Sensor Data Records for the sensors and objects they manage. Access methods for the Device SDR entries are described in the [IPMI 2.0] specification, Section 35, "Sensor Device Commands."

After a FRU is inserted, the System Manager, using the Shelf Manager, may gather the various SDRs from the FRU's IPM Controller to learn the various objects and how to use them. The System Manager uses the "Sensor Device Commands" to gather this information. Thus, commands, such as "Get Device SDR Info" and "Get Device SDR," which are optional in the IPMI specification, are mandatory in AdvancedTCA systems.

Most of the current Shelf Manager implementation gathers the individual Device Sensor Data Records of each FRU into a centralized SDR Repository. This SDR Repository may exist in either the Shelf Manager or System Manager. If the Shelf Manager implements the SDR Repository on-board, it shall also respond to "SDR Repository" commands.

This duplication of SDR repository commands creates sometime some confusion among AdvancedTCA users. This is mandatory for IPMC to support the Sensor Device Commands for IPMC built-in SDR as described in the [IPMI 2.0] specification, Section 35, "Sensor Device Commands." For the ShMC, the same set of commands for the centralized SDR Repository must be supported but they are described in the [IPMI 2.0] specification, Section 33, "SDR Repository Commands."

#### 4.3.2.1 IPMC Sensors

Table 4-17: IPMC Sensors

| ID | Sensor Name | Sensor Class | Description (Sensor Type, Event trigger) |
|---|---|---|---|
| 0 | FRU0 Hot Swap | Discrete | ATCA Board FRU Hot Swap Sensor for FRU 0 (Front Board)<br>Sensor type code = F0h PICMG Hot Swap<br>Event Reading type code = 6Fh Sensor specific<br>See PICMG 3.0 R3.0 Table 3-22, "FRU Hot Swap event message" |
| 1 | FRU1 Hot Swap | Discrete | ATCA Board FRU Hot Swap Sensor for FRU 1 (AMC B1)<br>Sensor type code = F0h PICMG Hot Swap<br>Event Reading type code = 6Fh Sensor specific<br>See PICMG 3.0 R3.0 Table 3-22, "FRU Hot Swap event message" |
| 2 | FRU2 Hot Swap | Discrete | ATCA Board FRU Hot Swap Sensor for FRU 2 (RTM)<br>Sensor type code = F0h PICMG Hot Swap<br>Event Reading type code = 6Fh Sensor specific<br>See PICMG 3.0 R3.0 Table 3-22, "FRU Hot Swap event message" |
| 3 | FRU3 Hot Swap | Discrete | ATCA Board FRU Hot Swap Sensor for FRU 3 (RTM Disk)<br>Sensor type code = F0h PICMG Hot Swap<br>Event Reading type code = 6Fh Sensor specific<br>See PICMG 3.0 R3.0 Table 3-22, "FRU Hot Swap event message" |
| 4 | FRU0 Reconfig | Discrete | Sensor Population Change on Carrier<br>Sensor type = 12h System Event<br>Event Reading type code = 6Fh Sensor specific, only offset 0 is used -see AMC.0 R2.0 for event trigger<br>-see IPMI v1.5 table 36.3, Sensor type code 12h for sensor definition |
| 5 | Temp -48V A Feed | Threshold | DC Feed A Input Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 6 | Temp -48V B Feed | Threshold | DC Feed B Input Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 7 | Temp Mez 12V Out | Threshold | DC Feed 12V Out Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 8 | Temp VDDQ | Threshold | VDDQ Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 9 | Temp Vcore | Threshold | Vcore Switcher Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 10 | Temp IPMC | Threshold | H8S2472 IPM Controller Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 11 | Temp IOH | Threshold | I/O Hub (IOH) Chipset Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |

| ID | Sensor Name | Sensor Class | Description (Sensor Type, Event trigger) |
|---|---|---|---|
| 12 | Temp ICH | Threshold | I/O Controller Hub (ICH) Chipset Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 13 | Temp Mngt Lan | Threshold | Management Ethernet Controller Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 14 | Temp BI Lan | Threshold | Base Interface Ethernet Controller Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 15 | Temp FI Lan | Threshold | Fabric Interface Ethernet Controller Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 16 | Temp Bay Inlet | Threshold | AMC B1 Inlet Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 17 | Temp CPU | Threshold | CPU Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 18 | Temp DIMM#1 | Threshold | DIMM#1 Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 19 | Temp DIMM#2 | Threshold | DIMM#2 Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 20 | Temp DIMM#3 | Threshold | DIMM#3 Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 21 | Temp DIMM#4 | Threshold | DIMM#4 Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 22 | Temp DIMM#5 | Threshold | DIMM#5 Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 23 | Temp DIMM#6 | Threshold | DIMM#6 Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 24 | Temp Disk | Threshold | Disk Temperature (Degrees)<br>Sensor type = 01h temperature<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 25 | Brd Input Power | Threshold | Power consumption in watts of the complete blade (including managed FRU)<br>Sensor type = 0Bh Other Unit-Based Sensor (Watt)<br>Event Reading type code = 01h threshold base<br>see IPMI v1.5 section 29.13.3 for threshold based event |

| ID | Sensor Name | Sensor Class | Description (Sensor Type, Event trigger) |
|---|---|---|---|
| 26 | AMC Power | Threshold | FRU 1 (AMC B1) Power consumption in watts<br>Sensor type = 0Bh Other Unit-Based Sensor (Watt)<br>Event Reading type code = 01h threshold base<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 27 | RTM Power | Threshold | FRU 2 (RTM) + FRU 3 (RTM's disk) Power consumption in watts<br>Sensor type = 0Bh Other Unit-Based Sensor (Watt)<br>Event Reading type code = 01h threshold base<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 28 | Vcore Power | Threshold | Vcore Power consumption in watts<br>Sensor type = 0Bh Other Unit-Based Sensor (Watt)<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 29 | Vddq Power | Threshold | Vddq Power consumption in watts<br>Sensor type = 0Bh Other Unit-Based Sensor (Watt)<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 30 | Vcc Mez Hold-UP | Threshold | Voltage on power mezsanine Vcc Hold-UP Sensor type = 02h voltage Event Reading type code = 01h threshold based see IPMI v1.5 section 29.13.3 for threshold based event |
| 31 | Vcc +1.0V SUS | Threshold | Voltage on board 1.0V suspend (management) power supply<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 32 | Vcc +1.2V SUS | Threshold | Voltage on board 1.2V suspend (management) power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 33 | Vcc +1.8V SUS | Threshold | Voltage on board 1.8V suspend (management) power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 34 | Vcc +3.3V SUS | Threshold | Voltage on board 3.3V suspend (management) power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 35 | Vcc +5V SUS | Threshold | Voltage on board 5V suspend (management) power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 36 | Vcc +12V SUS | Threshold | Voltage on board 12V suspend (management) power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 37 | Vcc Vtt | Threshold | Voltage on board Vtt payload power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 38 | Vcc VttDdr | Threshold | Voltage on board Vtt Ddr payload power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 39 | Vcc Vcore | Threshold | Voltage on board Vcore payload power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |

| ID | Sensor Name | Sensor Class | Description (Sensor Type, Event trigger) |
|---|---|---|---|
| 40 | Vcc +1.1V | Threshold | Voltage on board 1.1V payload power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 41 | Vcc +1.2V | Threshold | Voltage on board 1.2V payload power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 42 | Vcc +1.5V | Threshold | Voltage on board 1.5V payload power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 43 | Vcc +1.8V | Threshold | Voltage on board 1.8V payload power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 44 | Vcc +3.3V | Threshold | Voltage on board 3.3V payload power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 45 | Vcc +5V | Threshold | Voltage on board 5V payload power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 46 | Vcc +2.5V REF | Threshold | Voltage on board 2.5V reference power supply (Volts)<br>Sensor type = 02h voltage<br>Event Reading type code = 01h threshold based<br>see IPMI v1.5 section 29.13.3 for threshold based event |
| 47 | Vcc +1.8V CPU | Threshold | Voltage on board 1.8V CPU power supply (Volts) Sensor type = 02h voltage Event Reading type code = 01h threshold based see IPMI v1.5 section 29.13.3 for threshold based event |
| 48 | Vcc Vddq | Threshold | Voltage on board Vddq payload power supply (Volts) Sensor type = 02h voltage Event Reading type code = 01h threshold based see IPMI v1.5 section 29.13.3 for threshold based event |
| 49 | Vcc -48V A Feed | Threshold | Voltage on -48v feed A board input power supply (Volts) Sensor type = 02h voltage Event Reading type code = 01h threshold based see IPMI v1.5 section 29.13.3 for threshold based event |
| 50 | Vcc -48V B Feed | Threshold | Voltage on -48v feed B board input power supply (Volts) Sensor type = 02h voltage Event Reading type code = 01h threshold based see IPMI v1.5 section 29.13.3 for threshold based event |
| 51 | Feed A/B Status | Discrete | Feed A/B Redundancy Status. Sensor type = 08h Power Supply<br>Event Reading type code = 0Bh Discrete (Redundancy State), only offset 0,1 are used, see IPMI v1.5 table 36.2, event reading type code 0Bh for sensor definition |
| 52 | DIMM#1 SPD Pres | Discrete | DIMM#1 Temperature Sensor Presence Sensor type = 25h Entity Presence, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition |
| 53 | DIMM#2 SPD Pres | Discrete | DIMM#2 Temperature Sensor Presence Sensor type = 25h Entity Presence, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition |
| 54 | DIMM#3 SPD Pres | Discrete | DIMM#3 Temperature Sensor Presence Sensor type = 25h Entity Presence, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition |

| ID | Sensor Name | Sensor Class | Description (Sensor Type, Event trigger) |
|---|---|---|---|
| 55 | DIMM#4 SPD Pres | Discrete | DIMM#4 Temperature Sensor Presence Sensor type = 25h Entity Presence, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition |
| 56 | DIMM#5 SPD Pres | Discrete | DIMM#5 Temperature Sensor Presence Sensor type = 25h Entity Presence, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition |
| 57 | DIMM#6 SPD Pres | Discrete | DIMM#6 Temperature Sensor Presence Sensor type = 25h Entity Presence, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 25h (Entity Presence) for sensor definition |
| 58 | Fuse-Pres A Feed | Discrete | Fuse presence and fault detection -48 V on supply A Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 08h for sensor definition |
| 59 | Fuse-Pres B Feed | Discrete | Fuse presence and fault detection -48 V on supply B Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 08h for sensor definition |
| 60 | Fuse-RTN A Feed | Discrete | Fuse presence and fault detection RTN (Return) on supply A Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 08h for sensor definition |
| 61 | Fuse-RTN B Feed | Discrete | Fuse presence and fault detection RTN (Return) on supply B Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 08h for sensor definition |
| 62 | Fuse-Earl A Feed | Discrete | Fuse presence and fault detection on Early -48V supply A Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 08h for sensor definition |
| 63 | Fuse-Earl B Feed | Discrete | Fuse presence and fault detection on Early -48V supply B Sensor type = 08h Power Supply, Event Reading type code = 6Fh Sensor specific, only offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 08h for sensor definition |
| 64 | Power State | Discrete | Board Power State Sensor type = D0h Kontron OEM Power State Sensor Event Reading type code = 6Fh Sensor specific -see OEM sensor table, Sensor type code D1h for sensor definition |
| 65 | Power Good | Discrete | Actual power good status Sensor type = 08h Power Supply Event Reading type code = 77h OEM -see OEM sensor table, Event/Reading type code 77h for sensor definition |
| 66 | Power Good Event | Discrete | Power good status event that occur since the last power on or reset. Sensor type = 08h Power Supply Event Reading type code = 77h OEM -see OEM sensor table, Event/Reading type code 77h for sensor definition |
| 67 | Board Reset | Discrete | Board reset type and sources Sensor type = CFh OEM (Kontron Reset Sensor), Event Reading type code = 03h Digital Discrete offset 0,1 are used, -see OEM sensor table, Sensor type code CFh for sensor definition |
| 68 | POST Value | Discrete | Show current postcode value. No event generated by this sensor. Sensor type = C6h OEM (Kontron POST value sensor), Event Reading type code = 6Fh Sensor specific, offset 0 to 7 and 14 are used, -see OEM sensor table, Sensor type code C6h for sensor definition |
| 69 | Boot Error | Discrete | Boot Error Sensor Type = 1Eh Boot Error<br>Reading type code = 6Fh Sensor Specific, only offset 0 is used, -see IPMI v1.5 table 36.3, Sensor type code 1Eh for sensor definition |
| 70 | POST Error | Discrete | CPU Power On Self Test Error Sensor type = 0Fh System Firmware Progress Event Reading type code = 6Fh Sensor specific, only offset 0 is used, -see IPMI v1.5 table 36.3, Sensor type code 0Fh (System Firmware Progress) for sensor definition |
| 71 | Critical Int | Discrete | Critical Interrupt Sensor type = 13h Critical Interrupt, Event Reading type code = 6Fh Critical Interrupt offset 0,4,5 are used, -see IPMI v1.5 table 36.3, Sensor type code 13h for sensor definition |

| ID | Sensor Name | Sensor Class | Description (Sensor Type, Event trigger) |
|---|---|---|---|
| 72 | Memory | Discrete | Memory Status Sensor type = 0Ch Memory Event Reading type code = 6Fh Sensor specific, offset 0,1,3,4,5 are used, -see IPMI v1.5 table 36.3, Sensor type code 0Ch for sensor definition |
| 73 | CMOS Mem Size | Discrete | POST Memory Resize, Indicates if CMOS memory size if wrong Sensor type = 0Eh, POST Memory Resize Event Reading type code = 03h Digital Discrete offset 0,1 are used, -see IPMI v1.5 table 36.3, Event/Reading type code 03h for sensor definition |
| 74 | CMOS Passwd | Discrete | CMOS Password Failure Sensor type = 06h Platform Security Violation Attempt, Event Reading type code = 6Fh Sensor Specific offset 1 and 4 are used, -see IPMI v1.5 table 36.3, Sensor type code 06h for sensor definition |
| 75 | CPU Status | Discrete | Processor Status Sensor type = 07h Processor, Event Reading type code = 6Fh Sensor Specific offset 0,1,5 are used, -see IPMI v1.5 table 36.3, Sensor type code 07h for sensor definition |
| 76 | Bios Flash 0 | Discrete | BIOS Flash 0 Status Sensor type = 1Eh Boot Error Event Reading type code = 6Fh Sensor specific, only offset 3 is used, -see IPMI v1.5 table 36.3, Sensor type code 1Eh (Boot Error) for sensor definition |
| 77 | Bios Flash 1 | Discrete | BIOS Flash 1 Status Sensor type = 1Eh Boot Error Event Reading type code = 6Fh Sensor specific, only offset 3 is used, -see IPMI v1.5 table 36.3, Sensor type code 1Eh (Boot Error) for sensor definition |
| 78 | ACPI State | Discrete | Advance Configuration and Power Interface State Sensor type = 22h System ACPI Power State Event Reading type code = 6Fh Sensor specific, offset 0,4,5,10,11,12,14 are used. -see IPMI v1.5 table 36.3, Sensor type code 22h (ACPI Power State) for sensor definition |
| 79 | IPMI Watchdog | Discrete | IPMI Watchdog (payload watchdog) Sensor type = 23h Watchdog 2, Event Reading type code = 6Fh Sensor specific, offset 0,1,2,3,8 are used, -see IPMI v1.5 table 36.3, Sensor type code 23h (Watchdog 2) for sensor definition |
| 80 | CLK3 Control | Discrete | Clock Resource Sensor Sensor type = D0h, Kontron OEM Clock Resource Control Sensor Event Reading type code = 6Fh Sensor specific, offset 0,1,2,3,8 are used, -see OEM table, Sensor type code D0h (Kontron OEM Clock Resource Control Sensor) for sensor definition |
| 81 | FW Ver Change | Discrete | Firmware Change Detection Sensor type = 2Bh Version Change Event Reading type code = 6Fh Sensor specific, -see IPMI v1.5 table 36.3, Sensor type code 2Bh (Version Change) for sensor definition |
| 82 | Health Error | Discrete | General health status, Aggregation of critical sensor. This list is flexible and could be adjust based on customer requirements. Sensor type = 24h Platform Alert, Event Reading type code = 03h Digital Discrete offset 0,1 are used, -see IPMI v1.5 table 36.3, Sensor type code 24h for sensor definition |
| 83 | IPMB0 Link State | Discrete | IPMB-0 fault detection sensor Sensor type = F1h PICMG Physical IPMB-0 Event Reading type code = 6Fh Sensor specific - See PICMG 3.0 R3.0 Table 3-69, “Physical IPMB-0 event message” |
| 84 | FRU0 IPMBL State | Discrete | IPMB-L branch from FRU0 fault detection sensor. Sensor type = C3h OEM (Kontron OEM IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, -see OEM table, Sensor type code C3h (Kontron OEM IPMB-L Link State) for sensor definition |
| 85 | FRU1 IPMBL State | Discrete | IPMB-L branch from FRU1 fault detection sensor. Sensor type = C3h OEM (Kontron OEM IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, -see OEM table, Sensor type code C3h (Kontron OEM IPMB-L Link State) for sensor definition |
| 86 | FRU2 IPMBL State | Discrete | IPMB-L branch from FRU2 fault detection sensor. Sensor type = C3h OEM (Kontron OEM IPMB-L link state), Event Reading type code = 6Fh Sensor specific, offset 2 and 3 are used, -see OEM table, Sensor type code C3h (Kontron OEM IPMB-L Link State) for sensor definition |

| ID | Sensor Name | Sensor Class | Description (Sensor Type, Event trigger) |
|---|---|---|---|
| 87 | FRU Over Icc | Discrete | FRU Over Current Sensor Sensor type = CBh OEM (Kontron OEM FRU Over Current) Event Reading type code = 03h Digital Discrete offset 0,1 are used, -see OEM table, Sensor type code CBh (Kontron OEM FRU Overcurrent) for sensor definition |
| 88 | FRU Sensor Error | Discrete | FRU Error during external FRU Sensor discovery Sensor type = CCh OEM (Kontron OEM FRU sensor error) Event Reading type code = 03h Digital Discrete offset 0,1 are used, -see OEM table, Sensor type code CCh (Kontron OEM FRU sensor error) for sensor definition |
| 89 | FRU Pwr Denied | Discrete | FRU Power Denial Detection Sensor type = CDh OEM (Kontron FRU Power denied) Event Reading type code = 03h Digital Discrete offset 0,1 are used -see OEM table, Sensor type code CDh (Kontron OEM FRU Power Denied) for sensor definition |
| 90 | FRU MngtPwr Fail | Discrete | FRU Management Power Fail Sensor type = D2h OEM (Kontron FRU Management Power Fail) Event Reading type code = 03h Digital Discrete offset 0,1 are used - see OEM table, Sensor type code D2h (Kontron OEM FRU Management Power Fail) for sensor definition |
| 91 | FRU0 Agent | Discrete | FRU Information Agent - FRU0 Data Error Detection Sensor type = C5h OEM (Kontron FRU Info Agent) Event Reading type code = 0Ah Generic Discrete, offset 6,8 are used -see OEM table, Sensor type code C5h (Kontron OEM FRU Information Agent) for sensor definition |
| 92 | FRU1 Agent | Discrete | FRU Information Agent - FRU1 Data Error Detection Sensor type = C5h OEM (Kontron FRU Info Agent), Event Reading type code = 0Ah Generic Discrete, offset 6,8 are used -see OEM table, Sensor type code C5h (Kontron OEM FRU Information Agent) for sensor definition |
| 93 | FRU2 Agent | Discrete | FRU Information Agent - FRU2 Data Error Detection Sensor type = C5h OEM (Kontron FRU Info Agent), Event Reading type code = 0Ah Generic Discrete, offset 6,8 are used -see OEM table, Sensor type code C5h (Kontron OEM FRU Information Agent) for sensor definition |
| 94 | FRU3 Agent | Discrete | FRU Information Agent - FRU3 Data Error Detection Sensor type = C5h OEM (Kontron FRU Info Agent), Event Reading type code = 0Ah Generic Discrete, offset 6,8 are used -see OEM table, Sensor type code C5h (Kontron OEM FRU Information Agent) for sensor definition |
| 95 | EventRcv ComLost | Discrete | Detects communication with the event receiver (ShMc) has been lost Sensor type = 1Bh Cable/Interconnect, Event Reading type code = 03h Digital Discrete - see IPMI v1.5 table 36.2 and table 36.3 for sensor definition |
| 96 | IPMC Reboot | Discrete | IPMC reboot detection Sensor type = 24h Platform Alert, Event Reading type code = 03h Digital Discrete offset 0,1 are used -see IPMI v1.5 table 36.3, Sensor type code 24h for sensor definition |
| 97 | IPMC FwUp | Discrete | Kontron OEM IPMC firmware upgrade Status Sensor type = C7h OEM (Kontron OEM MC firmware upgrade Status) Event Reading type code = 6Fh Sensor specific, offset 0,1 are used -see OEM table, Sensor type code C7h (Kontron OEM MC firmware upgrade Status) for sensor definition |
| 98 | IPMC Storage Err | Discrete | Management sub-system health: non volatile memory error. Sensor type = 28h Management Subsystem Health Event Reading type code = 6Fh Sensor specific, only offset 1 is used, -see IPMI v1.5 table 36.3, Sensor type code 28h for sensor definition |
| 99 | IPMC SEL State | Discrete | Specify if the status of the SEL (Cleared/Almost Full/Full) Sensor type = 10h Event Logging Disable Event Reading type code = 6Fh Sensor specific, only offset 2,4,5 are used, -see IPMI v1.5 table 36.3, Sensor type code 10h (Event Log Disable) for sensor definition |

| ID | Sensor Name | Sensor Class | Description (Sensor Type, Event trigger) |
|---|---|---|---|
| 100 | ME Availability | Discrete | Provides status on the chipset Management Engine<br>Sensor type = 28h Management Subsystem Health<br>Event Reading type code = 0Ah Generic Discrete, offset 2,6,8 are used<br>see IPMI v1.5 table 36.2, event reading type code 0Ah for sensor definition |
| 101 | Jumper Status | Discrete | Reflects on-board jumper presence<br>Sensor type = D3h OEM (Kontron OEM Jumper Status)<br>Event Reading type code = 6Fh Sensor specific, offsets 0 to 14 are used<br>-see OEM table, Sensor type code D3h (Kontron OEM Jumper Status) for sensor definition |
| 102 | IPMI Info-1 | Discrete | Internal Management Controller firmware diagnostic Sensor type = C0h Kontron OEM Firmware Info Event Reading type code = 70h Kontron OEM Internal Diagnostic -see OEM table, Sensor type code C0h (Kontron OEM Firmware Info) for sensor definition and Event/Reading type code 70h (ontron OEM Internal Diagnostic) |
| 103 | IPMI Info-2 | Discrete | Internal Management Controller firmware diagnostic Sensor type = C0h Kontron OEM Firmware Info Event Reading type code = 75h Kontron OEM Internal Diagnostic -see OEM table, Sensor type code C0h (Kontron OEM Firmware Info) for sensor definition and Event/Reading type code 70h (ontron OEM Internal Diagnostic) |

#### *4.3.2.2 IPMC Health Indicator Sensor Aggregation*

The following table shows the sensors involved in the health sensor aggregation.

Table 4-18: IPMC Health Indicator Sensor Aggregation Table

| IPMI sensor ID | Sensor Name |
|---|---|
| 5 | Temp -48V A Feed |
| 6 | Temp -48V B Feed |
| 7 | Temp Mez 12V Out |
| 8 | Temp VDDQ |
| 9 | Temp Vcore |
| 10 | Temp IPMC |
| 11 | Temp IOH |
| 12 | Temp ICH |
| 13 | Temp Mngt Lan |
| 14 | Temp BI Lan |
| 15 | Temp FI Lan |
| 16 | Temp Bay Inlet |
| 17 | Temp CPU |
| 18 | Temp DIMM#1 |
| 19 | Temp DIMM#2 |
| 20 | Temp DIMM#3 |
| 21 | Temp DIMM#4 |
| 22 | Temp DIMM#5 |
| 23 | Temp DIMM#6 |
| 25 | Brd Input Power |

| IPMI sensor ID | Sensor Name |
|---|---|
| 26 | AMC Power |
| 27 | RTM Power |
| 28 | Vcore Power |
| 29 | Vddq Power |
| 30 | Vcc Mez Hold-UP |
| 31 | Vcc +1.0V SUS |
| 32 | Vcc +1.2V SUS |
| 33 | Vcc +1.8V SUS |
| 34 | Vcc +3.3V SUS |
| 35 | Vcc +5V SUS |
| 36 | Vcc +12V SUS |
| 37 | Vcc Vtt |
| 38 | Vcc VttDdr |
| 39 | Vcc Vcore |
| 40 | Vcc +1.1V |
| 41 | Vcc +1.2V |
| 42 | Vcc +1.5V |
| 43 | Vcc +1.8V |
| 44 | Vcc +3.3V |
| 45 | Vcc +5V |
| 46 | Vcc +2.5V REF |
| 47 | Vcc +1.8V CPU |
| 48 | Vcc Vddq |
| 49 | Vcc -48V A Feed |
| 50 | Vcc -48V B Feed |
| 51 | Feed A/B Status |
| 58 | Fuse-Pres A Feed |
| 59 | Fuse-Pres B Feed |
| 60 | Fuse-RTN A Feed |
| 61 | Fuse-RTN B Feed |
| 62 | Fuse-Earl A Feed |
| 63 | Fuse-Earl B Feed |
| 65 | Power Good |
| 66 | Power Good Event |
| 67 | Board Reset |
| 70 | POST Error |
| 71 | Critical Int |
| 72 | Memory |
| 73 | CMOS Mem Size |
| 74 | CMOS Passwd |

| IPMI sensor ID | Sensor Name |
|---|---|
| 75 | CPU Status |
| 76 | Bios Flash 0 |
| 77 | Bios Flash 1 |
| 79 | IPMI Watchdog |

### 4.3.3 FRU Information

Table 4-19:Board Information Area

| Board Information Area | |
|---|---|
| Field Description | Value (hex) |
| Format Version | 0x01 |
| Board Area Length | *Calculated |
| Language code | 0x19 |
| Manufacturing Date / Time | *Based on mfg. date |
| Board Manufacturer type/length | *Calculated |
| Board Manufacturer | "KONTRON " |
| Board Name type/length | *Calculated |
| Board Name | “AT8050” |
| Board Serial Number type/length | *Calculated |
| Board Serial Number | *10 digits serial number |
| Board Part Number type/length | *Calculated |
| Board Part Number | T5007AA#_R-ZZZZZ<br>(R= Board revision)<br>(Z=config. 00000 = No DDR3, 00001 = 12GB DDR3) |
| FRU File ID type/length | *Calculated |
| FRU File ID | “FRU5007-XX"<br>(XX=template version) |
| No more fields | 0xC1 |
| Padding | None |
| Board Area Checksum | *Calculated |

Table 4-20:Product Information Area

| Product Information Area | |
|---|---|
| Field Description | Value (hex) |
| Format Version | 0x01 |
| Product Area Length | *Calculated |
| Language code | 0x19 |
| Product Manufacturer type/length | *Calculated |
| Product Manufacturer | "KONTRON " |
| Product Name type/ length | *Calculated |
| Product Name | “AT8050” |
| Product Part Number type/length | *Calculated |
| Product Part Number | T5007AA#_R-ZZZZZ<br>(R= Board revision)<br>(Z=config. 00000 = No DDR3, 00001 = 12GB DDR3) |
| Product Version type/ length | *Calculated |
| Product Version | R (R=revision) |
| Product Serial Number type/length | *Calculated |
| Product Serial Number | XXXXXXXXX |
| Product Part Number type/length | *Calculated |
| Asset Tag type/length | 0xCF |
| Asset Tag | "_____" |
| FRU File ID type/length | *Calculated |
| FRU File ID | “FRU5007-XX"<br>(XX=template version) |
| No more fields | 0xC1 |
| Padding | None |
| Board Area Checksum | *Calculated |

* Variable X, may change on revisions.

#### 4.3.3.1 ATCA Board E-Keying Information

The board e-keying information contains PICMG 3.0 R3.0 defined channel and link descriptors required for matchmaking computation by the ShMC.

The following table gives the E-Keying capabilities of the board, as they appear in the FRU data.

Table 4-21: E-Keying capabilities of the board

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record Format Version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Record Type ID | C0h |
| Record format version | 02h |
| Manufacturer ID | 00315Ah (PICMG Record ID) |
| PICMG Record ID | 14h (Board Point-To-Point Connectivity Record) |
| Record Format Version | 00h |
| OEM GUID Count | 01h |
| OEM GUID [F0] | OEM PCIe x4 + CLK Update Channel |
| Link Descriptor | 00001101h |
| Link Grouping ID (Bits 31-24) | 0h : Single-Channel link |
| Link Type Extension (Bits 23-20) | 0h : None |
| Link Type (Bits 19-12) | 01h : PICMG 3.0 Base Interface 10/100/1000 BASE-T |
| Link Designator (Bits 11-0) | 101h : Base Interface, Channel 1, Port 0 |
| Link Descriptor | 00001102h |
| Link Grouping ID (Bits 31-24) | 0h : Single-Channel link |
| Link Type Extension (Bits 23-20) | 0h : None |
| Link Type (Bits 19-12) | 01h : PICMG 3.0 Base Interface 10/100/1000 BASE-T |
| Link Designator (Bits 11-0) | 102h : Base Interface, Channel 2, Port 0 |
| Link Descriptor | 00102F41h |
| Link Grouping ID (Bits 31-24) | 0h : Single-Channel link |
| Link Type Extension (Bits 23-20) | 1h : Fixed 10GBASE-BX4 [XAUI] |
| Link Type (Bits 19-12) | 02h : PICMG 3.1 Ethernet Fabric Interface |
| Link Designator (Bits 11-0) | F41h : Fabric Interface, Channel 1, Port 0, 1, 2, 3 |
| Link Descriptor | 00002341h |
| Link Grouping ID (Bits 31-24) | 0h : Single-Channel link |
| Link Type Extension (Bits 23-20) | 0h : Fixed 1000Base-BX |
| Link Type (Bits 19-12) | 02h : PICMG 3.1 Ethernet Fabric Interface |
| Link Designator (Bits 11-0) | 341h : Fabric Interface, Channel 1, Port 0,1 |
| Link Descriptor | 00002141h |
| Link Grouping ID (Bits 31-24) | 0h : Single-Channel link |
| Link Type Extension (Bits 23-20) | 0h : Fixed 1000Base-BX |
| Link Type (Bits 19-12) | 02h : PICMG 3.1 Ethernet Fabric Interface |
| Link Designator (Bits 11-0) | 141h : Fabric Interface, Channel 1, Port 0 |
| Link Descriptor | 00102F42h |
| Link Grouping ID (Bits 31-24) | 0h : Single-Channel link |
| Link Type Extension (Bits 23-20) | 1h : Fixed 10GBASE-BX4 [XAUI] |

| Field | Value |
|---|---|
| Link Type (Bits 19-12) | 02h : PICMG 3.1 Ethernet Fabric Interface |
| Link Designator (Bits 11-0) | F42h : Fabric Interface, Channel 2, Port 0, 1, 2, 3 |
| Link Descriptor | 00002342h |
| Link Grouping ID (Bits 31-24) | 0h : Single-Channel link |
| Link Type Extension (Bits 23-20) | 0h : Fixed 1000Base-BX |
| Link Type (Bits 19-12) | 02h : PICMG 3.1 Ethernet Fabric Interface |
| Link Designator (Bits 11-0) | 342h : Fabric Interface, Channel 2, Port 0,1 |
| Link Descriptor | 00002142h |
| Link Grouping ID (Bits 31-24) | 0h : Single-Channel link |
| Link Type Extension (Bits 23-20) | 0h : Fixed 1000Base-BX |
| Link Type (Bits 19-12) | 02h : PICMG 3.1 Ethernet Fabric Interface |
| Link Designator (Bits 11-0) | 142h : Fabric Interface, Channel 2, Port 0 |
| Link Descriptor | 000F0181h |
| Link Grouping ID (Bits 31-24) | 0h : Single-Channel link |
| Link Type Extension (Bits 23-20) | 0h : None |
| Link Type (Bits 19-12) | F0h : OEM PCIe x4 + CLK  Update Channel |
| Link Designator (Bits 11-0) | 181h : Update Channel Interface 1, Port 0 ( all ten pairs ) |

#### *4.3.3.2 AMC Carrier Activation and Carrier Information Table*

The AMC slot power budget is included in the following table.

Table 4-22:AMC Carrier Activation and Carrier Information Table

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Manufacturer ID | 00315Ah |
| PICMG Record ID | 17h<br>(Carrier Activation And Current Management) |
| Record Format Version | 00h |
| Maximum Internal Current | 29h (4.1 A @ 12 V ) => 49.2 Watts |
| Allowance for Module Activation Readiness | 002h |
| Module Activation and Power Descriptor Count | 01h |
| Carrier Activation and Power Descriptors. | 7Ah, 22h, FFh |
| Local IPMB Address | 7Ah |
| Maximum Module Current | 29h (4.1 A @ 12 V ) => 49.2 Watts |
| Reserved | FFh |

The Carrier Information Table gives the Carrier AMC.0 specification version and the Carrier's AMC sites list.

Table 4-23: Carrier AMC.0

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Manufacturer ID | 00315Ah (PICMG Record ID) |
| PICMG Record ID | 0x1A (Carrier Information Table) |
| Record Format Version | 00h |
| AMC.0 Extension Version | 02h (AMC.0 R2.0) |
| Carrier Site Number Count | 01h |
| Carrier Site Number | 05h |

#### *4.3.3.3 AMC Carrier Point-To-Point Connectivity Information*

As defined in the AMC.0 specification, On-Carrier Device Ids are arbitrarily assigned to devices that implement E-Key governed links. Remote resources, such as AMCs, use predefined Ids corresponding to their Site Numbers. The following table gives the mapping between the devices and the corresponding Ids.

Table 4-24:Mapping between the devices and the corresponding Ids

| Devices | Resource Id |
|---|---|
| Intel IOH PCI-Express Root Complex Port 3 | 00h |
| Intel IOH PCI-Express Root Complex Port 8 | 01h |
| Intel ICH10 SATA Controller | 02h |
| Intel 82576EB NC (front/rear) | 03h |
| Onboard Fabric Channel 1 Switch | 04h |
| Onboard Fabric Channel 2 Switch | 05h |
| FPGA Based UART | 06h |
| RTM (On-Carrier Virtual Device for RTM) | 07h |
| AMC B1 (AMC Site Number 5) | 85h |

The Carrier Point-To-Point Connectivity record gives the list of available point-to-point link paths between On-Carrier Devices and AMC Sites. The record's content is given by the following table.

Table 4-25:Record's content

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |

| Field | Value |
|---|---|
| Manufacturer ID | 00315Ah<br>(PICMG Record ID) |
| PICMG Record ID | 18h<br>(Carrier Point-To-Point Connectivity Record) |
| Record Format Version | 00h |
| Point-To-Point AMC Resource Descriptor | |
| Local Resource ID | 85h ->AMC Site 5 (AMC B1) |
| Point-To-Point Port Count | Dh |
| Point-to-Point Port Descriptor | 000003h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 0h |
| Remote Port (Bit 12-8) | 0h |
| Remote Resource ID (Bits 7-0) | 03h ->Carrier, Device 3<br>( Intel 82576EB NC (front/rear) ) |
| Point-to-Point Port Descriptor | 002103h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 1h |
| Remote Port (Bit 12-8) | 1h |
| Remote Resource ID (Bits 7-0) | 03h ->Carrier, Device 3<br>( Intel 82576EB NC (front/rear) ) |
| Point-to-Point Port Descriptor | 004002h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 2h |
| Remote Port (Bit 12-8) | 0h |
| Remote Resource ID (Bits 7-0) | 02h -> Intel ICH Sata Controller |
| Point-to-Point Port Descriptor | 004207h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 2h |
| Remote Port (Bit 12-8) | 2h |
| Remote Resource ID (Bits 7-0) | 07h -> Virtual On-Carrier Device 7 (RTM) |
| Point-to-Point Port Descriptor | 006307h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 3h |
| Remote Port (Bit 12-8) | 3h |
| Remote Resource ID (Bits 7-0) | 07h -> Virtual On-Carrier Device 7 (RTM) |
| Point-to-Point Port Descriptor | 008001h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 4h |
| Remote Port (Bit 12-8) | 0h |
| Remote Resource ID (Bits 7-0) | 01h ->Carrier, Device 1<br>(Intel IOH PCI-Express Root Complex Port 7) |
| Point-to-Point Port Descriptor | 00a101h |
| Reserved (Bits 23-18) | 0h |

| Field | Value |
|---|---|
| Local Port (Bits 13-17) | 5h |
| Remote Port (Bit 12-8) | 1h |
| Remote Resource ID (Bits 7-0) | 01h ->Carrier, Device 1<br>(Intel IOH PCI-Express Root Complex Port 7) |
| Point-to-Point Port Descriptor | 00c201h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 6h |
| Remote Port (Bit 12-8) | 2h |
| Remote Resource ID (Bits 7-0) | 01h ->Carrier, Device 1<br>(Intel IOH PCI-Express Root Complex Port 7) |
| Point-to-Point Port Descriptor | 00e301h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 7h |
| Remote Port (Bit 12-8) | 3h |
| Remote Resource ID (Bits 7-0) | 01h ->Carrier, Device 1<br>(Intel IOH PCI-Express Root Complex Port 7) |
| Point-to-Point Port Descriptor | 010804h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 8h |
| Remote Port (Bit 12-8) | 8h |
| Remote Resource ID (Bits 7-0) | 04h ->Carrier, Device 4<br>(Fabric Channel 1 via OnBoard Switch) |
| Point-to-Point Port Descriptor | 012805h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 9h |
| Remote Port (Bit 12-8) | 8h |
| Remote Resource ID (Bits 7-0) | 05h ->Carrier, Device 5<br>(Fabric Channel 2 via OnBoard Switch) |
| Point-to-Point Port Descriptor | 014704h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | Ah |
| Remote Port (Bit 12-8) | 0h |
| Remote Resource ID (Bits 7-0) | 04h ->Carrier, Device 4<br>(Fabric Channel 1 via OnBoard Switch) |
| Point-to-Point Port Descriptor | 016705h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | Bh |
| Remote Port (Bit 12-8) | 7h |
| Remote Resource ID (Bits 7-0) | 05h ->Carrier, Device 5<br>(Fabric Channel 2 via OnBoard Switch) |
| Point-to-Point Port Descriptor | 01ed07h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | Fh |
| Remote Port (Bit 12-8) | Dh |

| Field | Value |
|---|---|
| Remote Resource ID (Bits 7-0) | 07h -> Virtual On-Carrier Device 7 (RTM) |
| | |
| Point-To-Point AMC Resource Descriptor | |
| Local Resource ID | 07h -> Virtual On-Carrier Device 7 (RTM) |
| Point-To-Point Port Count | Bh |
| Point-to-Point Port Descriptor | 000003h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 0h |
| Remote Port (Bit 12-8) | 0h |
| Remote Resource ID (Bits 7-0) | 03h ->Carrier, Device 3<br>( Intel 82576EB NC (front/rear) ) |
| Point-to-Point Port Descriptor | 002103h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 1h |
| Remote Port (Bit 12-8) | 1h |
| Remote Resource ID (Bits 7-0) | 03h ->Carrier, Device 3<br>( Intel 82576EB NC (front/rear) ) |
| Point-to-Point Port Descriptor | 004285h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 2h |
| Remote Port (Bit 12-8) | 2h |
| Remote Resource ID (Bits 7-0) | 85h ->AMC Site 5<br>(AMC B1) |
| Point-to-Point Port Descriptor | 006385h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 3h |
| Remote Port (Bit 12-8) | 3h |
| Remote Resource ID (Bits 7-0) | 85h ->AMC Site 5<br>(AMC B1) |
| Point-to-Point Port Descriptor | 008000h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 4h |
| Remote Port (Bit 12-8) | 0h |
| Remote Resource ID (Bits 7-0) | 00h ->Carrier, Device 0<br>(Intel IOH PCI-Express Root Complex Port 3) |
| Point-to-Point Port Descriptor | 00a100h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 5h |
| Remote Port (Bit 12-8) | 1h |
| Remote Resource ID (Bits 7-0) | 00h ->Carrier, Device 0<br>(Intel IOH PCI-Express Root Complex Port 3) |
| Point-to-Point Port Descriptor | 00c200h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 6h |

| Field | Value |
|---|---|
| Remote Port (Bit 12-8) | 2h |
| Remote Resource ID (Bits 7-0) | 00h ->Carrier, Device 0<br>(Intel IOH PCI-Express Root Complex Port 3) |
| Point-to-Point Port Descriptor | 00e300h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | 7h |
| Remote Port (Bit 12-8) | 3h |
| Remote Resource ID (Bits 7-0) | 00h ->Carrier, Device 0<br>(Intel IOH PCI-Express Root Complex Port 3) |
| Point-to-Point Port Descriptor | 018102h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | Ch |
| Remote Port (Bit 12-8) | 1h |
| Remote Resource ID (Bits 7-0) | 02h ->Carrier, Device 2<br>(Intel ICH SATA Controller) |
| Point-to-Point Port Descriptor | 01a006h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | Dh |
| Remote Port (Bit 12-8) | 0h |
| Remote Resource ID (Bits 7-0) | 06h ->Carrier, Device 6<br>(FPGA Based UART) |
| Point-to-Point Port Descriptor | 01af85h |
| Reserved (Bits 23-18) | 0h |
| Local Port (Bits 13-17) | Dh |
| Remote Port (Bit 12-8) | Fh |
| Remote Resource ID (Bits 7-0) | 85h ->AMC Site 5 (AMC B1) |

#### 4.3.3.4 AMC Point-To-Point Connectivity Information

The following table gives AMC connectivity details for "Intel IOH PCI-Express Root Complex Port 3" (On-Carrier Device 0).

Table 4-26:AMC connectivity details for "Intel IOH PCI-Express Root Complex Port 3"

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Manufacturer ID | 00315Ah |
| PICMG Record ID | 19h (AMC Point-To-Point Connectivity Record) |
| Record Format Version | 00h |

| Field | Value |
|---|---|
| OEM GUID Count | 0h |
| Record Type/Connected-device ID | 00h(Carrier,Device 0->Intel IOH PCI-Express Root Complex Port 3) |
| AMC Channel Descriptor Count | 01h |
| AMC Channel Descriptor | F18820h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 03h |
| Lane 2 Port Number (Bits 14-10) | 02h |
| Lane 1 Port Number (Bits 9-5) | 01h |
| Lane 0 Port Number (Bits 4-0) | 00h |
| AMC Link Descriptor | FE00302f00h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 03h (Gen2 SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | F00h: AMC Channel 0,Lane0,1,2,3 |
| AMC Link Descriptor | FE00202f00h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 02h (Gen2 NO SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | F00h: AMC Channel 0,Lane0,1,2,3 |
| AMC Link Descriptor | FE00102f00h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 01h (Gen1 SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | F00h: AMC Channel 0,Lane0,1,2,3 |
| AMC Link Descriptor | FE00002f00h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (Gen1 NO SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |

The following table gives AMC connectivity details for "Intel IOH PCI-Express Root Complex Port 8" (On-Carrier Device 1).

Table 4-27:AMC connectivity details for "Intel IOH PCI-Express Root Complex Port 8"

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Manufacturer ID | 00315Ah |
| PICMG Record ID | 19h (AMC Point-To-Point Connectivity Record) |
| Record Format Version | 00h |
| OEM GUID Count | 0h |
| Record Type/Connected-device ID | 01h(Carrier,Device 0->Intel IOH PCI-Express Root Complex Port 8) |
| AMC Channel Descriptor Count | 01h |
| AMC Channel Descriptor | F18820h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 03h |
| Lane 2 Port Number (Bits 14-10) | 02h |
| Lane 1 Port Number (Bits 9-5) | 01h |
| Lane 0 Port Number (Bits 4-0) | 00h |
| AMC Link Descriptor | FE00302f01h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 03h (Gen2 SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | F01h: AMC Channel 1,Lane0,1,2,3 |
| AMC Link Descriptor | FE00202f01h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 02h (Gen2 NO SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | F01h: AMC Channel 1,Lane0,1,2,3 |
| AMC Link Descriptor | FE00102f01h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 01h (Gen1 SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | F01h: AMC Channel 1,Lane0,1,2,3 |
| AMC Link Descriptor | FE00002f01h |
| Reserved (Bits 39-34) | 3Fh |

| Field | Value |
|---|---|
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (Gen1 NO SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | F01h: AMC Channel 1,Lane0,1,2,3 |
| AMC Link Descriptor | FE00302101h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 03h (Gen2 SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | 101h: AMC Channel 1,Lane0 |
| AMC Link Descriptor | FE00202101h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 02h (Gen2 NO SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | 101h: AMC Channel 1,Lane0 |
| AMC Link Descriptor | FE00102101h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 01h (Gen1 SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | 101h: AMC Channel 1,Lane0 |
| AMC Link Descriptor | FE00002101h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Provides a Secondary PCI Express Port) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (Gen1 NO SSC) |
| AMC Link Type (Bits 19-12) | 02h (AMC.1 PCI Express) |
| AMC Link Designator (Bits 11-0) | 101h: AMC Channel 1,Lane0 |

The following table gives AMC connectivity details for "Intel ICH10 SATA Controller" (On-Carrier Device 2).

Table 4-28: AMC connectivity details for "Intel ICH10 SATA Controller"

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Manufacturer ID | 00315Ah |
| PICMG Record ID | 19h (AMC Point-To-Point Connectivity Record) |
| Record Format Version | 00h |
| OEM GUID Count | 0h |
| Record Type/Connected-device ID | 02h(Carrier,Device 2->Intel ICH10 SATA Controller) |
| AMC Channel Descriptor Count | 02h |
| AMC Channel Descriptor | FFFFE0h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 1Fh |
| Lane 2 Port Number (Bits 14-10) | 1Fh |
| Lane 1 Port Number (Bits 9-5) | 1Fh |
| Lane 0 Port Number (Bits 4-0) | 00h |
| AMC Channel Descriptor | FFFFE1h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 1Fh |
| Lane 2 Port Number (Bits 14-10) | 1Fh |
| Lane 1 Port Number (Bits 9-5) | 1Fh |
| Lane 0 Port Number (Bits 4-0) | 01h |
| AMC Link Descriptor | FE00107102h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Implements SATA Client interface) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 01h (Serial ATA) |
| AMC Link Type (Bits 19-12) | 07h (AMC.3 Storage) |
| AMC Link Designator (Bits 11-0) | 102h: AMC Channel 2,Lane0 |
| AMC Link Descriptor | FE00107103h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 02h (Implements SATA Client interface) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 01h (Serial ATA) |
| AMC Link Type (Bits 19-12) | 07h (AMC.3 Storage) |
| AMC Link Designator (Bits 11-0) | 103h: AMC Channel 3,Lane0 |

The following table gives AMC connectivity details for "Intel 82576EB (front/rear)" (On-Carrier Device 3).

Table 4-29:AMC connectivity details for "Intel 82576EB NC (front/rear)"

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Manufacturer ID | 00315Ah |
| PICMG Record ID | 19h (AMC Point-To-Point Connectivity Record) |
| Record Format Version | 00h |
| OEM GUID Count | 0h |
| Record Type/Connected-device ID | 03h(Carrier,Device 3->Intel 82576EB NC (front/rear)) |
| AMC Channel Descriptor Count | 02h |
| AMC Channel Descriptor | FFFFE0h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 1Fh |
| Lane 2 Port Number (Bits 14-10) | 1Fh |
| Lane 1 Port Number (Bits 9-5) | 1Fh |
| Lane 0 Port Number (Bits 4-0) | 00h |
| AMC Channel Descriptor | FFFFE1h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 1Fh |
| Lane 2 Port Number (Bits 14-10) | 1Fh |
| Lane 1 Port Number (Bits 9-5) | 1Fh |
| Lane 0 Port Number (Bits 4-0) | 01h |
| AMC Link Descriptor | FC00005104h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 00h (Exact match) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (1000 BaseBX) |
| AMC Link Type (Bits 19-12) | 05h (AMC.2 Ethernet) |
| AMC Link Designator (Bits 11-0) | 104h: AMC Channel 4,Lane0 |
| AMC Link Descriptor | FC00005105h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 00h (Exact match) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (1000 BaseBX) |
| AMC Link Type (Bits 19-12) | 05h (AMC.2 Ethernet) |
| AMC Link Designator (Bits 11-0) | 105h: AMC Channel 5,Lane0 |

The following table gives AMC connectivity details for "Onboard Fabric Channel 1 Switch" (On-Carrier Device 4).

Table 4-30:AMC connectivity details for "Onboard Fabric Channel 1 Switch"

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Manufacturer ID | 00315Ah |
| PICMG Record ID | 19h (AMC Point-To-Point Connectivity Record) |
| Record Format Version | 00h |
| OEM GUID Count | 0h |
| Record Type/Connected-device ID | 04h(Carrier,Device 4->Onboard Fabric Channel 1 Switch) |
| AMC Channel Descriptor Count | 02h |
| AMC Channel Descriptor | FFFFE7h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 1Fh |
| Lane 2 Port Number (Bits 14-10) | 1Fh |
| Lane 1 Port Number (Bits 9-5) | 1Fh |
| Lane 0 Port Number (Bits 4-0) | 007h |
| AMC Channel Descriptor | FFFFE8h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 1Fh |
| Lane 2 Port Number (Bits 14-10) | 1Fh |
| Lane 1 Port Number (Bits 9-5) | 1Fh |
| Lane 0 Port Number (Bits 4-0) | 08h |
| AMC Link Descriptor | FC00005106h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 00h (Exact match) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (1000 BaseBX) |
| AMC Link Type (Bits 19-12) | 05h (AMC.2 Ethernet) |
| AMC Link Designator (Bits 11-0) | 106h: AMC Channel 6,Lane0 |
| AMC Link Descriptor | FC00005107h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 00h (Exact match) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (1000 BaseBX) |
| AMC Link Type (Bits 19-12) | 05h (AMC.2 Ethernet) |
| AMC Link Designator (Bits 11-0) | 107h: AMC Channel 7,Lane0 |

The following table gives AMC connectivity details for "Onboard Fabric Channel 2 Switch" (On-Carrier Device 5).

Table 4-31:AMC connectivity details for "Onboard Fabric Channel 2 Switch"

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Manufacturer ID | 00315Ah |
| PICMG Record ID | 19h (AMC Point-To-Point Connectivity Record) |
| Record Format Version | 00h |
| OEM GUID Count | 0h |
| Record Type/Connected-device ID | 05h(Carrier,Device 5->Onboard Fabric Channel 2 Switch) |
| AMC Channel Descriptor Count | 02h |
| AMC Channel Descriptor | FFFFE7h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 1Fh |
| Lane 2 Port Number (Bits 14-10) | 1Fh |
| Lane 1 Port Number (Bits 9-5) | 1Fh |
| Lane 0 Port Number (Bits 4-0) | 07h |
| AMC Channel Descriptor | FFFFE8h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 1Fh |
| Lane 2 Port Number (Bits 14-10) | 1Fh |
| Lane 1 Port Number (Bits 9-5) | 1Fh |
| Lane 0 Port Number (Bits 4-0) | 08h |
| AMC Link Descriptor | FC00005108h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 00h (Exact match) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (1000 BaseBX) |
| AMC Link Type (Bits 19-12) | 05h (AMC.2 Ethernet) |
| AMC Link Designator (Bits 11-0) | 108h: AMC Channel 8,Lane0 |
| AMC Link Descriptor | FC00005109h |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 00h (Exact match) |

| Field | Value |
|---|---|
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (1000 BaseBX) |
| AMC Link Type (Bits 19-12) | 05h (AMC.2 Ethernet) |
| AMC Link Designator (Bits 11-0) | 109h: AMC Channel 9,Lane0 |

The following table gives AMC connectivity details for COM2 (On-Carrier Device 5)

Table 4-32:AMC connectivity details for "FPGA Based UART"

| Field | Value |
|---|---|
| Record Type ID | C0h |
| Record format version | 02h |
| Record Length | *Calculated |
| Record Checksum | *Calculated |
| Header Checksum | *Calculated |
| Manufacturer ID | 00315Ah |
| PICMG Record ID | 19h (AMC Point-To-Point Connectivity Record) |
| Record Format Version | 00h |
| OEM GUID Count | 1h |
| OEM GUID Id 0 | 471C5D14-2AE7-42B9-A9B0-0628546B42CC (OEM Module Serial Console Interconnect) |
| Record Type/Connected-device ID | 06h(Carrier,Device 6->FPGA Based UART) |
| AMC Channel Descriptor Count | 01h |
| AMC Channel Descriptor | FFFFE0h |
| Reserved (Bits 23-20) | 0Fh |
| Lane 3 Port Number (Bits 19-15) | 1Fh |
| Lane 2 Port Number (Bits 14-10) | 1Fh |
| Lane 1 Port Number (Bits 9-5) | 1Fh |
| Lane 0 Port Number (Bits 4-0) | 00h |
| AMC Link Descriptor | FC000f010ah |
| Reserved (Bits 39-34) | 3Fh |
| AMC Asymmetric Match (Bits 33-32) | 00h (Exact match) |
| Link Grouping ID (Bits 31-24) | 00h (Single-Channel Link) |
| AMC Link Type Extension (Bits 23-20) | 00h (None) |
| AMC Link Type (Bits 19-12) | F0h (OEM Module Serial Console Interconnect) |
| AMC Link Designator (Bits 11-0) | 10Ah: AMC Channel 10,Lane0 |

The AMC connectivity details for "On-Carrier Virtual RTM Device" is embedded on the RTM itself.

## 4.3.4 Clock E-Keying Information

The clock ekeying is used to find and activate matching clock pairs to/from available clock sources and clock receivers.
The board has a clock generator used as the (PCIe) FCLKA of AMC B1. Additionally, clocks from/to the ATCA backplane can be driven to/from the AMC B1 site using an on-carrier clock multiplexer.

The following table gives the clock resources id assignment mapping.

Table 4-33:Clock resources id assignment mapping

| OnBoard Clock Device | Clock Resource Id |
|---|---|
| PCIe Clock Generator | 0 |
| Clock Multiplexer | 1 |

### *4.3.4.1 Clock Point-To-Point Connectivity Information*

The following table gives all the clock link paths available on the Front Board Unit, as they appear in the FRU data in the Carrier Clock Point-to-Point Connectivity Record Table record.

Table 4-34:Carrier Clock Point-to-Point Connectivity Record Table

| Field | Value | Description |
|---|---|---|
| Record Type ID | C0h | |
| Record format version | 02h | |
| Record Length | *Calculated | |
| Record Checksum | *Calculated | |
| Header Checksum | *Calculated | |
| Manufacturer ID | 00315Ah | PICMG Record ID |
| PICMG Record ID | 2Ch | Carrier Clock Point-To-Point Connectivity Record |
| Record Format Version | 00h | |
| Clock Point-To-Point Resource Descriptor Count (m) | 0x02 | |
| Clock Point-To-Point Resource Descriptor | | |
| Clock Resource Id | 0x00 | 7:6 00b = On-Carrier device<br>5:4 0h (reserved)<br>3:0 On-Carrier Device 0 ( PCIe clock generator ) |
| Clock Point-to-Point Connection Count | 0x01 | |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x00 | On-Carrier Clock Id 0 |
| Remote Clock Id | 0x05 | AMC.0 R2.0 FCLKA clock |
| Remote Clock Resource Id | 0x45 | 7:6 01b = AMC<br>5:4 0h (reserved)<br>3:0 AMC Site Number ( 5 = AMC B1) |
| Clock Point-To-Point Resource Descriptor | | |

| Field | Value | Description |
|---|---|---|
| Clock Resource Id | 0x01 | 7:6 00b = On-Carrier device<br>5:4 0h (reserved)<br>3:0 On-Carrier Device 1( Clock Mux ) |
| Clock Point-to-Point Connection Count | 0x0A | |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x00 | On-Carrier Clock Id 0 |
| Remote Clock Id | 0x01 | CLK1A |
| Remote Clock Resource Id | 0x80 | 7:6 10b = Backplane clock<br>5:4 0h (reserved)<br>3:0 0h |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x01 | On-Carrier Clock Id 1 |
| Remote Clock Id | 0x02 | CLK1B |
| Remote Clock Resource Id | 0x80 | 7:6 10b = Backplane clock<br>5:4 0h (reserved)<br>3:0 0h |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x02 | On-Carrier Clock Id 2 |
| Remote Clock Id | 0x04 | CLK2A |
| Remote Clock Resource Id | 0x80 | 7:6 10b = Backplane clock<br>5:4 0h (reserved)<br>3:0 0h |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x03 | On-Carrier Clock Id 3 |
| Remote Clock Id | 0x05 | CLK2B |
| Remote Clock Resource Id | 0x80 | 7:6 10b = Backplane clock<br>5:4 0h (reserved)<br>3:0 0h |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x04 | On-Carrier Clock Id 4 |
| Remote Clock Id | 0x07 | CLK3A |
| Remote Clock Resource Id | 0x80 | 7:6 10b = Backplane clock<br>5:4 0h (reserved)<br>3:0 0h |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x05 | On-Carrier Clock Id 5 |
| Remote Clock Id | 0x08 | CLK3B |
| Remote Clock Resource Id | 0x80 | 7:6 10b = Backplane clock<br>5:4 0h (reserved)<br>3:0 0h |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x06 | On-Carrier Clock Id 6 |
| Remote Clock Id | 0x01 | TCLKA |
| Remote Clock Resource Id | 0x45 | 7:6 01b = AMC<br>5:4 0h (reserved)<br>3:0 AMC Site Number ( 5 = AMC B1) |
| Point-to-Point Clock Connection descriptor | | |

| Field | Value | Description |
|---|---|---|
| Local Clock Id | 0x07 | On-Carrier Clock Id 7 |
| Remote Clock Id | 0x03 | TCLKC |
| Remote Clock Resource Id | 0x45 | 7:6 01b = AMC<br>5:4 0h (reserved)<br>3:0 AMC Site Number ( 5 = AMC B1) |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x08 | On-Carrier Clock Id 8 |
| Remote Clock Id | 0x04 | TCLKB |
| Remote Clock Resource Id | 0x45 | 7:6 01b = AMC<br>5:4 0h (reserved)<br>3:0 AMC Site Number ( 5 = AMC B1) |
| Point-to-Point Clock Connection descriptor | | |
| Local Clock Id | 0x09 | On-Carrier Clock Id 9 |
| Remote Clock Id | 0x04 | TCLKD |
| Remote Clock Resource Id | 0x45 | 7:6 01b = AMC<br>5:4 0h (reserved)<br>3:0 AMC Site Number ( 5 = AMC B1) |

#### *4.3.4.2 Clock Configuration Information*

The following table gives AMC clock connectivity details for "PCIe Clock Generator" (On-Carrier Device 0).

Table 4-35:PCIe Clock Generator

| Field | Value | Description |
|---|---|---|
| Record Type ID | C0h | |
| Record format version | 02h | |
| Record Length | *Calculated | |
| Record Checksum | *Calculated | |
| Header Checksum | *Calculated | |
| Manufacturer ID | 00315Ah | PICMG Record ID |
| PICMG Record ID | 2Dh | Clock Configuration Record |
| Record Format Version | 00h | |
| Clock Resource Id | 0x00 | 7:6 00b = On-Carrier device 5:4 0h (reserved) 3:0 00h = On-Carrier Device 0 ( PCIe clock generator ) |
| Clock Configuration Descriptor Count | 0x01 | |
| Clock Configuration Descriptors | | |
| Clock Id | 0x00 | |
| Clock Control | 0x00 | 7:1 0h (reserved) [0] 0b = Activated by Carrier IPMC |
| Indirect Clock Descriptors Count(m) | 0x00 | |
| Direct Clock Descriptors Count(n) | 0x01 | |
| Indirect clock Descriptor | | None |
| Direct clock Descriptor | | |
| Features | 0x01 | 7:2 0h (reserved) [1] 0b = Not connected through PLL [0] 1b = Clock source |

| Field | Value | Description |
|---|---|---|
| Family | 0x02 | Reserved for PCI Express |
| Accuracy Level | 0x0E | Gen 2 Capable PCIe Clock |
| Frequency | 0x05F5E100 | As defined in AMC.1 R2.0 |
| Min Clock | 0x05F5E100 | As defined in AMC.1 R2.0 |
| Max Clock | 0x05F5E100 | As defined in AMC.1 R2.0 |

The following table gives AMC clock connectivity details for "Onboard Clock Multiplexer" (On-Carrier Device 1).

Table 4-36:Onboard Clock Multiplexer

| Field | Value | Description |
|---|---|---|
| Record Type ID | C0h | |
| Record format version | 02h | |
| Record Length | *Calculated | |
| Record Checksum | *Calculated | |
| Header Checksum | *Calculated | |
| Manufacturer ID | 00315Ah | PICMG Record ID |
| PICMG Record ID | 2D | Clock Configuration Record |
| Record Format Version | 00h | |
| Clock Resource Id | 0x01 | 7:6 00b = On-Carrier device 5:4 0h (reserved) 3:0 01h = On-Carrier Device 1 (Clock Multiplexer) |
| Clock Configuration Descriptor Count | 0x0A | |
| Clock Configuration Descriptors | | |
| Clock Id | 0x00 | Receiver input from CLK1A |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x02 | |
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 6 | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 7 | |
| Direct clock Descriptor | | none |
| Clock Id | 0x01 | Receiver input from CLK1B |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x02 | |
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |

| Field | Value | Description |
|---|---|---|
| Dependent ClockId | 6 | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 7 | |
| Direct clock Descriptor | | none |
| Clock Id | 0x02 | Receiver input from CLK2A |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x02 | |
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 6 | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 7 | |
| Direct clock Descriptor | | none |
| Clock Id | 0x03 | Receiver input from CLK2B |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x02 | |
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 6 | |
| Features | | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 7 | |
| Direct clock Descriptor | | none |
| Clock Id | 0x04 | Source output to CLK3A |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x02 | |
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x01 | 7:2 0h (reserved) [1] 0b = Not Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 8 | |
| Features | 0x01 | 7:2 0h (reserved) [1] 0b = Not Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 9 | |
| Direct clock Descriptor | | none |
| Clock Id | 0x05 | Source output to CLK3B |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x02 | |

| Field | Value | Description |
|---|---|---|
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x01 | 7:2 0h (reserved) [1] 0b = Not Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 8 | |
| Features | 0x01 | 7:2 0h (reserved) [1] 0b = Not Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 9 | |
| Direct clock Descriptor | | none |
| Clock Id | 0x06 | Source output to TCLKA |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x04 | |
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x03 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 0 | |
| Features | 0x03 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 1 | |
| Features | 0x03 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 2 | |
| Features | 0x03 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 3 | |
| Direct clock Descriptor | | none |
| Clock Id | 0x07 | Source output to TCLKC |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x04 | |
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x03 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 0 | |
| Features | 0x03 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 1 | |
| Features | 0x03 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 2 | |
| Features | 0x03 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 1b = Clock Source |
| Dependent ClockId | 3 | |
| Direct clock Descriptor | | none |

| Field | Value | Description |
|---|---|---|
| Clock Id | 0x08 | Receiver input from TCLKB |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x02 | |
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 4 | 4 |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 5 | |
| Direct clock Descriptor | | none |
| Clock Id | 0x09 | Receiver input from TCLKD |
| Clock Control | 0x01 | 7:1 0h (reserved) [0] 1b = Activated by Application |
| Indirect Clock Descriptors Count(m) | 0x02 | |
| Direct Clock Descriptors Count(n) | 0x00 | |
| Indirect clock Descriptor | | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 4 | |
| Features | 0x02 | 7:2 0h (reserved) [1] 1b = Connected through PLL [0] 0b = Clock Receiver |
| Dependent ClockId | 5 | |
| Direct clock Descriptor | | none |

### 4.3.5 Component Upgrade Support

Many components can be updated through the IPMC. Most of them (IPMC itself, FPGA and BIOS) are updated using the HPM.1 Hardware Platform Management IPM Controller Firmware Upgrade Specification revision 1.0. Kontron's IPMC firmware already complies to PICMG HPM.1 R1.0. HPM commands are available from any of the MC messaging interfaces. The images of the different components can be packaged in the same HPM image (They can also be separated). Packaging the images together allows to upgrade all the components using only one upgrade instruction. Moreover, it ensure all components upgraded are compatible.

The following table gives the HPM component IDs implemented on the AT8050.

Table 4-37:HPM component IDs

| Component ID | Description |
|---|---|
| 0 | MC Bootblock |
| 1 | IPMC Firmware |
| 2 | FPGA |
| 3 | BIOS |

Furthermore, non-HPM components can also be updated via the MC.

Table 4-38:non-HPM components

| Non HPM Component | Description |
|---|---|
| CMOS | CMOS information, programmed through Master Write/Read API |
| FRU Data | The FRU inventory information is updated via "Write FRU Data" commands |
| ME | Management Engine, updated through Intel's OEM update commands |

*Chapter 5*

# Software Setup

# 5. Software Setup

## 5.1 AMI BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory backed-up by a supercap or in the main BIOS flash and EEPROM. The latest is the default configuration.

### 5.1.1 Accessing the BIOS Setup Utility

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the AT8050. It uses the AMI Setup program, a setup utility in flash memory that is accessed by pressing the <DEL> (or <F4> from a console redirection terminal) key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

To run the AMI Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- When you get the following messages, hit <DEL> key to enter SETUP.

```
AMIBIOS(C)2010 American Megatrends, Inc.
KONTRON AT8050 BIOS Version 3.00


(C) American Megatrends, Inc.
64-3047-009999-00101111-031710-TYLSBURG-5007_300-Y2KC


Physical Processors Package: 1
Active Processors Cores: 4
Logical Processors: 8
Intel HT Technology: Enabled
QPI Speed: 5.866GT
CPU : Intel(R) Xeon(R) CPU L5518  @ 2.13GHz
 Speed : 2.13 GHz

Reset Type: Cold Reset
Currently Running On Primary BIOS.

Press DEL to run Setup (F4 on Remote Keyboard)
Press F12 if you want to boot from the network
Press F11 for BBS POPUP (F3 on Remote Keyboard)
Initializing USB Controllers .. Done.

Memory Channel 0 DIMM 0 Size 2048MB
Memory Channel 0 DIMM 1 Size Not Installed
Memory Channel 1 DIMM 0 Size 2048MB
Memory Channel 1 DIMM 1 Size Not Installed
Memory Channel 2 DIMM 0 Size 2048MB
Memory Channel 2 DIMM 1 Size Not Installed
DDR3: 6144MB OK, Speed: 1066MHz

Auto-detecting USB Mass Storage Devices ..
00 USB mass storage devices found and configured.
```

The main menu of the AMI BIOS CMOS Setup Utility appears on the screen.

```
  Main    Advanced    Security    Boot    System Management    Exit
*************************************************************************************
* System Overview                                        * Sub-menu to display    *
* ****************************************************** * memory configuration   *
* AMIBIOS                                                * of each DIMM           *
* BIOS Version                  08.00.15                 *                         *
* Build Date:                   03/24/10                 *                         *
* BIOS ID                       5007_300                 *                         *
* FPGA Version:                 2.04                     *                         *
*                                                        *                         *
*                                                        *                         *
* System Memory                 1016MB                   *                         *
* System Memory Speed           1333MHz                  *                         *
* * Memory Size Configuration                            *                         *
*                                                        * *    Select Screen     *
*                                                        * **    Select Item      *
*                                                        * Enter Go to Sub Screen *
*                                                        * F1    General Help     *
* System Time                   [23:33:11]               * F10   Save and Exit    *
* System Time                   [23:33:14]               * F10   Save and Exit    *
*                                                        *                         *
*                                                        *                         *
*************************************************************************************
           v02.61 (C)Copyright 1985-2010, American Megatrends, Inc.
```

Setup Default values provide optimum performance settings for all devices and system features.

**Note:**
The CMOS setup option described in this section is based on BIOS Version 3.00 The options and default settings may change in a new BIOS release.

**CAUTION**

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

**Note:**
All options in Bold are the default settings.

**WARNING**

BIOS V3.00 and highier is required to operate the board with a 5600 series processor.

## 5.1.2 Menu Bar

The Menu Bar at the top of the window lists these selections:

| Menu Selection | Description |
|---|---|
| Main | Use this menu for basic system configuration. |
| Advanced | Use this menu to set the Advanced Features available on your system. |
| Security | Use this menu to configure Security features. |
| Boot | Use this menu to determine the booting device order. |
| System Management | Use this menu to set and view the System Managment on your system. |
| Exit | Use this menu to choose Exits option. |

Use the left and right arrows keys to make a selection.

### *5.1.2.1 Legend Bar*

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates.

| Key | Function |
|---|---|
| <F1> | General Help windows. |
| <Esc> | Exit this menu. |
| --> arrow keys | Select a different menu. |
| <Home> or <End> | Move cursor to top or bottom of window. |
| <PgUp> or <PgDn> | Move cursor to top or bottom of window. |
| <-> | Select the Previous Value for the field. |
| <+> | Select the Next Value for the field. |
| <F2> and <F3> | Change colors used in Setup. |
| <F7> | Disacard the changes for all menus. |
| <F9> | Load the Optimal Default Configuration values for all menus. |
| <F10> | Save and exit. |
| <Enter> | Execute Command, display possible value for this field or Select the sub-menu. |

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. To save value commands in the Exit Menu, save the values displayed in all menus.

To display a submenu, use the arrow keys to move the cursor to the submenu you want. Then press <Enter>.

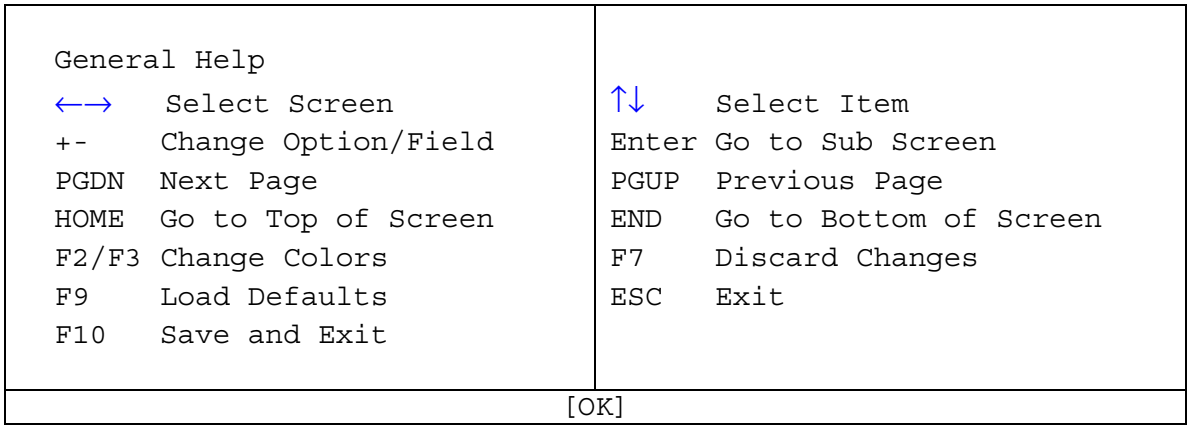
### *5.1.2.2 Field Help Window*

The help window on the right side of each menu displays the help text for the selected field.

It updates as you move the cursor to each field.

### 5.1.2.3 General Help Windows

Pressing <F1>on any menu brings up the General Help window that describes the legend keys and their alternates:




## 5.1.3 Main Menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| BIOS Version | 8.00.15 | Displays the AMI BIOS version. | N/A, display only. |
| Build Date | MM/DD/YY | Display the BIOS build Date. | N/A, display only. |
| BIOS ID | 5007_XYY | Display the BIOS ID, this include the BIOS Version. | N/A, display only. |
| FPGA Version | X.YY | Display the FPGA Version. | N/A, display only. |
| System Memory | X KB | Displays amount system memory. | N/A, display only. |
| System Memory Speed | X KB | Displays speed of the system memory. | N/A, display only. |
| Memory Size Configuration | N/A | Select sub-menu. | Sub-menu to display memory configuration of each DIMM. |
| System Time | HH:MM:SS | Set the system time. | Use [+] or [-] to configure system time. |
| System Date | MM/DD/YYYY | Set the system date. | Use [+] or [-] to configure system date. |

#### 5.1.3.1 Memory Size Configuration menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Channel 0, DIMM 0 Memory Size | X GB | Displays Channel 0, DIMM 0 memory size. AT8050: DIMM electrically farthest to CPU (filled first). DIMMs within a channel must be populated starting with the DIMMs farthest from the processor in a "fill-farthest" approach. | N/A, display only. |
| Channel 0, DIMM 1 Memory Size | X GB | Displays Channel 0, DIMM 1 memory size. AT8050: DIMM electrically closest to CPU (filled last). | N/A, display only. |
| Channel 1, DIMM 0 Memory Size | X GB | Displays Channel 1, DIMM 0 memory size. AT8050: DIMM electrically farthest to CPU (filled first). DIMMs within a channel must be populated starting with the DIMMs farthest from the processor in a "fill-farthest" approach. | N/A, display only. |
| Channel 1, DIMM 1 Memory Size | X GB | Displays Channel 1, DIMM 1 memory size. AT8050: DIMM electrically closest to CPU (filled last). | N/A, display only. |
| Channel 2, DIMM 0 Memory Size | X GB | Displays Channel 2, DIMM 0 memory size. AT8050: DIMM electrically farthest to CPU (filled first). DIMMs within a channel must be populated starting with the DIMMs farthest from the processor in a "fill-farthest" approach. | N/A, display only. |
| Channel 2, DIMM 1 Memory Size | X GB | Displays Channel 2, DIMM 1 memory size. AT8050: DIMM electrically closest to CPU (filled last). | N/A, display only. |
| System Memory Speed | X MHz | Displays system Memory speed | N/A, display only. |

### 5.1.4 Advanced Menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Advanced Processor Configuration | N/A | Selects sub-menu. | N/A |
| ACPI Configuration | N/A | Selects sub-menu. | N/A |
| Drive Configuration | N/A | Selects sub-menu | N/A |
| Event Log Configuration | N/A | Selects sub-menu. | N/A |
| Expansion ROM Configuration | N/A | Selects sub-menu. | N/A |
| PCI Express Configuration | N/A | Selects sub-menu. | N/A |
| USB Configuration | N/A | Selects sub-menu. | N/A |
| Advanced Chipset Control | N/A | Selects sub-menu. | N/A |
| Intel VT-d Configuration | N/A | Selects sub-menu. | N/A |
| I/O Virtualization | N/A | Selects sub-menu. | N/A |

### 5.1.4.1 Advanced Processor Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Manufacturer | Display | Show information about the CPU | N/A |
| Frequency | Display | Show frequency of the CPU | N/A |
| Cache L1 | Display | Show amount of L1 cache | N/A |
| Cache L2 | Display | Show amount of L2 cache | N/A |
| Cache L3 | Display | Show amount of L3 cache | N/A |
| Logical Processor | Display | Show total of processor including HT. | N/A |
| Physical Processor | Display | Show physical processor present in CPU | N/A |
| MPS and ACPI MADT ordering | **Modern ordering**<br>Legacy ordering | | MPS and ACPI MADT ordering.<br>Modern ordering for Windows XP or later OSes.<br>Legacy ordering for Windows 2000 or earlier OSes. |
| Max CPUID Value Limit | Disabled<br>**Enabled** | | Enable for legacy operating systems does not support CPUID function > 3. |
| Processor Virtualization | **Enabled**<br>Disabled | Allow virtualization to be enable, need supported OS | Enabled: Processor virtualization in use.<br>Disabled: Processor virtualization not in use. |
| CPU TM function | **Enabled**<br>Disabled | The Core i7 support only all enabled or all disabled. | CPU Thermal Monitor mechanism supoorted TM1 and TM2. They are all enabled together. |
| Intel® HT Technology | **Enabled**<br>Disabled | This allows multiprocessor to be enabled. | When 'Disabled' only one thread per enabled core is enabled. |
| Intel® SpeedStep™ tech | **Enabled**<br>Disabled | This allows Geyserville 3 to be enabled. | Disable: Disable GV3<br>Enable: Enable GV3 |
| Intel® TurboMode™ tech | **Enabled**<br>Disabled | This allows processor to increase spped when CPU are not used. | Turbo Mode allows processor cores to run faster than marked frequency in specifica condition. |

### 5.1.4.2 ACPI Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| ACPI Version Features | **V3.0**<br>V2.0<br>V1.0 | Support for 64-bit addressing for ACPI System Description Tables in ACPI 3.0, Only 32 bit for others description tables. | Enable RSDP pointers to 64-bit Fixed System Description Tables. Different ACPI version has some addition. |
| ACPI APIC Support | **Enabled**<br>Disabled | Support for ACPI APIC table pointer to Root System Description Table, RSDT pointer list can be enabled/disabled. | Enabled: ACPI APIC table support. Disabled: ACPI APIC table not supported. |
| Headless Mode | **Enabled**<br>Disabled | Headless operation mode through ACPI can be enabled/disabled. | Enabled: Headless operation mode through ACPI supported. Disabled: Headless operation mode through ACPI not supported. |

### 5.1.4.3 Drive Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| SATA#1 Configuration | Disabled<br>Compatible<br>**Enhanced** | Select whether the controller is using only legacy resources i.e. IRQ 14-15(compatible) or with memory resources only (Enhanced). Only shows when SATA#1 is configure in IDE mode. | AHCI: allows advanced SATA features such as Native Command Queuing and hot plug. IDE is legacy disk usage. |
| Configure SATA#1 as | **AHCI**<br>IDE | Advanced Host Controller Interface (AHCI) is an | AHCI: allows advanced SATA features such as Native Command Queuing and hot plug. IDE is legacy disk usage. |
| SATA Port 0 (PM) | N/A | Selects sub-menu. Only shows if "Configure SATA#1 as" is set to "IDE" | While entering setup, BIOS auto detects the presence of IDE devices. This displays the satus of auto detection of IDE devices. |
| SATA Port 1 (SM) | N/A | Selects sub-menu. Only shows if "Configure SATA#1 as" is set to "IDE" | While entering setup, BIOS auto detects the presence of IDE devices. This displays the satus of auto detection of IDE devices. |
| SATA Port 2 (PS) | N/A | Selects sub-menu. Only shows if "Configure SATA#1 as" is set to "IDE" | While entering setup, BIOS auto detects the presence of IDE devices. This displays the satus of auto detection of IDE devices. |
| AHCI Configuration | N/A | Selects sub-menu. | Section for AHCI Configuration. |

#### 5.1.4.3.1 SATA Port 0 (PM) Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Device | N/A | Display the device type (Hard disk). | Display only |
| Vendor | N/A | Display the vendor string of the disk. | Display only |
| Size | N/A | Display the size of the disk. | Display only |
| Ultra DMA | N/A | Display the current speed of the drive. | Display only |
| S.M.A.R.T. | N/A | Display the status of the Self-Monitoring, Analysis, and Reporting Technology. | Display only |
| Type | **Auto**<br>Not Installed | Auto will detect the device. Not installed will not detect the device. | Select the type of device connected to the system. |

#### 5.1.4.3.2 SATA Port 1 (SM) Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Device | N/A | Display the device type (Hard disk). | Display only |
| Vendor | N/A | Display the vendor string of the disk. | Display only |
| Size | N/A | Display the size of the disk. | Display only |
| Ultra DMA | N/A | Display the current speed of the drive. | Display only |
| S.M.A.R.T. | N/A | Display the status of the Self-Monitoring, Analysis, and Reporting Technology. | Display only |
| Type | **Auto**<br>Not Installed | Auto will detect the device. Not installed will not detect the device. | Select the type of device connected to the system. |

#### 5.1.4.3.3 SATA Port 2 (PS) configuration sub-menu fields.

| Feature | Option | Description | Help text |
|---|---|---|---|
| Device | N/A | Display the device type (Hard disk). | Display only |
| Vendor | N/A | Display the vendor string of the disk. | Display only |
| Size | N/A | Display the size of the disk. | Display only |
| Ultra DMA | N/A | Display the current speed of the drive. | Display only |
| S.M.A.R.T. | N/A | Display the status of the Self-Monitoring, Analysis, and Reporting Technology. | Display only |
| Type | **Auto**<br>Not Installed | Auto will detect the device. Not installed will not detect the device. | Select the type of device connected to the system. |

#### 5.1.4.3.4 AHCI Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| AHCI Port0 | N/A | Selects sub-menu. | While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of IDE devices. |
| AHCI Port1 | N/A | Selects sub-menu. | While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of IDE devices. |
| AHCI Port2 | N/A | Selects sub-menu. | While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of IDE devices. |

##### 5.1.4.3.4.1AHCI Port0 Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Device: | N/A | Show device type | N/A |
| Vendor: | N/A | Show HDD name and brand | N/A |
| Size | N/A | Show HDD size | N/A |
| SATA Port0 | **Auto**<br>Not Installed | When using "Not Installed" the controller will disable the device. | Select the type of device connected to the system. |

##### 5.1.4.3.4.2AHCI Port1 Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Device: | N/A | Show device type | N/A |
| Vendor: | N/A | Show HDD name and brand | N/A |
| Size | N/A | Show HDD size | N/A |
| SATA Port1 | **Auto**<br>Not Installed | When using "Not Installed" the controller will disable the device. | Select the type of device connected to the system. |

#### 5.1.4.3.4.3AHCI Port2 Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Device: | N/A | Show device type | N/A |
| Vendor: | N/A | Show HDD name and brand | N/A |
| Size | N/A | Show HDD size | N/A |
| SATA Port2 | **Auto**<br>Not Installed | When using "Not Installed" the controller will disable the device. | Select the type of device connected to the system. |

### *5.1.4.4 Event Log Configuration sub-menu*

| Feature | Option | Description | Help text |
|---|---|---|---|
| View Event Log | Enter | View all unread events in the Event Log. | View all unread events in the Event Log. |
| Mark Events as read | Enter | Mark all unread events as read in the Event Log. | Mark all unread events as read in the Event Log. |
| Clear all Event Logs | Enter | Discard all events in the Event Log. | Discard all events in the Event Log. |
| PCIE Error Log | **Yes**<br>No | | Options<br>No<br>Yes |
| DRAM Data Integrity Mode | **ECC**<br>Non-ECC | | ECC: ECC Checking enables.<br>Non-ECC: Use only for testing purposes. |
| ECC Error Reporting | **Disabled**<br>Correctable<br>Uncorrectable<br>both | | Correctable: ECC for testing purposes.<br>Uncorrestable: ECC errors reported.<br>Both: ECC errors for testing purposes.<br>Disabled: ECC errors not reported. |

### 5.1.4.5 Expansion ROM Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Ethernet BI Expansion ROM | Disabled<br>iSCSI<br>**PXE** | The base interface PXE Expansion ROM can be enabled/disabled. If disabled, remote LAN boot via base interface is not available to boot the system. | Disabled: Base interface PXE expansion ROM not used. If disabled, remote LAN boot via BI is not available to boot the system! ISCSI: Initializes iSCSI expansion ROM. PXE: Initializes base interface PXE expansion ROM. |
| Ethernet FI Expansion ROM | **Disabled**<br>iSCSI<br>PXE | The fabric interface PXE Expansion ROM can be enabled/disabled. If disabled, remote LAN boot via fabric interface is not available to boot the system. | Disabled: Fabric interface PXE expansion ROM not used. If disabled, remote LAN boot via FI is not available to boot the system! iSCSI:Initializes iSCSI expansion ROM. PXE: Initializes fabric interface PXE expansion ROM. |
| Management Ports Expansion ROM | **Disabled**<br>PXE | The Management Ports PXE Expansion ROM on the face plate can be enabled/disabled. If disabled, remote LAN boot via the management ports on the face plate is not available to boot the system. | Enabled: Initializes Management Ports PXE expansion ROM. Disabled: Management Ports PXE expansion ROM not used. If disabled, remote LAN boot via Management Ports is not available to boot the system! |
| RTM Expansion ROM | **Enabled**<br>Disabled | The RTM Expansion ROM can be enabled/ disabled. If disabled, any SAS devices attached to the RTM are not available to boot the system. | Enabled: Initializes RTM expansion ROM. Disabled: RTM expansion ROM not used. If disabled, any SAS devices attached to the RTM are not available to boot the system! |
| AMC Slot Expansion ROM | Enabled<br>**Disabled** | Enables or disables AMC Slot Expansion ROM(s), if any detected. If disabled, AMC Expansion ROM(s) code will not be executed during POST. | Enabled: Initializes AMC slot expansion ROM. Disabled: AMC slot expansion ROM not used. |
| Update Channel Expansion ROM | **Enabled**<br>Disabled | Enables or disables Update Channel Expansion ROM(s), if any detected. If disabled, Update Channel Expansion ROM(s) code will not be executed during POST | Enabled: Initializes Update Channel expansion ROM. Disabled: Update |

### 5.1.4.6 PCI Express Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| RTM Hot Plug Support | **Enabled**<br>Disabled | RTM hot plug support can be enabled/ disabled. | Enabled: Hot Plug for RTM available.<br>Disabled: Hot Plug for RTM not available.<br>Note: Need Power Cycle with any changes. |
| AMC Slot Hot Plug Support | **Enabled**<br>Disabled | AMC slot hot plug support can be enabled/ disabled. | Enabled: Hot Plug for AMC slot available.<br>Disabled: Hot Plug for AMC slot not available.<br>Note: Need Power Cycle with any changes. |
| Force Gen1 on AMC | Enabled<br>**Disabled** | Setting this to Enabled will force AMC in Gen1 Mode. Gen 2 will not be used. | Setting this to Enabled will force AMC in Gen1 Mode. |
| Relaxed Ordering | **Auto**<br>Disabled<br>Enabled | The Relaxed Ordering attribute is applicable and permitted to be Set with AtomicOp Requests, where it affects the ordering of both the Requests and their associated Completions. | Enables/Disables PCI Express Device Relaxed Ordering. |
| Maximum Payload Size | **Auto**<br>128 Bytes<br>256 Bytes<br>512 Bytes<br>1024 Bytes<br>2048 Bytes<br>4096 Bytes | This field sets maximum TLP payload size for the Function. As a Receiver, the Function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. | Set Maximum Payload of PCI Express Device or allow System BIOS select the value. |
| Extended Tag Field | **Auto**<br>Disabled<br>Enabled | Enables a Function to use an 8-bit Tag field as a Requester. If the bit is Clear, the Function is restricted to a 5-bit Tag field. | If ENABLED, allows Devoce to use 8-bit TAG field as a requester. |
| No Snoop | **Auto**<br>Disabled<br>Enabled | The No Snoop attribute is applicable and permitted to be Set with AtomicOp Requests, but atomicity must be guaranteed regardless of the No Snoop attribute value | Enables/Disables PCI Express Device No Snoop option. |
| Maximum Read Request Size | **Auto**<br>128 Bytes<br>256 Bytes<br>512 Bytes<br>1024 Bytes<br>2048 Bytes<br>4096 Bytes | This field sets the maximum Read Request size for the Function as a Requester. The Function must not generate Read Requests with size exceeding the set value. | Set Maximum Read Request Size of PCI Express Device or allow System BIOS select the value. |
| Extended Synch | **Auto**<br>Disabled<br>Enabled | When Enabled, this bit forces the transmission of additional Ordered Sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. | If ENABLED, allows generation of Extended Synchronization patterns. |

### 5.1.4.7 USB Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| USB 2.0 Controller Mode | FullSpeed<br>**HiSpeed** | Configures the USB 2.0 Controller in HiSpeed (480Mbps) or FullSpeed (12Mbps). | FullSpeed: 12 Mbps<br>HiSpeed: 480 Mbps |
| BIOS EHCI Hand-Off | **Enabled**<br>Disabled | A workaround for OSes without EHCI hand-off support can be enabled/disabled. The EHCI ownership change should be claimed by an EHCI driver. | Enabled: EHCI hand-off support enabled.<br>Disabled: EHCI hand-off support disabled. |
| USB Mass Storage Device Configuration (only present if USB Mass Storage detected) | N/A | Selects sub-menu. | Configure the USB Mass Storage Class Devices. |

### 5.1.4.8 USB Mass Storage Device Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Device #1-6 | | Mass Storage Device identification | |
| Emulation Type (for each devices) | **Auto**<br>Floppy<br>Forced FDD<br>Hard Disk<br>CDROM | If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive). | If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD. |

### 5.1.4.9 Advanced Chipset Control sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| CPU Bridge Configuration | N/A | Select sub-menu | N/A |
| Northbridge Configuration | N/A | Select sub-menu | N/A |
| Spread Spectrum Clocking Mode | **Enabled**<br>Disabled | Allows BIOS to set Clock Spread Spectrum for EMI (electromagnetic interference) control. | Enabled: Allows setting of Clock Spread Spectrum for EMI control. Disabled: Denies setting of Clock Spread Spectrum for EMI control. |

#### 5.1.4.9.1 CPU Bridge Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| CPU Revision | N/A | Display CPU revision ID. | Show only |
| Current QPI Frequency | N/A | Display Current QPI frequency speed in GT/s | Show only |
| Current Memory Frequency | N/A | Display current memory speed (DDR-3) in MHz | Show only |
| DDR3 2x Refresh Rate | **Disabled**<br>Enabled | | Allows override selection of the DDR3 refresh rate for normal operation.<br>Enabled use the 2x refresh rate for high temperature. Disabled use normal 1x refresh rate. |

#### 5.1.4.9.2 Northbridge Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| NB Revision | N/A | Display Current NB revision ID. | Show only |
| Current QPI Frequency | N/A | Display Current QPI frequency speed in GT/s | Show only |
| Intel QuickData Technology / DMA | **Enabled**<br>Disabled | Enable special setting to made available the Direct Memory Access. | Intel QuickData Technology / Direct Memory Access configuration. |
| Intel QuickData Technology / DCA | **Enabled**<br>Disabled | Enable special setting to made available the Direct Cache Access. | Intel QuickData Technology / Direct Cache Access configuration. |

### *5.1.4.10 Intel VT-d Configuration Sub-Menu*

| Feature | Option | Description | Help text |
|---|---|---|---|
| Intel VT-d | Enabled<br>Disabled | Enable VT-d feature from INTEL. This will add DMAR table in ACPI to allows supporting OS to take advantage of the Virtualization Technology for Directed I/O. | Enabled: allow DMAR table to be present in ACPI table for virtualization.<br>Disabled: DMAR table is not present. |

### *5.1.4.11 I/O Virtualization Sub-Menu*

| Feature | Option | Description | Help text |
|---|---|---|---|
| SR-IOV Supported | **Disabled**<br>Enabled | | Options<br>Disabled<br>Enabled |

## 5.1.5 Security Menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Supervisor Password | Installed<br>Not Installed | Indicates the status of the Supervisor Password. | Indicates the status of the supervisor password. |
| User Password | Installed<br>Not Installed | Indicates the status of the User Password. | Indicates the status of the user password. |
| Set Supervisor Password | Enter | The supervisor password can be installed or changed. | Install or change the supervisor password. |
| Set User Password | Enter | The user password can be installed or changed. | Install or change the user password. |
| Clear User Password | Enter | Immediately clears the User password. | Clears user password. |
| User Access Level | No Access<br>**View Only**<br>Limited<br>Full Access | Controls the user access level to the BIOS Setup utility. Supervisor has full access to the BIOS Setup utility. No Access: Prevents user access to the setup utility. View Only: Allows read only user access to the setup utility i.e. none of the fields can be changed. Limited: Allows limited fields such as date and time to be changed in user access to the setup utility. Full Access: Allows unlimited user access to the setup utility. | Controls access to the setup utility. No Access: Prevents user access. View Only: Allows read only user access. Limited: Allows limited fields to be changed. Full Access: Allows unlimited user access. |
| Execute Disable Bit | Enabled<br>**Disabled** | Execute Disable Bit allows the processor to classify areas in memory by where application code can execute and where it cannot preventing certain classes of malicious buffer overflow attacks when combined with a supporting operating system. | Enabled: Allows processor to prevent application code access to certain memory areas. Needs supporting OS. Disabled: No restrictions to application code memory area access by processor. |

## 5.1.6 Boot Menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Boot Settings Configuration | N/A | Selects sub-menu. | Selects boot settings configuration. |
| Boot Device Priority | N/A | Selects sub-menu. | Selects boot device priority. |
| Hard Disk Drives | N/A | Selects sub-menu. | Lists available hard disk drives in priority order. |
| Removable Drives | N/A | Selects sub-menu. | Lists available removable disk drives in priority |
| CD/DVD Drives | N/A | Selects sub-menu. | Lists available CD/DVD drives in priority order. |
| USB Drives | N/A | Selects sub-menu. | Lists available USB drives in priority order. |
| Network Drives | N/A | Selects sub-menu. | Lists available network drives in priority order. |
| Other Drives | N/A | Selects sub-menu. | Lists available other drives in priority order. |

### 5.1.6.1 Boot Settings Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Quick Boot Mode | **Enabled**<br>Disabled | Allows/denies skipping the memory tests during a cold boot. Quick Boot enabled has no impact on a warm reset boot since then memory is not initialized during a warm reset. | Enabled: Allows skipping the memory tests during a cold boot. Disabled: Allows the extended memory test to be executed during a cold boot. |
| Progressive Boot | Enabled<br>**Disabled** | If disabled, the normal boot path is used.<br>If enabled, IPMI need to be enabled. The OS Load Timeout watchdog will be enabled at time selected by user. If OS load WD is disabled, it will be re-enabled by progressive boot. | Enabled: Allows BIOS to bypass a failing device upon WD bite.<br>Note: If OS Load is set to disable this option will enable WD at 600 seconds. |
| Progressive Boot Action | Reset sequence<br>**Keep booting** | If value is set to Reset sequence, the boot order is reset upon good start from a device without any WD bite.<br>If value is set to Keep booting, the boot sequence keep the failling device and boot from the next. | Reset sequence: Boot sequence is reset after a good start from a device.<br>Keep booting: Boot sequence start from last successful bootable device. |
| Warm Reset Initial count | Never<br>**Always**<br>5<br>10<br>15 | Never does Cold reset. Always always do a warm reset after the first Cold boot. The rest of the option are count for warm reset. | Select the value of the warm reset count. Always: Always do a warm reset. Never: Always do a cold reset. |
| Default Reset Type | Hard Reset<br>Warm Reset | | Sets the reset type issued whenever front panel reset button is pushed or IPMI Watchdog expires with reset action configured. |

### 5.1.6.2 Boot Device Priority sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| 1st Boot Device | Type: Boot device | Specifies the priority of the available boot sources. The list includes USB CD ROM, USB Hard Drive, SAS Hard Drive and PXE. Other supported devices might be dynamically added | Specifies the priority of the available boot sources. |
| ... | | | |
| Nth Boot Device | Type: Boot device | Specifies the boot priority of the available boot sources. The list includes USB CD ROM, USB Hard Drive, SAS Hard Drive and PXE. Other supported devices might be dynamically added | Specifies the priority of the available boot sources. |

### 5.1.6.3 Hard Disk Drives sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| 1st Drive | Varies | Specifies the boot priority of the available Hard Disk devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |
| ... | | | |
| Nth Drive | Varies | Specifies the boot priority of the available Hard Disk devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |

### 5.1.6.4 Removable Drives sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| 1st Drive | Varies | Specifies the boot priority of the available Removable devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |
| ... | | | |
| Nth Drive | Varies | Specifies the boot priority of the available Removable devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |

### 5.1.6.5 CD/DVD Drives sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| 1st Drive | Varies | Specifies the boot priority of the available CD or DVD devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |
| ... | | | |
| Nth Drive | Varies | Specifies the boot priority of the available CD or DVD devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |

### 5.1.6.6 USB Disk Drives sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| 1st Drive | Varies | Specifies the boot priority of the available USB Disk devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |
| ... | | | |
| Nth Drive | Varies | Specifies the boot priority of the available USB Disk devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |

### 5.1.6.7 Network Disk Drives sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| 1st Drive | Varies | Specifies the boot priority of the available Network Disk devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |
| ... | | | |
| Nth Drive | Varies | Specifies the boot priority of the available Network Disk devices. | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |

### 5.1.6.8 All Other Disk Drives sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| 1st Drive | Varies | Specifies the boot priority of any other available devices (other than Hard Disk, Removable, CD/DVD, USB disk or Network). | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |
| ... | | | |
| Nth Drive | Varies | Specifies the boot priority of any other available devices (other than Hard Disk, Removable, CD/DVD, USB disk or Network). | Specifies the boot priority of the available devices. Select the boot device with UpArrow or DownArrow key. Press Enter to set the selection as the intended boot device. |

## 5.1.7 System Management Menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Remote Access Configuration | N/A | Selects sub-menu. | N/A |
| Set LAN Configuration | N/A | Selects sub-menu. | IPMI over LAN (and Serial Over LAN). |
| Watchdog Timers | N/A | Selects sub-menu. | N/A |
| System Information | N/A | Selects sub-menu. | N/A |
| Managed FRU Deactivation Policies | N/A | Selects sub-menu. | N/A |
| OEM e-keying Configuration | N/A | Selects sub-menu. | N/A |

### *5.1.7.1 Remote Access Configuration sub-menu*

| Feature | Option | Description | Help text |
|---|---|---|---|
| Serial Port Number | **COM1**<br>COM2 | Configures serial port for console redirection. Also used for Headless operation mode through ACPI. | Select serial port for console redirection. |
| Serial Port 1 I/O address | 3F8/IRQ4 | Displays the hardware address of the COM 1 port. | N/A, display only. |
| Serial Port 2 I/O address | 2F8/IRQ3 | Displays the hardware address of the COM 2 port i.e. RTM serial port. | N/A, display only. |
| Baud Rate | **115200 8,n,1**<br>57600 8,n,1<br>38400 8,n,1<br>19200 8,n,1<br>9600 8,n,1 | Configures serial port Baud rate for both serial ports. | Select serial port Baud rate. |
| Flow Control | **Hardware**<br>Software<br>None | Configures flow control for console redirection for both serial ports. | Select flow control for console redirection. |
| Terminal Type | **ANSI**<br>VT100<br>VTUTF8 | Configures the type of console emulation used for both serial ports. | Select the typeof console emulation used. |
| Terminal Size | 80x24 | Displays terminal size. | N/A, display only. |

### 5.1.7.2 Set LAN Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Channel Number | 01 or 02 | Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Channels 01 and 02 on Base interface are available. The channel number assignments are described in IPMI Specification 2.0, table 6-1. | Enter Channel Number for SET LAN Config Command. Proper value 01 or 02. |
| Channel Status | Valid or Invalid | Display Valid if IPMC support LAN Channel. | N/A, display only. |
| IP Address | N/A | Selects sub-menu. | Enter for IP Address Configuration. |
| MAC Address | N/A | Selects sub-menu. | Enter for MAC Address Configuration. |
| Subnet Mask | N/A | Selects sub-menu. | Enter for Subnet Mask Configuration. |
| Gateway Address | N/A | Selects sub-menu. | Enter for Gateway IP Address Configuration. |
| VLAN ID | N/A | Selects sub-menu. | Enter for VLAN ID Configuration. |
| VLAN Priority | N/A | Selects sub-menu. | Enter for VLAN Priority Configuration. |
| Active LAN Channel Number | **None**<br>01<br>02<br>Both | Each interface has a channel number that is used when configuring the channel and for routing messages between channels. The channel number assignments are described in IPMI Specification 2.0, table 6-1. | Enter Active LAN Channel Number for Set LAN Configuration Command. |

### 5.1.7.3 IP Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| LAN Parameter Selector | 03 | The parameter selector assignments are described in IPMI Specification 2.0, table 23-4. Selector #03: IP Address. | N/A, display only. |
| Channel Number | 01 or 02 | Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Channels 01 and 02 on Base interface are available. The channel number assignments are described in IPMI Specification 2.0, table 6-1. | Enter Channel Number for SET LAN Config Command. Proper value 01 or 02. |
| Channel Status | Valid or Invalid | Display Valid if IPMC support LAN Channel. | N/A, display only. |
| IP Address Source | Static or DHCP | Select whether IP Address is set Static or retreive using DHCP. | Select IP Address Source: Static or DHCP |
| Current IP Address | xxx.xxx.xxx.xxx | Display the current LAN configuration stored in IPMI NVRAM for IPMI LAN. | N/A, display only. |
| IP Address | xxx.xxx.xxx.xxx | This allows setting an IP Address for LAN configuration when IP Address Source is set to static. This option is hiden when DHCP source is selected. | Enter IP Address in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only). |

### 5.1.7.4 MAC Address Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| LAN Parameter Selector | 05 | The parameter selector assignments are described in IPMI Specification 2.0, table 23-4. Selector #05: MAC Address. | N/A, display only. |
| Channel Number | 01 or 02 | Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Channels 01 and 02 on Base interface are available. The channel number assignments are described in IPMI Specification 2.0, table 6-1. | Enter Channel Number for SET LAN Config Command. Proper value 01 or 02. |
| Channel Status | Valid or Invalid | Display Valid if IPMC support LAN Channel. | N/A, display only. |
| Current MAC Address | xx.xx.xx.xx.xx.x x | Display the current MAC Address stored in IPMI NVRAM for IPMI LAN. | N/A, display only. |

### 5.1.7.5 Subnet Mask Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| LAN Parameter Selector | 06 | The parameter selector assignments are described in IPMI Specification 2.0, table 23-4. Selector #06: Subnet Mask. | N/A, display only. |
| Channel Number | 01 or 02 | Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Channels 01 and 02 on Base interface are available. The channel number assignments are described in IPMI Specification 2.0, table 6-1. | Enter Channel Number for SET LAN Config Command. Proper value 01 or 02. |
| Channel Status | Valid or Invalid | Display Valid if IPMC support LAN Channel. | N/A, display only. |
| IP Address Source | Static or DHCP | Select whether IP Address is set static or retreive using DHCP. | Select IP Address Source: Static or DHCP |
| Current Subnet Mask | xxx.xxx.xxx.xxx | Display the current Subnet Mask configuration stored in IPMI NVRAM for IPMI LAN. | N/A, display only. |
| Subnet Mask | xxx.xxx.xxx.xxx | This allows setting of a Subnet Mask for LAN configuration when IP Address Source is set to static. This option is hiden when DHCP source is selected. | Enter Subnet Mask in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only). |

### 5.1.7.6 Gateway Address Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| LAN Parameter Selector | 12 | The parameter selector assignments are described in IPMI Specification 2.0, table 23-3. Selector #12: Default Gateway Address. | N/A, display only. |
| Channel Number | 01 or 02 | Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Channels 01 and 02 on Base interface are available. The channel number assignments are described in IPMI Specification 2.0, table 6-1. | Enter Channel Number for SET LAN Config Command. Proper value 01 or 02. |
| Channel Status: | Valid or Invalid | Display Valid if IPMC support LAN Channel. | N/A, display only. |
| IP Address Source | Static or DHCP | Select whether IP Address is set static or retreive using DHCP. | Select IP Address Source: Static or DHCP |
| Current Gateway Address: | xxx.xxx.xxx.xxx | Display the current Gateway configuration stored in IPMI NVRAM for IPMI LAN. | N/A, display only. |
| Gateway Address | xxx.xxx.xxx.xxx | This allows setting an Gateway IP Address for LAN configuration when IP Address Source is set to static. This option is hiden when DHCP source is selected. | Enter Gateway IP Address in decimal in the form of XXX.XXX.XXX.XXX (XXX less than 256 and in decimal only). |

### 5.1.7.7 VLAN ID Configuration

| Feature | Option | Description | Help text |
|---|---|---|---|
| LAN Parameter Selector | 20 | The parameter selector assignments are described in IPMI Specification 2.0, table 23-4. Selector #20: 802.1q VLAN ID (12-bit). | N/A, display only. |
| Channel Number | 01 or 02 | Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Channels 01 and 02 on Base interface are available. The channel number assignments are described in IPMI Specification 2.0, table 6-1. | Enter Channel Number for SET LAN Config Command. Proper value 01 or 02. |
| Channel Status: | Valid or Invalid | Display Valid if IPMC support LAN Channel. | N/A, display only. |
| 802.1q VLAN ID Value | xxx | This allows setting an 802.1q VLAN ID for LAN configuration. | Enter VLAN ID value in decimal. VLAN ID must be between 1 and 4094. |
| Current 802.1q VLAN ID Value: | xxxx | Display the current 801.1q VLAN ID configuration stored in IPMI NVRAM for IPMI LAN. | N/A, display only. |
| Support VLAN Tagged Packets | **Enabled**<br>Disabled | Select if 802.1q VLAN tagged packets are added. | Select if VLAN Tagged Packets are to be added or not. |
| VLAN Tagged Packets Status: | Enabled or Disabled | Display the current status of the 801.1q VLAN tagged packets configuration stored in IPMI NVRAM for IPMI LAN. | N/A, display only. |

### 5.1.7.8 VLAN Priority Configuration

| Feature | Option | Description | Help text |
|---|---|---|---|
| LAN Parameter Selector | 21 | The parameter selector assignments are described in IPMI Specification 2.0, table 23-4. Selector #21: 802.1q VLAN Priority. | N/A, display only. |
| Channel Number | 01 or 02 | Each interface has a channel number that is used when configuring the channel and for routing messages between channels. Channels 01 and 02 on Base interface are available. The channel number assignments are described in IPMI Specification 2.0, table 6-1. | Enter Channel Number for SET LAN Config Command. Proper value 01 or 02. |
| Channel Status: | Valid or Invalid | Display Valid if IPMC support LAN Channel. | N/A, display only. |
| 802.1q VLAN Priority Value | x | This allows setting an 802.1q VLAN priority for LAN configuration. | Enter VLAN Priority value in decimal. Proper value below 8. |
| Current VLAN Priority Value: | x | Display the current 801.1q VLAN Priority configuration stored in IPMI NVRAM for IPMI LAN. | N/A, display only. |

### 5.1.7.9 Watchdog Timer sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| BIOS POST Timeout | Disabled<br>60<br>120<br>**150**<br>300<br>600 | Configures the BIOS POST IPMI HW watchdog timeout value in seconds. The BIOS POST watchdog will be disabled if the timeout value is set 0. | Select the BIOS POST IPMI HW watchdog timeout value. |
| BIOS POST Action | No Action<br>**Hard Reset**<br>Power Down<br>Power Cycle | Configures which action to take when the BIOS POST IPMI HW watchdog expires. | Select which action to take when the BIOS POST IPMI HW watchdog expires. |
| OS Load Timeout | **Disabled**<br>15<br>30<br>45<br>60<br>90<br>120<br>150<br>300<br>600 | Configures the OS Load IPMI HW watchdog timeout value in seconds. The OS Load watchdog will be disabled if the timeout value is set 0. | Select the OS Load IPMI HW watchdog timeout value. |
| OS Load Action | No Action<br>**Hard Reset**<br>Power Down<br>Power Cycle | Configures which action to take when the OS Load IPMI HW watchdog expires. | Select which action to take when the OS Load IPMI HW watchdog expires. |

### 5.1.7.10 System Information sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Board Product Name | AT8050 | Displays the CPU blade product name. | N/A, display only. |
| Board Vendor | Kontron | Displays CPU blade vendor. | N/A, display only. |
| Board Serial Number | Varies | Displays the CPU blade serial number. | N/A, display only. |
| Board Part Number | Varies | Displays the CPU blade part number. | N/A, display only. |
| Chassis Slot | 1..16 | Displays the current chassis slot number for the CPU blade. | N/A, display only. |
| BIOS In Use | Primary<br>Secondary | Displays the current BIOS device in use (primary or secondary). | The current BIOS device in use (primary or secondary). |
| IPMI Device and FW Info | N/A | Selects sub-menu. | N/A, display only. |

### 5.1.7.11 IPMI Device and FW Info sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| IPMI Version | 2.0 | Displays IPMI Specification version. | N/A, display only. |
| IPMI Device ID | Varies | Displays IPMI device ID. OEM defined, IPMI Device ID has been assigned like this: Renesas H8S2148 = 1 Kontron PMM = 2 Renesas H8S2145 = 3 Renesas H8S2166 = 4 Renesas H8S2138 = 5 Renesas H8S2168 = 6 Renesas H8S2472 = 7 | N/A, display only. |
| IPMI Device Revision | Varies | Displays IPMI device revision. OEM defined, specify the version of the IPMI Device controller. | N/A, display only. |
| IPMI Firmware Version | Varies | Displays IPMI firmware version. | N/A, display only. |
| SDR Revision | Varies | Displays SDR (Sensor Data Record) revision. This field correspond to the implementation specific auxiliary information from IPMI "Get Device ID Command", byte 13. The SDR revision is displayed in decimal notation. | N/A, display only. |
| Maintenance Revision | Varies | Displays Maintenance revision. This field correspond to the implementation specific auxiliary information from IPMI "Get Device ID Command", byte 15. The byte is displayed as a 2-digit hexadecimal number. | N/A, display only. |
| Aux Revision Info byte 0 | Varies | Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 13. The byte is displayed as a 2-digit hexadecimal number. | N/A, display only. |
| Aux Revision Info byte 1 | Varies | Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 14. The byte is displayed as a 2-digit hexadecimal number. | N/A, display only. |
| Aux Revision Info byte 2 | Varies | Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 15. The byte is displayed as a 2-digit hexadecimal number. | N/A, display only. |
| Aux Revision Info byte 3 | Varies | Displays implementation specific auxiliary information from IPMI "Get Device ID Command", byte 16. The byte is displayed as a 2-digit hexadecimal number. | N/A, display only. |

### 5.1.7.12 OEM e-keying Configuration sub-menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| PCI Express SSC Setting | Enabled<br>Disabled | PCI Express Spread Spectrum Clock Mode support can be SSC/Non-SSC. | Select the PCI Express Spread Spectrum Clock "SSC" Mode. Warning! Re-insert the blade after changing the PCI Express Clock Mode. This is used for AMC.1 module e-keying. |
| PCI Express SSC State | Enabled<br>Disabled | Display actual AMC PCI Express Spread Spectrum Clock Mode. | N/A |
| Upd. Channel Override Setting | Disabled<br>Auto<br>Enabled | Route Update Channel PCI Express. | Disabled: disable PCIe port and PCIe clock. Enabled: enable PCIe port and PCIe clock Auto: enable PCIe based on e-keying. Warning! Reinsert the blade after changing settings. |
| Upd. Channel Override State | Disabled<br>Auto<br>Enabled | Display actual Update Channel PCI Express Routting. | N/A |
| Management LAN Setting | Disabled<br>Front Panel<br>AMC.2 Module<br>RTM<br>Fabric Interface | Route Management LAN to the selected destination. | Selects where the Management LAN ports are routed. Warning! Reinsert the blade after changing settings. |
| Management LAN State | Disabled<br>Front Panel<br>AMC.2 Module<br>RTM<br>Fabric Interface | Display actual Management LAN Routing. | N/A |
| AMC P8-11 Setting | Disabled<br>Fabric Interface | Route AMC port 8-11 to Fabric or disable. | Disabled: AMC.2 module is not connected to Fabric Interface. FI: allow AMC.2 module connection to FI. When this option is enabled, the i82599EB cannot be used on the FI.Warning! Re-insert the blade after changing settings. |
| AMC P8-11 State | Disabled<br>Fabric Interface | Display actual AMC Port 8-11 Routing. | N/A |
| RTM Serial Port Setting | CPU COM2<br>AMC P15 | Route AMC port 15 to RTM or disable. | Select which Serial Port is routed to the RTM Serial Port connecter. An e-keying match is required between the AMC and the RTM for the serial link to work. Warning! Re-insert the blade after chaning settings. |

| Feature | Option | Description | Help text |
|---|---|---|---|
| RTM Serial Port State | CPU COM2<br>AMC P15 | Display actual RTM Serial Port Routing. | N/A |
| ICH SATA P0 Setting | Disabled<br>AMC | Route ICH SATA P0 to AMC or disable | Select AMC to connect a SATA disk in the AMC to the ICH controller.<br>Select Disabled to route AMC to the RTM SAS controller. Warning! Re-insert the blade after changing settings. |
| ICH SATA P0 State | Disabled<br>AMC | Display actual ICH SATA P0 Routing. | N/A |
| AMC PCI Express Setting | Disabled<br>Auto | Route AMC PCIe based on e-keying or disabled | Disabled: Disable AMC PCI Express.<br>Auto: Enable AMC PCI Express based on e-keying. Warning! Re-insert the blade after changing settings. |
| AMC PCI Express State | Disabled<br>Auto | Display actual AMC PCI Express | N/A |

### *5.1.7.13 Managed FRU Deactivation Policies sub-menu*

| Feature | Option | Description | Help text |
|---|---|---|---|
| On AMC Deactivation (FRU1) | Deactivate FRU0<br>**Deactivate FRU1** | AMC Deactivation Policy. Deactivate AMC only or Gracefull Shutdown Front Board | Select FRU0 to shutdown the board or FRU1 for AMC. |
| On RTM Deactivation (FRU2) | **Deactivate FRU0**<br>Deactivate FRU2 | RTM Deactivation Policy. Deactivate RTM only or Gracefull Shutdown Front Board | Select FRU0 to shutdown the board or FRU2 for RTM. |
| On RTM Disk Deactivation (FRU3) | **Deactivate FRU0**<br>Deactivate FRU3 | RTM Disk Deactivation Policy. Deactivate RTM Disk only or Gracefull Shutdown Front Board. | Select FRU0 to shutdown the board or FRU3 for RTM disk. |

### 5.1.8 Exit Menu

| Feature | Option | Description | Help text |
|---|---|---|---|
| Exit Saving Changes | N/A | Saves modified settings into non-volatile memory and reboots the system. | Exit system setup saving changes to non-volatile memory. |
| Exit Discarding Changes | N/A | Discards modifications to settings and reverts to the state when Setup was entered, then complete remaining POST. | Exit system setup without saving changes. |
| Load Setup Defaults | N/A | Loads the factory default settings. | Load default settings. |
| Discard Changes | N/A | Discards modifications to settings and reverts to the state when Setup was entered. | Discard changes without exiting setup. |
| Exit & Execute BIOSRollback | N/A | Exits the Setup utility without saving any changes and then performs a Rollback of the on-board BIOS chips. If the currently executing BIOS was the primary BIOS, the system would change to the backup BIOS (and vice versa). | Rollback BIOS without saving any changes. |

## 5.2 Boot Utilities

AMI Boot Utilities are: Boot Menu POP-UP

Boot Menu POP-UP is a boot screen that displays a selection of boot devices from which you can boot your operating system.

### 5.2.1 Entering BIOS Setup Menu

Pressing <DEL> (or <F4> from a console redirection) during POST enters BIOS Setup.

### 5.2.2 Boot Menu POP-UP

Pressing <F11> (or <F3> from a Console Redirection terminal) displays the Boot Menu POP-UP with these options:

1 Load the operating system from a boot device of your choice.

2 Exit the Boot Menu POP-UP (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

### 5.2.3 SAS Option ROM

To access the SAS Option ROM, follow the procedure listed below.

1 Option ROM for SAS needs to be enabled and the RTM must be present.

2 Press "F3" to select the boot device.

3 Press "CTRL-C" during the execution of the option ROM.

4 BIOS mention: "Please wait, invoking SAS Configuration Utility..."

"***LSI Corp Configuration Utility will load after initialization***"

5 Select "SCSI:LSI MPI Boot Support" in Popup menu

The menu is now available.

### 5.2.4 BOOT Menu POP-UP

The BOOT Menu POP-UP expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, CDROM, Flash Disk, SCSI or LAN. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in the Boot device <F11> (or <F3> from a Console Redirection terminal).

## 5.3 Console Redirection (VT100 Mode)

The VT100 operating mode allows remote setup of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

### 5.3.1 Requirements

The terminal should emulate a VT100 or an ANSI terminal. Terminal emulation programs such as Telix©, HyperTherminal(Windows), minicom(Linux) or ProComm©(Windows) can also be used.

### 5.3.2 ANSI and VT100 Keystroke Mapping

| | |
|---|---|
| Up | <ESC>[A |
| Down | <ESC>[B |
| Right | <ESC>[C |
| Left | <ESC>[D |
| Home | <ESC>[H |
| End | <ESC>[K |
| F1 | <ESC>OP |
| F2 | <ESC>OQ |
| F3 | <ESC>OR |
| F4 | <ESC>OT |

## 5.3.3 VT-UTF8 Keystroke Mapping

The following "escape sequences" are defined in the "Conventions for Keys Not in VT100 Terminal Definition and ASCII Character Set" section of "Standardizing Out-of-Band Management Console Output and Terminal Emulation (VT-UTF8 and VT100+)",available for download at microsoft.com.

| | |
|---|---|
| F1 Key | <ESC>1 |
| F2 Key | <ESC>2 |
| F3 Key | <ESC>3 |
| F4 Key | <ESC>4 |
| F5 Key | <ESC>5 |
| F6 Key | <ESC>6 |
| F7 Key | <ESC>7 |
| F8 Key | <ESC>8 |
| F9 Key | <ESC>9 |
| F10 Key | <ESC>0 |
| F11 Key | <ESC>! |
| F12 Key | <ESC>@ |
| Alt Modifier | <ESC>^A |
| Control Modifier | <ESC>^C |
| Home Key | <ESC>h |
| End Key | <ESC>k |
| Insert Key | <ESC>+ |
| Delete Key | <ESC>- |
| Page Up Key | <ESC>? |
| Page Down Key | <ESC>/ |

These "escape sequences" are supported by VT-UTF8 compliant terminal connections, such as Windows Server 2003 Emergency Management Services (EMS).

AMIBIOS8 Serial Redirection supports these key sequences under two configurations:

- "Terminal Type" setup question is set to "VT-UTF8"
- "Terminal Type" setup question is set to "VT100" or "ANSI" and "VTUTF8 Combo Key Support" setup question is set to "Enabled"

*Chapter 6*

# Thermal Considerations

# 6. Thermal Considerations

The following chapter provide system integrators with the necessary information to satisfy thermal and airflow requirements when using the AT8050.

## 6.1 Thermal Monitoring

To ensure optimal operation and long-term reliability of the AT8050, all on-board components must remain within the maximum temperature specifications. The most critical components on the AT8050 are the processor, the memory modules and the chipset. Operating the AT8050 above the maximum operating limits will result in application performance degradation (e.g. the processor might throttles if it overheats) or may even damage the board. To ensure functionality at the maximum temperature, the blade supports several temperature monitoring and control features.

### 6.1.1 Heat Sinks

Multiple key components of the AT8050 are equipped with a specifically designed heat sink to ensure the best possible product for operational stability and long-term reliability. The physical size, shape, and construction of the heat sinks ensure the lowest possible thermal resistance. Moreover, the heat sinks were specifically designed to use forced airflow as found in ATCA systems.

### 6.1.2 Temperature Sensors

The AT8050 is equipped with 21 temperature sensors that are accessible via IPMI. Sensors are precisely positioned near critical components to accurately measure the on-board parts temperature. Temperature monitoring must be exercised to ensure highest possible level of system thermal management. An external system manager constitutes one of the best solution for thermal management, being able to report sensor status to end-user or manage events filters for example.

All sensors available on the AT8050, its RTM and the AMC can carry are listed into the Sensor Data Repository with their thresholds as defined by the PICMG 3.0 specification. The following extract (from the PICMG 3.0 Base Specification) details naming convention for thresholds as well as the meaning of each threshold level.

*IPMI non-critical / PICMG 3.0 minor / telco minor:*

**Temperature is getting closer to operating limit; it is not really a "problem" yet. It's only a warning.**

*IPMI critical / PICMG 3.0 major / telco major:*

**Temperature is at or over normal operating limit, but not in destructive zone. Unit still operating but MTBF might be affected.**

*IPMI non-recoverable / PICMG 3.0 critical/ telco critical:*

**Temperature has reached a destructive level. Device might be damaged.**

Most ATCA chassis react to temperature events in the following manner: When a minor threshold is reached, the shelf manager will incrementally increase airflow (fan speed) to bring the temperature below the crossed threshold. When a major threshold is reached, the shelf manager will increase the fans to maximum speed. When a critical threshold is reached, the shelf manager will shutdown the blade to prevent damage. The shelf alarm panel, when available, can inform the operator with LEDs when an alarm (minor, major, critical) is raised. Refer to your chassis documentation to adapt and optimize your temperature monitoring application to chassis capabilities. See also System Airflow section for more information.

Below is the list of temperature sensors with their respective thresholds.

Table 6-1:Temperature Sensors Thresholds

| Sensor ID | Lower Thresholds | | | Upper Thresholds | | |
|---|---|---|---|---|---|---|
| | **Minor** | **Major** | **Critical** | **Minor** | **Major** | **Critical** |
| Temp -48V A Feed | N/A | 0°C | -10°C | +75°C | +85°C | +110°C |
| Temp -48V B Feed | N/A | 0°C | -10°C | +75°C | +85°C | +110°C |
| Temp Mez 12V Out | N/A | 0°C | -10°C | +75°C | +85°C | +110°C |
| Temp CPU | +5°C | 0°C | -10°C | +77°C | TCC-5°C | +125°C |
| Temp Vcore | -35°C | -40°C | -50°C | +75°C | +85°C | +95°C |
| Temp VDDQ | -35°C | -40°C | -50°C | +75°C | +85°C | +95°C |
| Temp IOH | +10°C | +5 | -5°C | +75°C | +85°C | +95°C |
| Temp ICH | +5°C | 0°C | -10°C | +85°C | +95°C | +105°C |
| Temp Mngt Lan | +5°C | 0°C | -10°C | +90°C | +100°C | +110°C |
| Temp BI Lan | +5°C | 0°C | -10°C | +90°C | +100°C | +110°C |
| Temp FI Lan | +5°C | 0°C | -10°C | +90°C | +100°C | +110°C |
| Temp IPMC | +5°C | 0°C | -10°C | +90°C | +100°C | +110°C |
| Temp Bay Inlet | +5°C | 0°C | -10°C | +75°C | +85°C | +95°C |
| Temp DIMM#1 (Channel 0, Dimm0) | +5°C | 0°C | -10°C | +75°C | +85°C | +95°C |
| Temp DIMM#2 (Channel 0, Dimm1) | +5°C | 0°C | -10°C | +75°C | +85°C | +95°C |
| Temp DIMM#3 (Channel1, Dimm0) | +5°C | 0°C | -10°C | +75°C | +85°C | +95°C |
| Temp DIMM#4 (Channel 1, Dimm1) | +5°C | 0°C | -10°C | +75°C | +85°C | +95°C |
| Temp DIMM#5 (Channel 2, Dimm0) | +5°C | 0°C | -10°C | +75°C | +85°C | +95°C |
| Temp DIMM#6 (Channel 2, Dimm1) | +5°C | 0°C | -10°C | +75°C | +85°C | +95°C |

### 6.1.3 Airflow blockers

It is highly recommended to use airflow blockers (ATCA slot) and AMC airflow blocker in the AT8050 (or any empty AMC slot) to block any slot open to exterior air. Failure to do so would go against forced air principles applied on ATCA components, reducing system's cooling efficiency. Moreover, airflow blockers offer a higher impedance to forced air than typical board, who tend to let more air into slots filled with AT8050 or other ATCA boards.

### 6.1.4 System Airflow

The airflow impedance (pressure) curve gives multiple information and tips about thermal operational range of the system carrying the AT8050. Once volumetric airflow capability of your chassis is known, the PQ curve can help determine the ambient (room) temperature setpoint that should be used for optimal operation. If you are using various models of ATCA blades into the same chassis, it is possible to find the best thermal fit. Having the volumetric airflow value for each chassis slot, is it then possible to decide the layout using the pressure curves.

Table 6-2:Pressure curve AT8050 with AMC Filler

| Test Poin | Airflow (CFM) | Pressure drop (in H20) | Airflow (m³/h) | Pressure Drop (Pa) |
|---|---|---|---|---|
| 1 | 12,04 | 0,038 | 20,46 | 9,57 |
| 2 | 15,03 | 0,048 | 25,54 | 12,02 |
| 3 | 21,02 | 0,069 | 34,00 | 17,28 |
| 4 | 25,00 | 0,100 | 42,48 | 24,91 |
| 5 | 30,01 | 0,142 | 50,99 | 35,26 |
| 6 | 35,02 | 0,195 | 59,50 | 48,61 |
| 7 | 40,02 | 0,257 | 68,00 | 64,07 |
| 8 | 45,06 | 0,321 | 76,55 | 79,95 |
| 9 | 50,01 | 0,381 | 84,97 | 95,00 |

Figure 6-1:Pressure Curve in Imperial

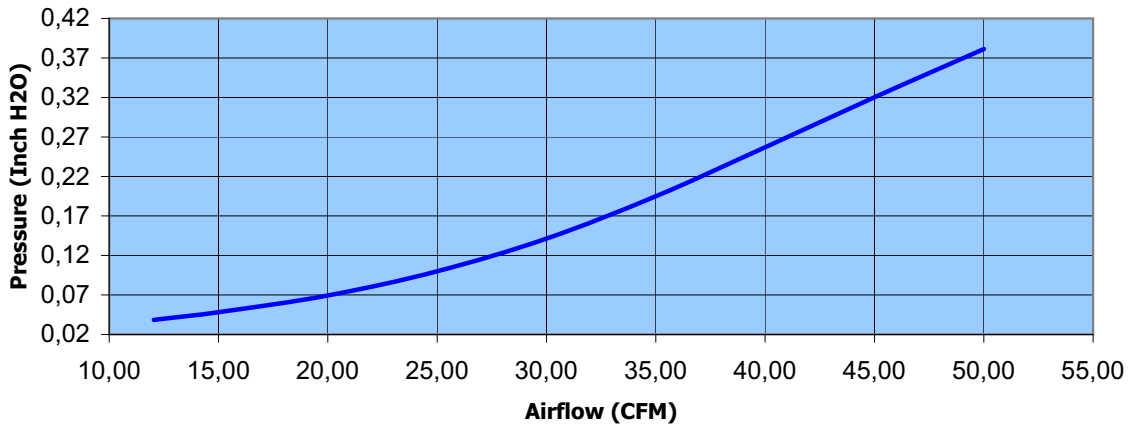
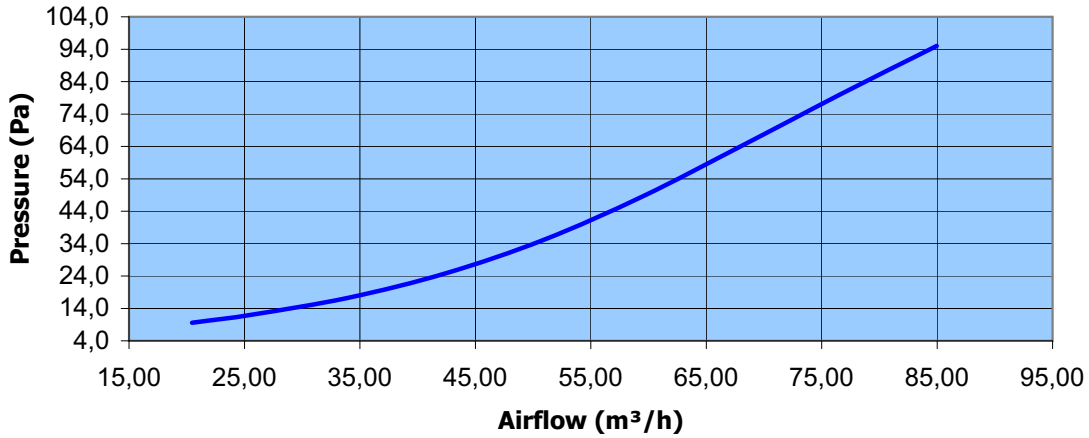


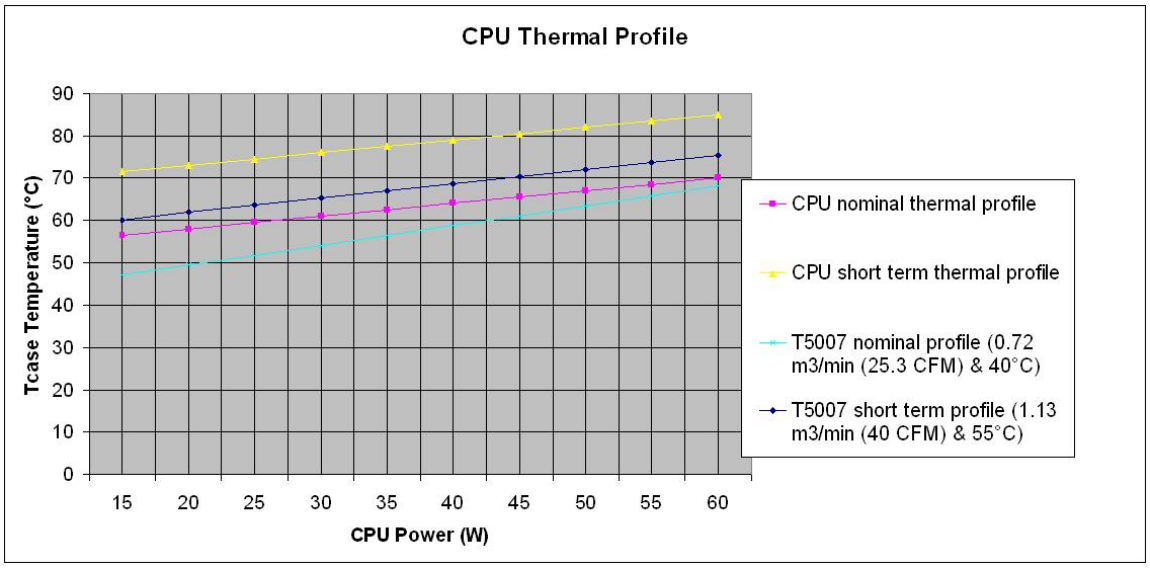
Figure 6-2:Pressure Curve in Metric




## 6.1.5 Thermal Profile

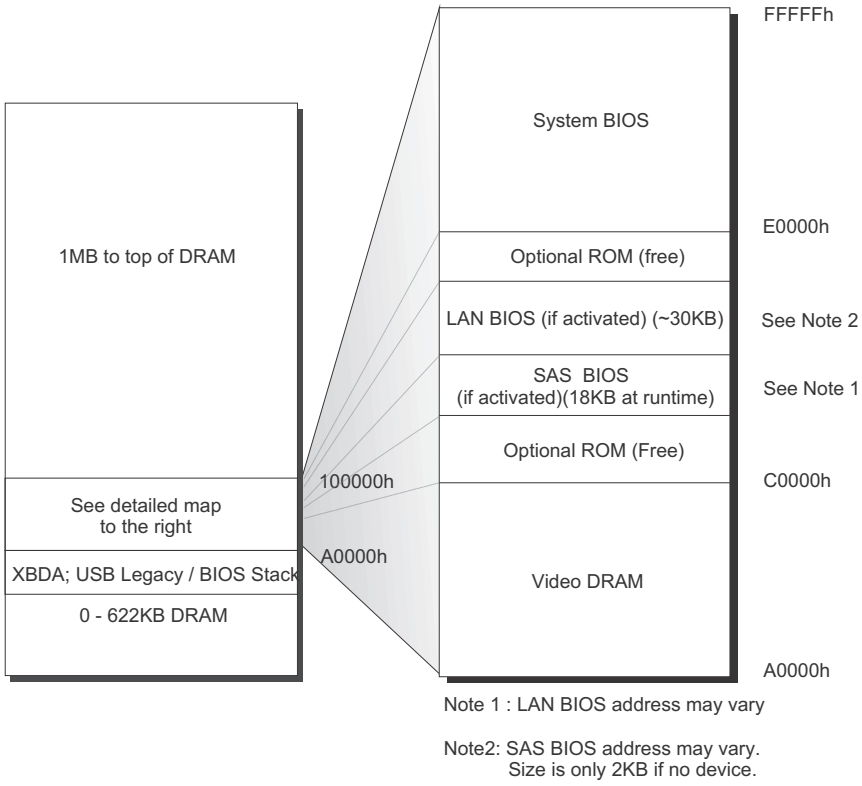
It is important to follow the thermal profile to make sure the MTBF values are respected. The CPU usage will influence the temperature that the case can handle. Refer to the figure below for more details.

Figure 6-3:CPU Thermal Profile



# A. Memory & I/O Maps

## A.1 Memory Mapping




| Address | Function |
|---|---|
| 00000-9B7FF | 0-622 KB DRAM |
| 9B800-9FFFF | 622KB - 640 KB XBDA; USB Legacy / BIOS Stack |
| A0000-BFFFF | Video DRAM |
| C0000-DBFFF | Optional ROM (Free)<br>LAN BIOS around 30KB if activated, address may vary<br>External Fiber Channel BIOS 18KB-64KB , address may vary |
| E0000-FFFFF | System BIOS |
| 100000-PCI Memory | DRAM available |

# A.2 Kontron I/O Mapping

| Address | Optional Address | Function |
|---|---|---|
| 000-01F | | DMA Controller 1 |
| 020-03F | | Interrupt Controller 1 |
| 040-05F | | Timer |
| 060-06F | | Keyboard |
| 070-07F | | Real-time clock |
| 080-09F | | DMA Page Register |
| 0A0-0BF | | Interrupt Controller 2 |
| 0C0-0DF | | DMA Controller 2 |
| 0F0-0F1, 0F8-0FF | | Math Coprocessor |
| 1F0-1F7, 3F6 | | Primary IDE |
| 170-177, 376 | | Secondary IDE |
| 378-37F | | Parallel Port (Used as PLD POD) |
| 3F8-3FF (COM1) | | Serial Port 1 (COM1 by default) |
| 2F8-2FF (COM2) | | Serial Port 2 (COM2 by default) |
| 400-7FF | | Chipset Reserved |
| 800-9FF | | Chipset Reserved |
| A00-A1F | | Kontron Registers (on-board) |

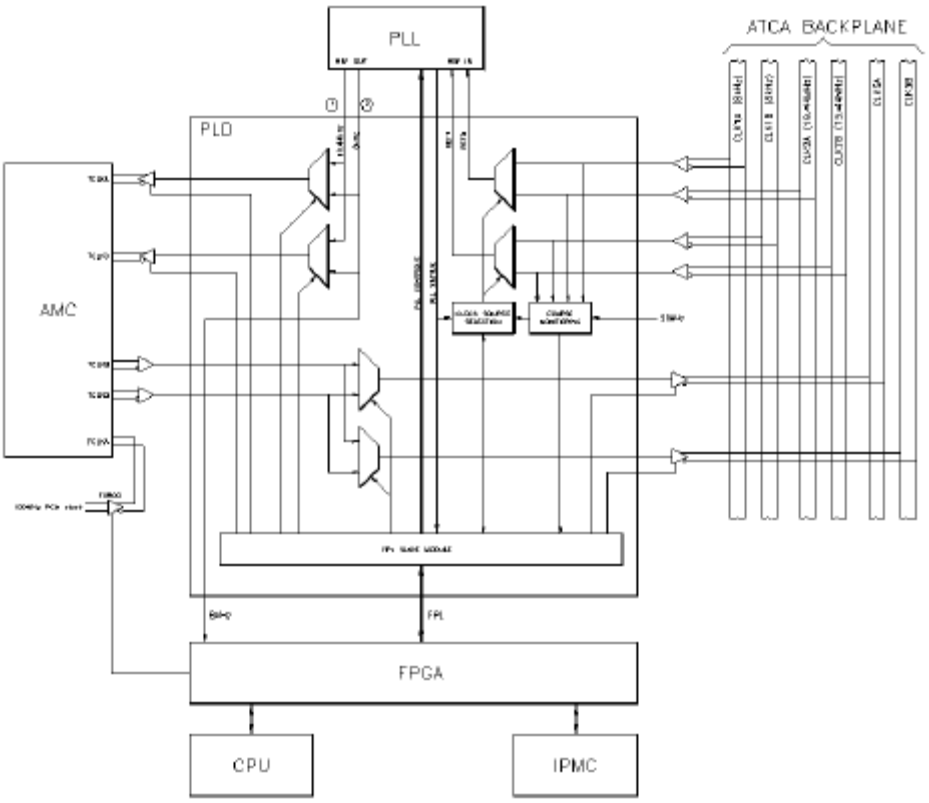
# A.3 PCI IDSEL and Device Numbers

| BUS# | DEV# | V. ID | D. ID | Funct. # | Description | PCI Description |
|---|---|---|---|---|---|---|
| 00 | 00 | 8086 | 3406 | 0 | Intel Corporation QuickPath Architecture I/O Hub to ESI Port (rev 10) | IOH |
| 00 | 01 | 8086 | | 0 | Intel Corporation QuickPath Architecture I/O Hub PCI Express Root Port 1 (rev 10) | IOH |
| 00 | 03 | 8086 | 340a | 0 | Intel Corporation QuickPath Architecture I/O Hub PCI Express Root Port 3 (rev 10) | IOH |
| 00 | 04 | 8086 | 340b | 0 | Intel Corporation QuickPath Architecture I/O Hub PCI Express Root Port 4 (rev 10) | IOH |
| 00 | 05 | 8086 | 340c | 0 | Intel Corporation QuickPath Architecture I/O Hub PCI Express Root Port 5 (rev 10) | IOH |
| 00 | 07 | 8086 | 340e | 0 | Intel Corporation QuickPath Architecture I/O Hub PCI Express Root Port 7 (rev 10) | IOH |
| 00 | 08 | 8086 | 340f | 0 | Intel Corporation QuickPath Architecture I/O Hub PCI Express Root Port 8 (rev 10) | IOH |
| 00 | 09 | 8086 | 3410 | 0 | Intel Corporation QuickPath Architecture I/O Hub PCI Express Root Port 9 (rev 10) | IOH |
| 00 | 0a | 8086 | 3411 | 0 | Intel Corporation QuickPath Architecture I/O Hub PCI Express Root Port 10 (rev 10) | IOH |
| 00 | 10 | 8086 | 3425 | 0 | Intel Corporation QuickPath Interconnect Physical and Link Layer Registers Port 0 (rev 10) | IOH |
| 00 | 10 | 8086 | 3426 | 1 | Intel Corporation QuickPath Interconnect Routing and Protocol Layer Registers Port 0 (rev 10) | IOH |
| 00 | 11 | 8086 | 3427 | 0 | Intel Corporation QuickPath Interconnect Physical and Link Layer Registers Port 1 (rev 10) | IOH |
| 00 | 11 | 8086 | 3428 | 1 | Intel Corporation QuickPath Interconnect Routing and Protocol Layer Registers Port 1 (rev 10) | IOH |
| 00 | 14 | 8086 | 342e | 0 | Intel Corporation QuickPath Architecture I/O Hub System Management Registers (rev 10) | IOH |
| 00 | 14 | 8086 | 3422 | 1 | Intel Corporation QuickPath Architecture I/O Hub GPIO and Scratch Pad Registers (rev 10) | IOH |
| 00 | 14 | 8086 | 3423 | 2 | Intel Corporation QuickPath Architecture I/O Hub Control Status and RAS Registers (rev 10) | IOH |
| 00 | 14 | 8086 | 3438 | 3 | Intel Corporation QuickPath Architecture I/O Hub Throttle Registers (rev 10) | IOH |
| 00 | 16 | 8086 | 3430 | 0 | Intel Corporation DMA Engine (rev 10) | IOH |
| 00 | 16 | 8086 | 3431 | 1 | Intel Corporation DMA Engine (rev 10) | IOH |
| 00 | 16 | 8086 | 3432 | 2 | Intel Corporation DMA Engine (rev 10) | IOH |
| 00 | 16 | 8086 | 3433 | 3 | Intel Corporation DMA Engine (rev 10) | IOH |
| 00 | 16 | 8086 | 3429 | 4 | Intel Corporation DMA Engine (rev 10) | IOH |
| 00 | 16 | 8086 | 342a | 5 | Intel Corporation DMA Engine (rev 10) | IOH |
| 00 | 16 | 8086 | 342b | 6 | Intel Corporation DMA Engine (rev 10) | IOH |
| 00 | 16 | 8086 | 342c | 7 | Intel Corporation DMA Engine (rev 10) | IOH |
| 00 | 1d | 8086 | 3a34 | 0 | Intel Corporation ICH10 USB UHCI Controller #1 | ICH |
| 00 | 1d | 8086 | 3a35 | 1 | Intel Corporation ICH10 USB UHCI Controller #2 | ICH |
| 00 | 1d | 8086 | 3a36 | 2 | Intel Corporation ICH10 USB UHCI Controller #3 | ICH |

| BUS# | DEV# | V. ID | D. ID | Funct. # | Description | PCI Description |
|---|---|---|---|---|---|---|
| 00 | 1d | 8086 | 3a3a | 7 | Intel Corporation ICH10 USB2 EHCI Controller #1 | ICH |
| 00 | 1e | 8086 | 244e | 0 | Intel Corporation 82801 PCI Bridge (rev 90) | ICH |
| 00 | 1f | 8086 | 3a16 | 0 | Intel Corporation ICH10 LPC Interface Controller | ICH |
| 00 | 1f | 8086 | 3a22 | 2 | Intel Corporation ICH10 6 port SATA AHCI Controller | ICH |
| 00 | 1f | 8086 | 3a30 | 3 | Intel Corporation ICH10 SMBus Controller | ICH |
| 02 | 00 | 8086 | 10c9 | 0 | Intel Corporation 82576 Gigabit Network Connection | I82576 on Base Interface |
| 02 | 00 | 8086 | 10c9 | 0 | Intel Corporation 82576 Gigabit Network Connection | I82576 on Base Interface |
| 03 | 00 | 8086 | 10d8 | 0 | Intel Corporation 82599 Gigabit Network Connection | I82599 on Fabric Interface |
| 03 | 00 | 8086 | 10d8 | 1 | Intel Corporation 82599 Gigabit Network Connection | I82599 on Fabric Interface |
| 04 | 00 | 8086 | 10c9 | 0 | Intel Corporation 82576 Gigabit Network Connection | I82576 on Management LAN |
| 04 | 00 | 8086 | 10c9 | 1 | Intel Corporation 82576 Gigabit Network Connection | I82576 on Management LAN |
| 06 | 00 | | | 0 | | RTM |
| 0f | 00 | | | 0 | | AMC |
| 18 | 00 | | | 0 | | Update Channel |

# A.4 Telco Clock

Clock Circuit Overview



## A.4.1 Register Description

### *A.4.1.1 Base + 00h TelClock0: Backplane Clock Status, PLL Reference & Interface Selection*

| Offset | Action | D7 | D6 | D6 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 00h | Read | IFSEL | MAN | SEL_REFA | BP_REF | CLK2B | CLK2A | CLK1B | CLK1A |
| | Write | IFSEL* | MAN | SEL_REFM | BP_REF | NU | NU | NU | NU |
| | Reset | 0 | 0 | 0 | 0 | NA | NA | NA | NA |

| Name | Description |
|---|---|
| IFSEL | Interface selection. This bit is always writable from the IPMC side but on the LPC side, the CPU can only read it.<br>1: IPMC has write control of the interface<br>0: Main CPU (LPC) has write control of the interface |
| MAN | 0: The PLD chooses automatically the reference used by the DPLL (CLKA or B).<br>1: Selection of the DPLL reference is manual. Write the selection in bit SEL_REF. |
| SEL_REFA<br>SEL_REFM | On a read, return the reference automatically selected by the CPLD:<br>0: REF0 is the reference used by the PLL (i.e. CLKA)<br>1: REF1 is the reference used by the PLL (i.e. CLKB)<br><br>When bit MAN=1, the application software can select the reference by writing the desired value in this bit. This bit is not writtable when MAN=0. Note that on a read, this bit returns the automatic selection event if MAN=1. |
| BP_REF | Backplane selection of clock to connect to the PLL.<br>0: Use backplane CLK1A and CLK1B (8kHz)<br>1: Use backplane CLK2A and CLK2B (19.44MHz) |
| CLK1A/B<br>CLK2A/B | Coarse monitoring status. A1 indicate that the corresponding backplane clock is present. A0, that it is absent. Those statuses are valid only if CLK1A/B is 8kHz and CLK2A/B is 19.44MHz. If other frequencies are used, those bits should be ignored. |

### A.4.1.2 Base + 01h TelClock1: PLL Control & Status

| Offset | Action | D7 | D6 | D6 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 01h | Read | LOCK | FAIL1 | FAIL0 | 0 | TIE_CLR# | MODE | RESET | OOR |
| | Write | NU | NU | NU | NU | TIE_CLR# | MODE | RESET | OOR |
| | Reset | NA | NA | NA | NA | 1 | 1 | 0 | 0 |

| Name | Description |
|---|---|
| LOCK | PLL lock status.<br>1: PLL locked<br>0: PLL not locked (PLL in holdover or free running) |
| FAIL1 | REF1 (CLK1B or CLK2B according to BP_REF) failed with current OOR setting. Same as FAIL0 but for REF1. |
| FAIL0 | REF0 (CLK1A or CLK2A according to BP_REF) failed with current OOR setting.<br>1: failed clock.<br>0: passed clock. |
| TIE_CLR# | Timing-Interval-Error adjustement.<br>1: normal mode.<br>0: adjust phase to match reference. |
| MODE | PLL operating mode.<br>1: freerun mode(may be used for tests).<br>0: normal mode. |
| RESET | Hardware reset of the PLL. This bit is forced to '1' when the payload power (i.e. PLL power) is turned off.<br>1: reset<br>0: normal operation |
| OOR | OUT-OF-Range selection. Determine what is considered a precision fault by the PLL.<br>1: 64 - 83ppm.<br>0: 40 - 52ppm. |

**Note:**
This register needs to be reprogrammed every time the blade is resetted. Those are direct pin control and status. See the ZL30108 datasheet for a detailed explanation of the functionality.

### A.4.1.3 Base + 02h TelClock2: AMCs Clock Enables & Frequency Selection

| Offset | Action | D7 | D6 | D6 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 02h | Read | B2TCF | B2TAF | B2TCEN | B2TAEN | B1TCF | B1TAF | B1TCEN | B1TAEN |
| | Write | B2TCF | B2TAF | B2TCEN | B2TAEN | B1TCF | B1TAF | B1TCEN | B1TAEN |
| | Reset | 0 | 0 | 0* | 0* | 0 | 0 | 0* | 0* |

| Name | Description |
|---|---|
| B2* | Reserved for AMC-B2 (for board that have two AMCs). |
| B1TCF | AMC-B1 TCLK Frequency<br>1: use 8kHz frame pulse from PLL<br>0: use 19.44MHz from PLL |
| B1TAF | AMC-B1 TCLKA Frequency<br>1: use 8kHz frame pulse from PLL<br>0: use 19.44MHz from PLL |
| B1TCEN | AMC-B1 TCLKC Enable. This bit is forced to 0 when the AMC is in fault or removed.<br>1: drive AMC-B1 clock TCLKC<br>0: don't drive AMC-B1 TCLKC |
| B1TAEN | AMC-B1 TCLKA Enable. this bit is forced to 0 when the AMC is in fault or removed.<br>1: drive AMC-B1 clock TCLKA<br>0: don't drive AMC-B1 TCLKA |

**Note:**

If the clock source of the PLL is 19.44MHz, the phase of this clock is unrelated to any other 8kHz clock in the system.

The AMC has to be present and fully powered for the enable bits to be settable. On a unexpected extraction (user doesn't wait for the blue LED), the hardware automatically clears bits B1TCEN and B1TAEN in case a user would extract and re-insert immediatly the AMC.

### A.4.1.4 Base + 03h TelClock3: PLD Configuration & Version

| Offset | Action | D7 | D6 | D6 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 03h | Read | PLD_CONFIG | | | | PLD_VERSION | | | |
| | Write | NA | | | | | | | |
| | Reset | NA | | | | | | | |

| Name | Description |
|---|---|
| CONFIG | Circuit configuration that the PLD expect. For the interface and circuit described in this document, this field is away 0000. If the PLD is abscent or not programmed, this field will return 0000. |
| VERSION | Code version of the PLD for the above configuration. If the PLD is absent or not programmed, this field will return 0000. |

### A.4.1.5 Base + 04h TelClock4: Backplane CLK3A/B configuration (optional)

| Offset | Action | D7 | D6 | D6 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 04h | Read | 0 | 0 | 0 | 0 | CLK3AMC | CLK3FRQ | CLK3BE | CLK3AE |
| | Write | NU | NU | NU | NU | CLK3AMC | CLK3FRQ | CLK3BE | CLK3AE |
| | Reset | NA | NA | NA | NA | 0 | 0 | 0 | 0 |

| Name | Description |
|---|---|
| CLK3AMC | Reserved for selection of the AMC that provides the clock for backplane CLK3A/B.<br>Applicable tot boards with two AMCs.<br>0: use AMC-B1<br>1: use AMC-B2 |
| CLK3FRQ | Backplane CLK3A frequency.<br>0: copy AMC TCKLB to backplane CLK3A/B<br>1: copy AMC TCLKD to backplane CLK3A/B |
| CLK3BE | Same as CLK3AE but to CLK3B |
| CLK3AE | Backplane CLK3A Enable.<br>0: don't drive this clock<br>1: drive this clock |

**Note:**
The FPGA will automatically clear bits CLK3BE and CLK3AE when the AMC is removed since the clock source is not valid anymore.

### A.4.1.6 Base + 05h TelClock5: Clock Events & Alarm (IPMC only)

| Offset | Action | D7 | D6 | D6 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 05h | Read | LOCKE | FAIL1E | FAIL0E | SELREFE | 0 | 0 | 0 | 0 |
| | Write | Clear | Clear | Clear | Clear | NU | NU | NU | NU |
| | Reset | X* | X* | X* | X* | NA | NA | NA | NA |

| Name | Description |
|---|---|
| LACKE | Same as FAIL0 but for the lock status of the PLL. This bit captures the "unlock" state. This would typically be used to generate an alarm. |
| FAIL1E | Same as FAIL0 but for reference 1. |
| FAIL0E | This bit captures the assertion of a failure on reference 0 on the PLL. This is basically a short failure detection that the IPMC would otherwise miss. Use Telco+1 to read the current state. To Clear this bit, write a 1 in it. The bit will be cleared even if there is still a fauld on this clock. |
| SELREFE | Same as FAIL0 but for the selected reference. This bit goes to one everytime the selected reference changes. This is just to inform the software that a reference change occured. |

**Note:**

* unpredictable: need to be cleared by IPMC on power up.

Events and alarms are implemented in the FPGA. The FPGA build them using the raw signals from the first three registers.

Note that this register is only available on the IPMC side of the interface.

# B. Connector Pinouts

## B.1 Connectors and Headers Summary

| Connector | Description |
|---|---|
| J2 | PostCodes |
| J5 | AMC |
| J8 | Ethernet Port 0 |
| J9 | Ethernet Port 1 |
| J10 | USB (2x Stacked) |
| J12 | Serial Port, COM1 |
| J20 | Synchronisation Clocks, Update Channel |
| J22 | USB Flash Drive |
| J23 | Base Interface & Fabric Intercface |
| J30 | RTM |
| P10 | Power & IPMB |

## B.2 Post Codes (J2)

| Signal | Pin |
|---|---|
| VCC3 | 1 |
| POST:DATA | 2 |
| POST:CLOCK | 3 |
| GND | 4 |

# B.3 AMC B1 (J5)

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| B1 | GND | B43 | GND | B86 | GND | B129 | TxD15- |
| B2 | 12V | B44 | RxD4+ | B87 | TxD8- | B130 | TxD15+ |
| B3 | PS1# | B45 | RxD4- | B88 | TxD8+ | B131 | GND |
| B4 | MP_3V3 | B46 | GND | B89 | GND | B132 | RxD15- |
| B5 | GA0 | B47 | TxD4+ | B90 | RxD8- | B133 | RxD15+ |
| B6 | RSV | B48 | TxD4- | B91 | RxD8+ | B134 | GND |
| B7 | GND | B49 | GND | B92 | GND | B135 | TxD16- |
| B8 | RSV | B50 | RxD5+ | B93 | TxD9- | B136 | TxD16+ |
| B9 | 12V | B51 | RxD5- | B94 | TxD9+ | B137 | GND |
| B10 | GND | B52 | GND | B95 | GND | B138 | RxD16- |
| B11 | RxD0+ | B53 | TxD5+ | B96 | RxD9- | B139 | RxD16+ |
| B12 | RxD0- | B54 | TxD5- | B97 | RxD9+ | B140 | GND |
| B13 | GND | B55 | GND | B98 | GND | B141 | TxD17- |
| B14 | TxD0+ | B56 | IPMB-L-SCL | B99 | TxD10- | B142 | TxD17+ |
| B15 | TxD0- | B57 | 12V | B100 | TxD10+ | B143 | GND |
| B16 | GND | B58 | GND | B101 | GND | B144 | RxD17- |
| B17 | GA1 | B59 | RxD6+ | B102 | RxD10- | B145 | RxD17+ |
| B18 | 12V | B60 | RxD6- | B103 | RxD10+ | B146 | GND |
| B19 | GND | B61 | GND | B104 | GND | B147 | TxD18- |
| B20 | RxD1+ | B62 | TxD6+ | B105 | TxD11- | B148 | TxD18+ |
| B21 | RxD1- | B63 | TxD6- | B106 | TxD11+ | B149 | GND |
| B22 | GND | B64 | GND | B107 | GND | B150 | RxD18- |
| B23 | TxD1+ | B65 | RxD7+ | B108 | RxD11- | B151 | RxD18+ |
| B24 | TxD1- | B66 | RxD7- | B109 | RxD11+ | B152 | GND |
| B25 | GND | B67 | GND | B110 | GND | B153 | TxD19- |
| B26 | GA2 | B68 | TxD7+ | B111 | TxD12- | B154 | TxD19+ |
| B27 | 12V | B69 | TxD7- | B112 | TxD12+ | B155 | GND |
| B28 | GND | B70 | GND | B113 | GND | B156 | RxD19- |
| B29 | RxD2+ | B71 | IPMB-L_SDA | B114 | RxD12- | B157 | RxD19+ |
| B30 | RxD2- | B72 | 12V | B115 | RxD12+ | B158 | GND |
| B31 | GND | B73 | GND | B116 | GND | B159 | TxD20- |
| B32 | TxD2+ | B74 | CLK1+ | B117 | TxD13- | B160 | TxD20+ |
| B33 | TxD2- | B75 | CLK1- | B118 | TxD13+ | B161 | GND |
| B34 | GND | B76 | GND | B119 | GND | B162 | RxD20- |
| B35 | RxD3+ | B77 | CLK2+ | B120 | RxD13- | B163 | RxD20+ |
| B36 | RxD3- | B78 | CLK2- | B121 | RxD13+ | B164 | GND |
| B37 | GND | B79 | GND | B122 | GND | B165 | TCLK (N.C.) |
| B38 | TxD3+ | B80 | CLK3+ | B123 | TxD14- | B166 | TMS (N.C.) |
| B39 | TxD3- | B81 | CLK3- | B124 | TxD14+ | B167 | TRST# (N.C.) |

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| B40 | GND | B82 | GND | B125 | GND | B168 | TDO (N.C.) |
| B41 | ENABLE# | B83 | PS0#(GND) | B126 | RxD14- | B169 | TDI (N.C.) |
| B42 | 12V | B84 | 12V | B127 | RxD14+ | B170 | GND |
| | | B85 | GND | B128 | GND | | |

## B.4 Ethernet (J8 & J9)

| Signal | Pin | | Pin | Signal |
|---|---|---|---|---|
| BI_DA+ | 1 | | 5 | BI_DC- |
| BI_DA- | 2 | | 6 | BI_DB- |
| BI_DB+ | 3 | | 7 | BI_DD+ |
| BI_DC+ | 4 | | 8 | BI_DD- |

## B.5 USB Port (J10)

| Signal | Pin |
|---|---|
| VCC | 1 |
| DATA- | 2 |
| DATA+ | 3 |
| GND | 4 |

## B.6 Serial Port, COM1 (J12)

| Signal | Pin | | Pin | Signal |
|---|---|---|---|---|
| RTS | 1 | | 5 | GND |
| DTR | 2 | | 6 | RX# |
| TX# | 3 | | 7 | DSR |
| GND | 4 | | 8 | CTS |

# B.7 Synchronisation Clocks, Update Channel (J20)

| Pin | ROW A | ROW B | ROW C | ROW D | ROW E | ROW F |
|---|---|---|---|---|---|---|
| 1 | CLK1A+ | CLK1A- | CLK1B+ | CLK1B- | CLK2A+ | CLK2A- |
| 2 | Tx4(UP)+ | Tx4(UP)- | Rx4(UP)+ | Rx4(UP)- | CLK3A+ | CLK3A- |
| 3 | Tx2(UP)+ | Tx2(UP)- | Rx2(UP)+ | Rx2(UP)- | Tx3(UP)+ | Tx3(UP)- |
| 4 | Tx0(UP)+ | Tx0(UP)- | Rx0(UP)+ | Rx0(UP)- | Tx1(UP)+ | Tx1(UP)- |
| 5 | Tx2[15]+(N.C.) | Tx2[15]-(N.C.) | Rx2[15]+(N.C.) | Rx2[15]-(N.C.) | Tx3[15]+(N.C.) | Tx3[15]-(N.C.) |
| 6 | Tx0[15]+(N.C.) | Tx0[15]-(N.C.) | Rx0[15]+(N.C.) | Rx0[15]-(N.C.) | Tx1[15]+(N.C.) | Tx1[15]-(N.C.) |
| 7 | Tx2[14]+(N.C.) | Tx2[14]-(N.C.) | Rx2[14]+(N.C.) | Rx2[14]-(N.C.) | Tx3[14]+(N.C.) | Tx3[14]-(N.C.) |
| 8 | Tx0[14]+(N.C.) | Tx0[14]-(N.C.) | Rx0[14]+(N.C.) | Rx0[14]-(N.C.) | Tx1[14]+(N.C.) | Tx1[14]-(N.C.) |
| 9 | Tx2[13]+(N.C.) | Tx2[13]-(N.C.) | Rx2[13]+(N.C.) | Rx2[13]-(N.C.) | Tx3[13]+(N.C.) | Tx3[13]-(N.C.) |
| 10 | Tx0[13]+(N.C.) | Tx0[13]-(N.C.) | Rx0[13]+(N.C.) | Rx0[13]-(N.C.) | Tx1[13]+(N.C.) | Tx1[13]-(N.C.) |

| Pin | ROW G | ROW H | ROW AB | ROW CD | ROW EF | ROW GH |
|---|---|---|---|---|---|---|
| 1 | CLK2B+ | CLK2B- | GND | GND | GND | GND |
| 2 | CLK3B+ | CLK3B- | GND | GND | GND | GND |
| 3 | Rx3(UP)+ | Rx3(UP)- | GND | GND | GND | GND |
| 4 | Rx1(UP)+ | Rx1(UP)- | GND | GND | GND | GND |
| 5 | Rx3[15]+(N.C.) | Rx3[15]-(N.C.) | GND | GND | GND | GND |
| 6 | Rx1[15]+(N.C.) | Rx1[15]-(N.C.) | GND | GND | GND | GND |
| 7 | Rx3[14]+(N.C.) | Rx3[14]-(N.C.) | GND | GND | GND | GND |
| 8 | Rx1[14]+(N.C.) | Rx1[14]-(N.C.) | GND | GND | GND | GND |
| 9 | Rx3[13]+(N.C.) | Rx3[13]-(N.C.) | GND | GND | GND | GND |
| 10 | Rx1[13]+(N.C.) | Rx1[13]-(N.C.) | GND | GND | GND | GND |

# B.8 USB Flash Drive(J22)

| Signal | Pin | | Pin | Signal |
|---|---|---|---|---|
| VCC | 1 | | 6 | N.C. |
| N.C. | 2 | | 7 | GND |
| USB_DATA- | 3 | | 8 | N.C. |
| N.C. | 4 | | 9 | |
| USB_DATA+ | 5 | | 10 | RSV |

# B.9 Base Interface & Fabric Intercface (J23)

| Pin | ROW A | ROW B | ROW C | ROW D | ROW E | ROW F |
|---|---|---|---|---|---|---|
| 1 | Tx2[2]+ | Tx2[2]- | Rx2[2]+ | Rx2[2]- | Tx3[2]+ | Tx3[2]- |
| 2 | Tx0[2]+ | Tx0[2]- | Rx0[2]+ | Rx0[2]- | Tx1[2]+ | Tx1[2]- |
| 3 | Tx2[1]+ | Tx2[1]- | Rx2[1]+ | Rx2[1]- | Tx3[1]+ | Tx3[1]- |
| 4 | Tx0[1]+ | Tx0[1]- | Rx0[1]+ | Rx0[1]- | Tx1[1]+ | Tx1[1]- |
| 5 | BI_DA1+ | BI_DA1- | BI_DB1+ | BI_DB1- | BI_DC1+ | BI_DC1- |
| 6 | BI_DA2+ | DI_DA2- | BI_DB2+ | BI_DB2- | DI_DC2+ | BI_DC2- |
| 7 | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. |
| 8 | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. |
| 9 | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. |
| 10 | N.C. | N.C. | N.C. | N.C. | N.C. | N.C. |

| Pin | ROW G | ROW H | ROW AB | ROW CD | ROW EF | ROW GH |
|---|---|---|---|---|---|---|
| 1 | Rx3[2]+ | Rx3[2]- | GND | GND | GND | GND |
| 2 | Rx1[2]+ | Rx1[2]- | GND | GND | GND | GND |
| 3 | Rx3[1]+ | Rx3[1]- | GND | GND | GND | GND |
| 4 | Rx1[1]+ | Rx1[1]- | GND | GND | GND | GND |
| 5 | BI_DD1+ | BI_DD1- | GND | GND | GND | GND |
| 6 | BI_DD2+ | DI_DD2- | GND | GND | GND | GND |
| 7 | N.C. | N.C. | GND | GND | GND | GND |
| 8 | N.C. | N.C. | GND | GND | GND | GND |
| 9 | N.C. | N.C. | GND | GND | GND | GND |
| 10 | N.C. | N.C. | GND | GND | GND | GND |

# B.10 RTM Connector (J30)

| Pin | ROW A | ROW B | ROW C | ROW D | ROW E | ROW F |
|---|---|---|---|---|---|---|
| 1 | V_12V_1 | V_12V_5 | V_12V_2 | V_3V2_SUS | FPGA_IO_3 | RTM_PRSNT# |
| 2 | V_12V_3 | V_12V_6 | V_12V_4 | NC_D2 | IPMC_SCL | IPMC_SDA |
| 3 | SP_TX | SP_RX | JTAG_TD1 | JTAG_TDO | JTAG_TMS | JTAG_TCK |
| 4 | USB1_D+ | USB1_D- | INT_0 | INT_1 | RTML_TX | RTML_RX |
| 5 | SP_RTS# | SP_CTS# | MD2# | RSVD_D5 | CLK_PE+ | CLK_PE- |
| 6 | SATA_TX+ | SATA_TX- | SATA_RX+ | SATA_RX- | SFP1_SCL | SFP1_SDA |
| 7 | SAS_0_TX+ | SAS_0_TX- | SAS_0_RX+ | SAS_0_RX- | SAS_1_TX- | SAS_1_TX+ |
| 8 | GBE_TX1+ | GBE_TX1- | GBE_RX1+ | GBE_RX1- | GBE_TX2+ | GBE_TX2- |
| 9 | PE6_TX- | PE6_TX+ | PE7_RX- | PE7_RX+ | PE5_TX+ | PE5_TX- |
| 10 | PE4_TX- | PE4_TX+ | PE5_RX+ | PE5_RX- | PE7_TX+ | PE7_TX- |

| Pin | ROW G | ROW H | ROW AB | ROW CD | ROW EF | ROW GH |
|---|---|---|---|---|---|---|
| 1 | FPGA_IO_1 | RTM_EN# | GND | GND | GND | GND |
| 2 | USB0_D+ | USB0_D- | GND | GND | GND | GND |
| 3 | JTAG_TRST | FPGA_IO_2 | GND | GND | GND | GND |
| 4 | RTML_CLK | PROG | GND | GND | GND | GND |
| 5 | RSVD_G5 | JTAG_SEL | GND | GND | GND | GND |
| 6 | SFP0_SCL | SFP0_SDA | GND | GND | GND | GND |
| 7 | SAS_1_RX+ | SAS_1_RX- | GND | GND | GND | GND |
| 8 | GBE_RX2+ | GBE_RX2- | GND | GND | GND | GND |
| 9 | PE6_RX+ | PE6_RX- | GND | GND | GND | GND |
| 10 | PE4_RX- | PE4_RX+ | GND | GND | GND | GND |

# B.11 Power (P10)

| Signal | Pin | | Pin | Signal |
|---|---|---|---|---|
| N.P. | 1 | | 2 | N.P. |
| N.P. | 3 | | 4 | N.P. |
| HA0 | 5 | | 6 | HA1 |
| HA2 | 7 | | 8 | HA3 |
| HA4 | 9 | | 10 | HA5 |
| HA6 | 11 | | 12 | HA7/P |
| SCL_A | 13 | | 14 | SDA_A |
| SCL_B | 15 | | 16 | SDA_B |
| MT1_TIP(N.C.) | 17 | | 18 | MT2_TIP(N.C.) |
| RING_A(N.C.) | 19 | | 20 | RING_B(N.C.) |
| MT1_RING(N.C.) | 21 | | 22 | MT2_RING(N.C.) |
| RRTN_A(N.C.) | 23 | | 24 | RRTN_B(N.C.) |
| SHELF_GND | 25 | | 26 | LOGIC_GND |
| ENABLE_B | 27 | | 28 | VRTN_A |
| VRTN_B | 29 | | 30 | EARLY_A |
| EARLY_B | 31 | | 32 | ENABLE_A |
| -48V_A | 33 | | 34 | -48V_B |

# C. BIOS Setup Error Codes

## C.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

| Checkpoint | Description |
|---|---|
| Before D1 | Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled. |
| D1 | Perform keyboard controller BAT test. Check if waiking up from power management suspend state. Save power-on CPUID value in scratch CMOS. |
| D0 | Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum. |
| D2 | Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled. |
| D3 | If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled. |
| D4 | Test base 512KB memory. Adjust policies and cache first 8MB. Set stack. |
| D5 | Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. |
| D6 | Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information. |
| D7 | Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash. |
| D8 | The Runtime module is uncompressed into memory. CPUID information is stored in memory. |
| D9 | Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM. |
| DA | Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See POST Code Checkpoints section of document for more information. |
| E1-E8 | |
| EC-EE | OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next. Refer to memory initialization ERROR CODE D.5 |

# C.2 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

| Checkpoint | Description |
|---|---|
| 03 | Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags." |
| 04 | Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A.<br>Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system |
| 05 | Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table. |
| 06 | Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt.<br>Traps INT1Ch vector to "POSTINT1ChHandlerBlock." |
| 08 | Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5. |
| C0 | Early CPU Init Start -- Disable Cache - Init Local APIC |
| C1 | Set up boot strap processor Information |
| C2 | Set up boot strap processor for POST |
| C5 | Enumerate and set up application processors |
| C6 | Re-enable cache for boot strap processor |
| C7 | Early CPU Init Exit |
| 0A | Initializes the 8042 compatible Key Board Controller. |
| 0B | Detects the presence of PS/2 mouse. |
| 0C | Detects the presence of Keyboard in KBC port. |
| 0E | Testing and initialization of different Input Devices. Also, update the Kernel Variables.<br>Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1.<br>Uncompress all available language, BIOS logo, and Silent logo modules. |
| 13 | Early POST initialization of chipset registers. |
| 24 | Uncompress and initialize any platform specific BIOS modules. |
| 30 | Initialize System Management Interrupt. |
| 2A | Initializes different devices through DIM.<br>See DIM Code Checkpoints section of document for more information. |
| 2C | Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs. |
| 2E | Initializes all the output devices. |
| 31 | Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module. |
| 33 | Initializes the silent boot module. Set the window for displaying text information. |
| 37 | Displaying sign-on message, CPU information, setup key message, and any OEM specific information. |
| 38 | Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information. |
| 39 | Initializes DMAC-1 & DMAC-2. |

| Checkpoint | Description |
|---|---|
| 3A | Initialize RTC date/time. |
| 3B | Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system. |
| 3C | Mid POST initialization of chipset registers. |
| 40 | Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA...etc. |
| 50 | Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed. |
| 52 | Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. |
| 60 | Initializes NUM-LOCK status and programs the KBD typematic rate. |
| 75 | Initialize Int-13 and prepare for IPL detection. |
| 78 | Initializes IPL devices controlled by BIOS and option ROMs. |
| 7A | Initializes remaining option ROMs. |
| 7C | Generate and write contents of ESCD in NVRam. |
| 84 | Log errors encountered during POST. |
| 85 | Display errors to the user and gets the user response for error. |
| 87 | Execute BIOS setup if needed / requested. |
| 8C | Late POST initialization of chipset registers. |
| 8D | Build ACPI tables (if ACPI is supported) |
| 8E | Program the peripheral parameters. Enable/Disable NMI as selected |
| 90 | Late POST initialization of system management interrupt. |
| A0 | Check boot password if installed. |
| A1 | Clean-up work needed before booting to OS. |
| A2 | Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed. |
| A4 | Initialize runtime language module. |
| A7 | Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's. |
| A8 | Prepare CPU for OS boot including final MTRR values. |
| A9 | Wait for user input at config display if needed. |
| AA | Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module. |
| AB | Prepare BBS for Int 19 boot. |
| AC | End of POST initialization of chipset registers. |
| B1 | Save system context for ACPI. |
| 00 | Passes control to OS Loader (typically INT19h). |
| 61-70 | OEM POST Error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next. |
| DD-DE | OEM PCI init debug POST code during DIMM init, See DIM Code Checkpoints section of document for more information. |

# C.3 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system busses. The following table describes the main checkpoints where the DIM module is accessed:

| Checkpoint | Description |
|---|---|
| 2A | Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices. |
| 38 | Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 CONFIGURES all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices. |
| DD-DE | OEM PCI init debug POST code during DIMM init. DEh during BUS number assignment and DDh during ressource allocation, Hight byte is the BUS number. |

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.

1 = func#1, static devices initialization on the BUS concerned.

2 = func#2, output device initialization on the BUS concerned.

3 = func#3, input device initialization on the BUS concerned.

4 = func#4, IPL device initialization on the BUS concerned.

5 = func#5, general device initialization on the BUS concerned.

6 = func#6, error reporting for the BUS concerned.

7 = func#7, add-on ROM initialization for all BUSes.

8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).

1 = On-board System devices.

2 = ISA devices.

3 = EISA devices.

4 = ISA PnP devices.

5 = PCI devices.

# C.4 Memory Initialization ERROR Code

| Checkpoint | Description |
|---|---|
| E8 | Memory Error - No memory installed. |
| EA | Memory Error - DDR3 Initialisation |
| EB | Memory Error - Memory test |
| ED | Memory Error - RDIMMs and UDIMMs are mixed |
| EE | Memory Error - Invalid Memory Population |
| EF | Memory Error - Memory structure problem |

# D. Software Update

To update the board software, it is recommended to use the Kontron update CD. A version of this CD can be found on the CD/DVD provided with your board or on the Kontron's FTP site. Updating your board with this Update CD will have a payload impact on your board. To update your board from the update CD, boot from the CD and follow the instructions provided in the AT8050 - Update CD User guide provided with the CD image file.

A remote update procedure is also available using the HPM files. This procedure has no payload impact. The instructions on how to use it are provided with the HPM package.

The latest versions of the Update CD and HPM files are available from the Kontron's FTP site(cbu.kontron.ca).

# E. Getting Help

If, at any time, you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

| North America | EMEA |
|---|---|
| Tel.: +1 888 294 4558 | Tel.: +800-KONTRONAG |
| Fax: +1 858 677 0898 | Fax: +49 821 4086 888 |

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at:

North America: support@us.kontron.com

EMEA: support@kontron.com

Or at the following address:

| North America | EMEA |
|---|---|
| Kontron America, Inc. | Kontron Europe GmbH |
| 14118 Stowe Drive | Lise-Meitner-Str. 3-5 |
| Poway, CA 92064-7147 | 86156 Augsburg |
| USA | Germany |

## E.1 Returning Defective Merchandise

Before returning any merchandise please do one of the following:

- Call

  1 Call our Technical Support department in North America at +1 888 294 4558 and in EMEA at +800-KONTRONAG. Make sure you have the following on hand: our Invoice #, your Purchase Order #, and the Serial Number of the defective unit.

  2 Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.

3 The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.

4 Make sure you receive an RMA # from our Technical Support before returning any merchandise.

- E-mail

1 Send us an e-mail at: support@us.kontron.com in North America and at: support@kontron.com in EMEA. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the serial number of the defective product and a description of the problem.

## E.2 When Returning a Unit

- In the box, you must include the name and telephone number of a contact person, in case further explanations are required. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.
- Ensure that the unit is properly packed. Pack it in a rigid cardboard box.
- Clearly write or mark the RMA number on the outside of the package you are returning.
- Ship prepaid. We take care of insuring incoming units.

| North America | EMEA |
|---|---|
| Kontron America, Inc. | Kontron Europe GmbH |
| 14118 Stowe Drive | Lise-Meitner-Str. 3-5 |
| Poway, CA 92064-7147 | 86156 Augsburg |
| USA | Germany |

# F. Glossary

| Acronyms | Descriptions |
|---|---|
| ACPI | Advanced Configuration & Power Interface |
| AdvancedMC | (Same as AMC). Advanced Mezzanine Card. |
| AMC | (Same as AdvancedMC). Advanced Mezzanine Card. |
| AMC.0 | Advanced Mezzanine Card Base Specification. |
| AMC.1 | PCI Express and Advanced Switching on AdvancedMC. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0). |
| AMC.2 | Ethernet Advanced Mezzanine Card Specification. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0). |
| AMC.3 | Advanced Mezzanine Card Specification for Storage. A subsidiary specification to the Advanced Mezzanine Card Base Specification (AMC.0). |
| ANSI | American National Standards Institute |
| API | Application Programming Interface |
| APIC | Advanced Programmable Interrupt Controller |
| ASCII | American Standard Code for Information Interchange. ASCII codes represent text in computers, communications equipment, and other devices that work with text. |
| ATA | Advanced Technology Attachment |
| ATAPI | Advanced Technology Attachment Packet Interface |
| ATCA | Advanced Telecommunications Computing Architecture |
| BBS | BIOS Boot Specification |
| BI | Base Interface. Backplane connectivity defined by the ATCA. |
| BIOS | Basic Input/Output System |
| BMC | Base Management Controller |
| CD | Compact Disk |
| CDROM | (Same as CD-ROM). Compact Disk Read-Only Memory. |
| CD-ROM | (Same as CDROM). Compact Disk Read-Only Memory. |
| CFM | Cubic Foot per Minute |
| CLI | Command-Line Interface |
| CLK1 | AdvancedTCA bused resource Synch clock group 1 |
| CLK1A | AdvancedTCA bused resource Synch clock group 1, bus A |
| CLK1B | AdvancedTCA bused resource Synch clock group 1, bus A |
| CLK2 | AdvancedTCA bused resource Synch clock group 2 |
| CLK2A | AdvancedTCA bused resource Synch clock group 2, bus A |
| CLK2B | AdvancedTCA bused resource Synch clock group 2, bus B |
| CLK3 | AdvancedTCA bused resource Synch clock group 3 |
| CLK3A | AdvancedTCA bused resource Synch clock group 3 , bus A |
| CLK3B | AdvancedTCA bused resource Synch clock group 3 , bus B |
| CMOS | Complementary Metal Oxide Semiconductor. Also refers to the small amount of battery (or capacitor) powered CMOS memory to hold the date, time, and system setup parameters. |
| CPLD | Complex Programmable Logic Device |
| CP-TA | Communications Platforms Trade Association |
| CPU | Central Processing Unit. This sometimes refers to a whole blade, not just a processor component. |

| Acronyms | Descriptions |
|---|---|
| CTS | Clear To Send |
| DDR3 | DDR3 SDRAM or Double-Data-Rate three (3) Synchronous Dynamic Random Access Memory. |
| DHCP | Dynamic Host Configuration Protocol |
| DIMM | Dual In-line Memory Module |
| DMA | Direct Memory Access |
| DMI | Desktop Management Interface |
| DTC | Data Transfer Controller |
| DTR | Data Terminal Ready |
| DTS | Digital Thermal Sensor in IA32 processors. |
| DVD | Digital Video Disk |
| ECC | Error Checking and Correction |
| EMI | ElectroMagnetic Interference |
| ETH | Same as Ethernet. |
| FC | Fibre Channel |
| FCC | Federal Communications Commission |
| FI | Fabric Interface. Backplane connectivity defined by the ATCA. |
| FIFO | First In First Out |
| FPGA | Field-Programmable Gate Array |
| FRU | Field Replaceable Unit. Any entity that can be replaced by a user in the field. Not all FRUs are hot swappable. |
| FWH | FirmWare Hub. Boot flash connected to the LPC bus containing BIOS FW. |
| Gb | Gigabit |
| GB | (Same as GByte) GigaByte. |
| GByte | (Same as GB) GigaByte. |
| GbE | Gigabit Ethernet |
| GHz | GigaHertz |
| GND | GrouND |
| HDD | Hard Disc Drive |
| HPM | PICMG Hardware Platform Management specification family |
| HPM.1 | Hardware Platform Management IPM Controller Firmware Upgrade Specification |
| HW | HardWare |
| I2C | Inter Integrated Circuit bus |
| ICH | I/O Controller Hub |
| ICT | In-Circuit Test |
| ID | IDentification |
| IEEE | Institute of Electrical and Electronics Engineers |
| IMVP-6 | Intel Mobile Voltage Positioning. The Intel Mobile Voltage Positioning specification for the Intel® Core™ Duo Processor. It is a DC-DC converter module that supplies the required voltage and current to a single processor. |
| IO | (Same as I/O). Input Output |
| IOH | I/O Hub |
| IOL | IPMI-Over-LAN |
| IP | Internet Protocol |

| Acronyms | Descriptions |
|---|---|
| IPM | Intelligent Platform Management |
| IPMB | Intelligent Platform Management Bus |
| IPMB-0 | Intelligent Platform Management Bus Channel 0, the logical aggregation of IPMB-A and IPMB-B. |
| IPMB-A | Intelligent Platform Management Bus A |
| IPMB-B | Intelligent Platform Management Bus B |
| IPMB-L | Intelligent Platform Management Bus Local |
| IPMC | Intelligent Platform Management Controller |
| IPMI | Intelligent Platform Management Interface |
| IPMIFWU | Intelligent Platform Management Interface FirmWare Update |
| IPv6 | Internet Protocol version 6 |
| IRQ | Interrupt ReQuest |
| JTAG | Joint Test Action Group |
| KHz | KiloHertz |
| LAN | Local Area Network |
| LED | Light-Emitting Diode |
| LFM | Low Frequency Mode. The lowest operating speed for the processor. |
| LPC | Low Pin Count port |
| MAC | Media Access Controller address of a computer networking device. |
| MB | MegaByte |
| MCH | Memory Controller Hub |
| MHz | MegaHertz |
| MMC | Module Management Controller. MMCs are linked to the IPMC. |
| NC | Not Connected |
| OOS | Out Of Service |
| OS | Operating System |
| PHY | PHYsical layer. Generic electronics term referring to a special electronic integrated circuit or functional block of a circuit that takes care of encoding and decoding between a pure digital domain (on-off) and a modulation in the analog domain. |
| PICMG | PCI Industrial Computer Manufacturers Group |
| PICMG® | PCI Industrial Computer Manufacturers Group |
| POST | Power-On Self-Test |
| prAMC | Processor AMC |
| RAID | Redundant Array of Independent Disks / Redundant Array of Inexpensive Disks. |
| RAM | Random Access Memory |
| RHEL | Red Hat Enterprise Linux |
| RoHS | Restriction of the Use of Certain Hazardous Substances |
| RS-232 | (Same as RS232). Recommended Standard 232. |
| RS232 | (Same as RS-232). Recommended Standard 232. |
| RTC | Real Time Clock |
| RTM | Rear Transition Module |
| RTM-Link | Rear Transition Module Link. Kontron 3-wire protocol. |
| RTS | Request To Send |

| Acronyms | Descriptions |
|---|---|
| SAS | Serial Attached SCSI |
| SATA | Serial ATA |
| SEL | System Event Log |
| SFP | Small Form-factor Pluggable |
| ShMC | Shelf Management Controller |
| SMB | (Same as SMBus/SMBUS). System Management Bus. |
| SMBIOS | System Management BIOS |
| SMBUS | (Same as SMB/SMBus). System Management Bus. |
| SMBus | (Same as SMB/SMBUS). System Management Bus. |
| SOL | Serial Over LAN |
| SPI | Serial Peripheral Interface |
| SpeedStep | (Same as EIST). Enhanced Intel SpeedStep Technology. |
| SSE2 | Streaming SIMD Extension 2. SIMD is "Single Instruction, Multiple Data". |
| SSE3 | Streaming SIMD Extension 3. SIMD is "Single Instruction, Multiple Data". |
| SSH | Secure SHell. A network protocol that allows data to be exchanged over a secure channel between two computers. |
| TCLKA | Telecom CLocK A. AMC Clock Interface. |
| TCLKB | Telecom CLocK B. AMC Clock Interface. |
| TCLKC | Telecom CLocK C. AMC Clock Interface. |
| TCLKD | Telecom CLocK D. AMC Clock Interface. |
| TX | Transmit |
| TXD | Transmit |
| UART | Universal Asynchronous Receiver Transmitter |
| USB | Universal Serial Bus |
| VCC | Power supply |
| VLAN | Virtual Local Area Network |
| XAUI | X (meaning ten) Attachement Unit Interface. A standard for connecting 10 Gigabit Ethernet (10GbE) ports. |