» Kontron User's Guide «

Kontron microETXexpress®-PV

microETXexpress®-PV Computer-on-Module (COM)

Version 1.4

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1 User Information

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Please consult our website at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section for the latest BIOS downloads, Product Change Notifications and additional tools and software. You can also always contact your board supplier for technical support.

2 Introduction

2.1 The microETXexpress®-PV COM

The Kontron microETXexpress®-PV Computer-on-Module (COM) extends the COM Express® specification to include a small module form factor (95 x 95 mm) with the commonly used COM Express® Type 2 connector for use on ultra-low power embedded devices. The microETXexpress®-PV COM design enables the development of energy-saving devices based on the second generation 1.66 GHz Intel® Atom™ processor D510, D410, and N450 technology and the Intel® I/O Controller Hub 82801HBM (ICH8M) with the secure development path of an established, future-proof industry standard, the COM Express® Type 2 form factor.

The Kontron microETXexpress®-PV module processor has an integrated memory controller for up to 2 GB DDR2 RAM (2x 1GB configuration). The graphics core has a maximum resolution of 1400x1050 VGA and 18-bit single channel LVDS for WXGA (1366x768). With five PCI Express lanes for flexible configurations as well as PCI, I^2C, SPI, and LPC bus, the microETXexpress®-PV COM is ideal for multi-interface, ultra-low power carrier board designs. These special features make this 95 x 95 mm Computer-on-Module a key solution for applications like infotainment, digital signage, POS/POI, medical technology, and automation that require both mobile and compact stationary low power devices.

All modules in the Kontron microETXexpress® family are compatible with the COM Express® standard (Pin-out Type 2) and thus ensure easy interchangeability as well as design scalability and future migration paths. The microETXexpress®-PV COM is a complete PC with standard interfaces such as USB, Gigabit Ethernet, SATA II, and PATA as well as additional options like high-definition audio (HDA) and an LVDS flat panel interface.

2.2 Naming Clarifications

The COM Express® standard defines a Computer-On-Module, or COM, with all the components necessary for a bootable host computer, packaged as a super-component. The interfaces provide a smooth transition path from legacy parallel interfaces such as IDE or parallel ATA (PATA) to Low Voltage Differential Signaling (LVDS) interfaces including the PCI bus, PCI Express*, and Serial ATA (SATA).

» ETXexpress® modules are Kontron COM Express® modules in the basic form factor (125mm x 95mm)

» microETXexpress® modules are Kontron COM Express® modules in the compact form factor (95mm x 95mm)

» nanoETXexpress® modules are Kontron COM Express® compatible modules in an ultra-small form factor that follow pin-out type 1(55mm x 84mm)

NOTE: The Kontron microETXexpress®-PV module takes advantage of new features introduced in the PICMG COM COM.0R2.0 COM Express® Specification.

2.3 Understanding the COM Functionality

All Kontron microETXexpress® and ETXexpress® modules contain two connectors (X1A and X1B), each with two rows. The primary connector rows are Row A and Row B. The secondary connector rows are Row C and Row D. The primary connector (Row A and Row B) features the following legacy-free functionality:

» Analog VGA graphics

» Gigabit Ethernet LAN

» Serial ATA (SATA)

» Intel® High Definition Audio (HDA)

» 8xUSB 2.0

» 4.75V to 18.0V VCC

» LPC (Low Pin Count) Bus

» Five x1 PCI Express lanes

» GPIO

» LVDS 18-bit, single channel

» SMBus

» Watchdog timer (WDT)

» I^2C

» SPI Bus

The secondary connector (Row C and Row D) supports the following buses and I/O:

» IDE and parallel ATA (PATA)

» PCI

NOTE: For a full description of the COM Express Type 2 pin-out, refer to the PICMG website or PICMG documentation.

2.4 COM Express® Documentation

This product manual serves as one of three principal references for this COM Express® module design. It documents the specifications and features of the microETXexpress®-PV COM. The other two references, which are available from your Kontron support representative or from PICMG, include:

» The COM Express® Specification, R2.0, which defines the COM Express® module form factor, pin-out, and signals. This document can be obtained by filling out the order form on the PIGMG website at http://www.picmg.com .

» The PICMG COM Express® Design Guide, which serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COM Express® modules. This guide is on the PICMG website at http://www.picmg.com .

2.5 COM Express® COM Benefits

Compact form factor (95 x 95 mm) Computer-on-Module Express (COM Express) modules are very compact, highly integrated computers that use the Type 2 COM Express® connector pin-out. All microETXexpress® modules feature a standardized form factor and a standardized connector layout for a specified set of signals, as defined in the PICMG COM Express® specification. This standardization lets designers create a single-system baseboard that can accept present and future microETXexpress® modules.

Kontron microETXexpress® modules include common personal computer (PC) peripheral functions such as:

» Graphics

» USB ports

» Ethernet

» Audio

» IDE, PATA, and SATA hard disk drive formats

Baseboard designers can optimize exactly how each of these functions is implemented physically for the intended application by placing connectors precisely where they are needed on a baseboard that is designed for an optimal fit in the system packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in super-component simplifies packaging, eliminates cabling, and significantly reduces system-level total cost of ownership.

A single baseboard design can use a range of COM Express modules. This flexibility enables product differentiation at various price/performance

points, and the design of future-proof systems with a built-in upgrade path. The modularity of a COM Express solution also ensures against obsolescence as computer technology evolves. A properly designed COM Express baseboard can work with several successive generations of COM Express modules.

A COM Express baseboard design has many of the advantages of a custom, computer-board design, but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specifications

3.1 Functional Specification

Processor: Intel® Atom™ Technology

» CPU: Intel® Atom™ N450 single core, 5.5W TDP
Intel® Atom™ D410 single core, 10.5W TDP
Intel® Atom™ D510 dual core, 15W TDP
All with integrated DRAM and graphics

» Cores: Up to 2 cores

» Bus Speed: Up to 2 x 1.66 GHz

» Cache: L1 cache 24KB write-back data/32KB instruction
L2 cache up to 2x512 KB, 8-way

» Memory: Up to 2GB (single channel) DDR2 S0DIMM (667 MHz only)

2x 1GB configuration only

» Video Controller: Integrated, Intel® GMA 3150 (200 MHz for N450 or 400 MHz for D410/D510) with DirectX*9-compliant Pixel Shader 2.0
Intel® Clear Video Technology:
MPEG2 Hardware Acceleration
ProcAmp
Intel® Dynamic Video Memory Technology 4.0

» Graphics: Analog VGA, with max resolution 1400x1050 at 60 Hz for the N450 or 2048x1536 at 60 Hz for the D410/D510.
18-bit single channel LVDS with resolution 1366x768

» Features: Hyper-Threading Technology (HTT)
Execute Disable Bit
BIOS-enabled enhanced Intel® SpeedStep Technology (modules with the N450 CPU only)
CPU Sleep States:
D510/D410: C0/C1
N450: C0/C1(E)/C2(E)/C4(E)

» Instruction Set: IA 32-bit and Intel® 64 architecture

» Package: 22mm x 22mm

» Thermal Spec: Operation: 0° to 70°C
Storage: -10° to 85°

Chipset: Intel® I/O Controller Hub 82801HBM (ICH8M)

» USB: 8xUSB 2.0

» Audio: Intel® High Definition Audio (24 bit / 96 kHz) controller

» PCI Express: Five PCIe x1 lanes or configurable (via BIOS modification) to an x4 , x2 or x1 interface

» TDP: 2.3W
Package: 31mmx31mm

Integrated Graphics: Intel® Graphics Media Accelerator 3150 (Intel® GMA 3150)

» Features: Intel® Dynamic Video Memory Technology 4.0
DirectX* 9 compliant Pixel Shader 2.0
Integrated single LVDS channel resolution up to 1280x800 or 1366x768 (for flat panels)
Analog RGB display output resolution up to 1400x1050 @ 60Hz for the Intel® Atom™
N450 or D410 processors and 2048 x 1536@ 60 Hz for the Intel® Atom™ D510 processor
Intel® Clear Video Technology
-- MPEG2 Hardware Acceleration
-- ProcAmp

Display Interfaces

» VGA: The maximum resolution supported is 2048 x 1536 @ 60Hz (Intel® Atom™ D510 processor)

» Flat Panel: Single Channel LVDS 18bit
resolution up to 1366 x 768 (WXGA)

Storage

» SATA: 3xSATA ports supporting up to 1.5 Gbps (SATA150) and 3.0 Gbps (SATA300) transfer rate

» PATA (IDE): 1x Parallel ATA (PATA) supports ATA transfer mode up to Ultra DMA 5 at 100MB/s.

Onboard Devices:

» Ethernet: Intel® 82567LM 10/100/1000 Mbit Gigabit Ethernet Controller
The 82567LM is only a PHY; the MAC is in the ICH. It is connected to the GLCI and LCI interfaces of the ICH8M.

» Ethernet Features: WakeOnLAN, PXE Lanboot,

» TPM: AT97SC3204 TPM from Atmel

» Watchdog Timer: BIOS enables and configures watchdog in the CPLD.
Watchdog has the option to generate NMI after the delay has expired.

» PCI: The PCI 32-bit 33 MHz interface from the ICH (rev. 2.3 compliant) is connected to the COM Express connector.

» Power Management: BIOS enables ACPI power management revision 3.0 for supported OS.
BIOS enables SpeedStep Technology for the Atom N450 processor.
The Atom D510 and D410 processors do not support SpeedStep technology.

Additional Interfaces:

» LPC bus: Yes, to COM Express A-B connector

» SMBus: Yes, to COM Express A-B connector

» I^2C: Yes, fast I^2C (from Intel® ICH8M)

» GPIO: 4x GPI and 4x GPO

» SPI Yes, to COM Express A-B connector

» JIDA: Yes, JIDA EEPROM
JIDA BIOS support
JILI BIOS support
AMI AMIBIOS8 Core BIOS

» K-Station: Yes

» Bootlogo: Yes

» MARS: Supported for smart battery management

» HWM: Temperature monitoring for CPU and board temperature (external ON Semiconductor ADT7476 hardware monitor)

» Passive Cooling: Passive and Critical Trip Point

» ACPI: ACPI 3.0

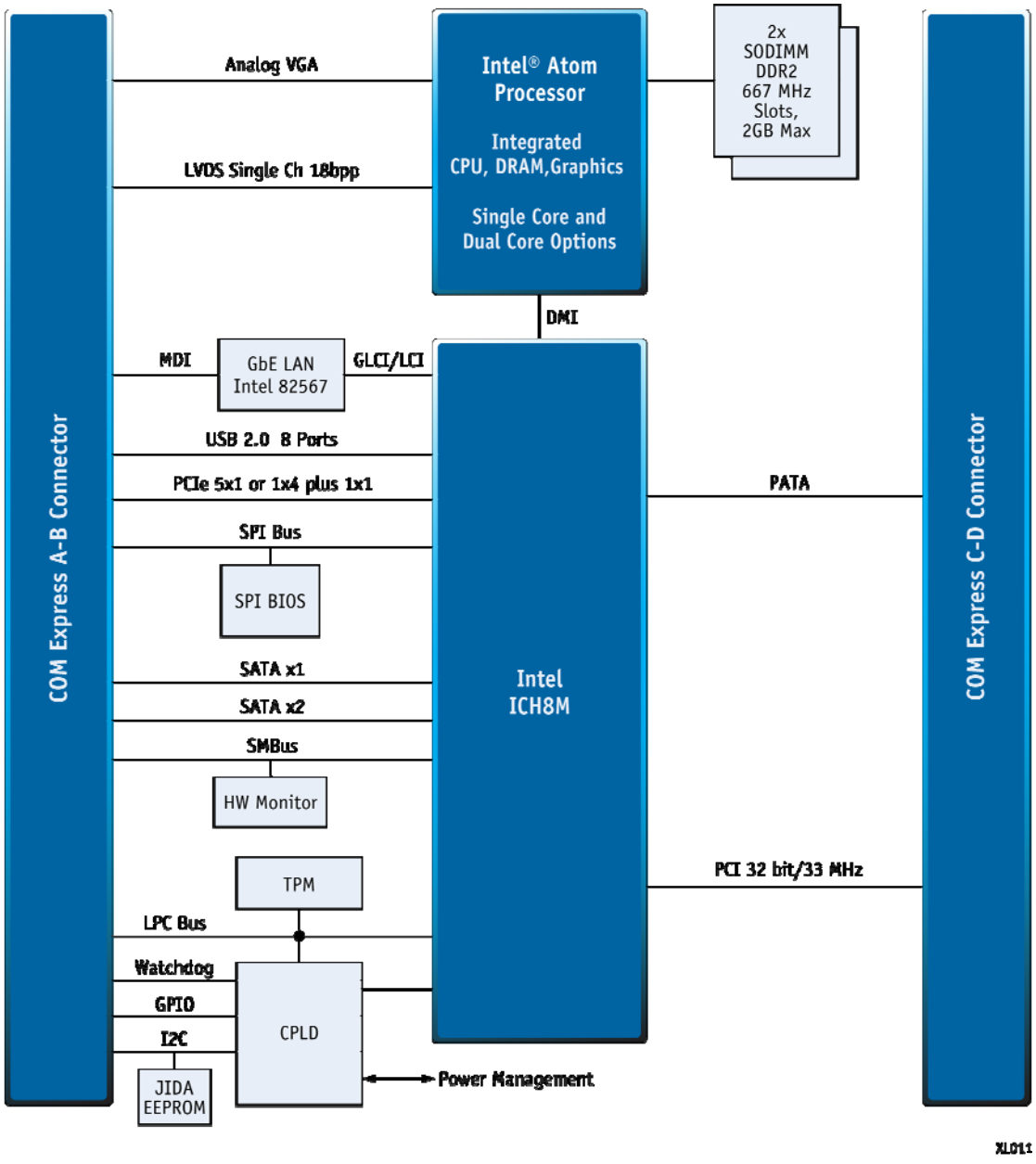
» S-States: S0, S3, S4, S5

» Input Voltage: Single supply support with wide range power supply input, 4.75V – 18V
The 5.0V supply is the standby power rail.

3.2 Functional Block Diagram

Figure 1 is t he microETXexpress®-PV COM block diagram

Figure 1: microETXexpress®-PV COM Block Diagram



3.3 Mechanical Specifications

Module Dimensions

» 95 mm x 95 mm ±0.2 mm (3.47 in. x 3.47 in)

Height on Top

» Approximately 9.20 mm maximum (without the PCB)

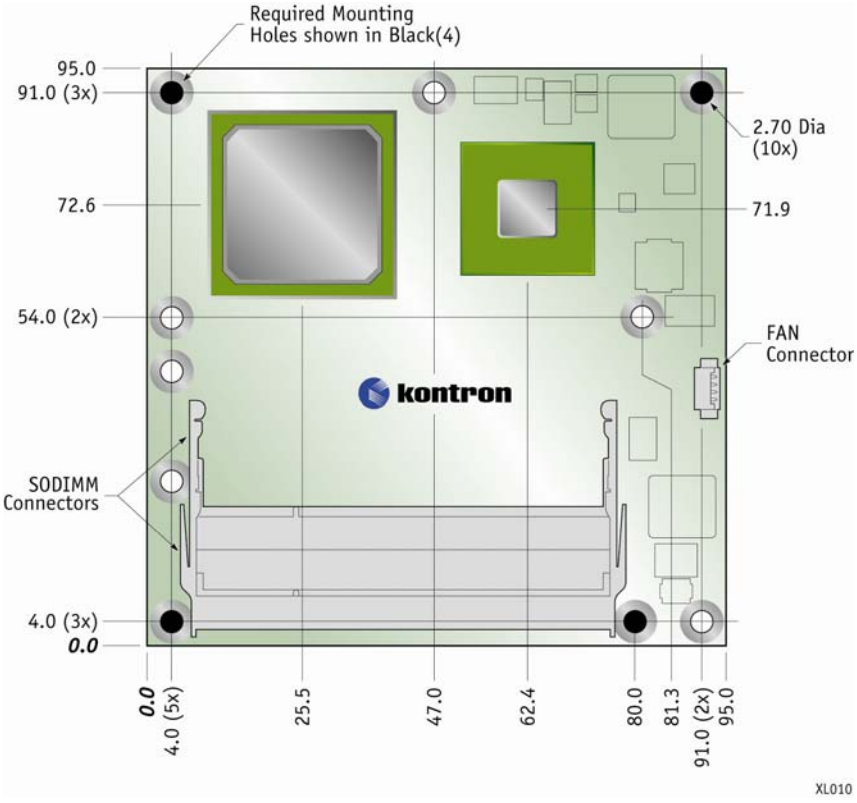
» Height varies depending on whether the optional cooling solution (either a passive heat sink or a heat spreader plate) is installed

Height on Bottom

» Approximately 3.5 mm maximum (without the PCB)

Figure 2 is the microETXexpress®-PV COM mechanical drawing

Figure 2: microETXexpress®-PV COM Mechanical Drawing



All dimensions are shown in millimeters. The COM Express® specification says that these holes should be ± 0.25mm [±0.010"], unless otherwise noted. The tolerances for placement of the COM Express connector with respect to the peg holes (dimensions [16.50, 6.00]) should be ± 0.10mm [±0.004"]. The 2x 220-pin connectors are mounted on the back of the PCB and not viewable in Figure 2. The mounting holes shown in the drawing use 6mm diameter pads and 2.7mm plated holes for use with 2.5mm hardware. The pads are tied to the PCB ground plane. Gray circles represent the mechanical mounting holes. Black circles represent the mounting holes required by the PICMG COM Express® standard.

3.4 Electrical Specifications

3.4.1Supply Voltage

» 4.75V to +18V on the VCC_12V pins and 4.75V to 5.25V on the VCC_5V_SBY.

Power Supply Rise time specifications

» The input voltages shall raise from ≤10% of nominal to within the regulation ranges within 0.1ms to 20ms.

» There shall be a smooth and continuous ramp with each DC input voltage from 10% to 90% of its final set-point, as required in the ATX specification.

» The maximum ramp up rate shall be 1V/ms maximum in order to prevent any excessive inrush current that could damage the module.

3.4.2Power consumption Current (Windows XP SP3)

The testing performed to capture the supply current data used tested modules mounted on a Kontron evaluation board with a mouse and keyboard connected. The power consumption tests were executed in Windows XP (with SP3) using a tool to stress the CPU and memory at 100 % load. The power measurement values were captured after 15 minutes of full load. All boards were equipped with a two (2) 1024-MB DDR2 SDRAM. The modules were tested using the maximum CPU frequency. For more detailed information, refer to the "Power Consumption" diagrams on the EMD Customer section of the Kontron website.

Table 1: Atom D510 - 36007-0000-16-2

	Power Consumption in [W]
Windows Desktop (idle)	10.8
Maximum power configuration	21.16
S3 with Wake-on-LAN disabled	0.440
S5 with Wake-on-LAN disabled	0.255

Table 2: Atom D410 - 36007-0000-1

	Power Consumption in [W]
Windows Desktop (idle)	9.7
Maximum power configuration	16.56
S3 with Wake-on-LAN disabled	0.440
S5 with Wake-on-LAN disabled	0.255

Table 3: Atom N450 - 36007-0000-16-0

	Power Consumption in

	[W]
Windows Desktop (idle)	7.5
Maximum power configuration	15.20
S3 with Wake-on-LAN disabled	0.440
S5 with Wake-on-LAN disabled	0.255

NOTE: It is difficult to test for all possible applications on the market. There may be an application that draws more power from the CPU than the values measured in the table above. Take this into consideration if you are at the limit of the thermal specification, in which case you should consider improving your thermal solution.

3.5 Environmental Specifications

3.5.1Temperature

Operating: (with Kontron heat spreader plate assembly):

- Ambient temperature: 0 to 70°C
- Maximum heat spreader-plate temperature: 0 to 70°C*
- Non-operating: -10°C to +85°C

NOTES: *1) The maximum operating temperature with the heat spreader plate installed is the maximum measurable temperature on any spot on the heat spreader surface. You must maintain the temperature according to the specification above.
2) All parts used have industrial operating temperature (-40°C to 85°C).

Operating (without Kontron heat spreader plate assembly):

- Maximum operating temperature: 0-60°C
- Non operating: -10°C to +85°C

NOTE: **The maximum operating temperature is the maximum measurable temperature on any spot on the module surface. You must maintain the temperature according to the specification above.

Humidity

- Operating: 5% to 95% (non-condensing)at 40°C
- Non operating: 5% to 95% (non-condensing) at 40°C

3.6 MTBF

218,015 hours

4 COM Connectors

The pin-outs for microETXexpress® interface connectors X1A (primary connector, rows A and B) and X1B (secondary connector, rows C and D) are documented for convenient reference. See the PICMG COM Express® Specification on the PICMG website and COM Express® Design Guide on the Kontron website for detailed, design-level information.

Figure 3: COM Interface Connector Locations

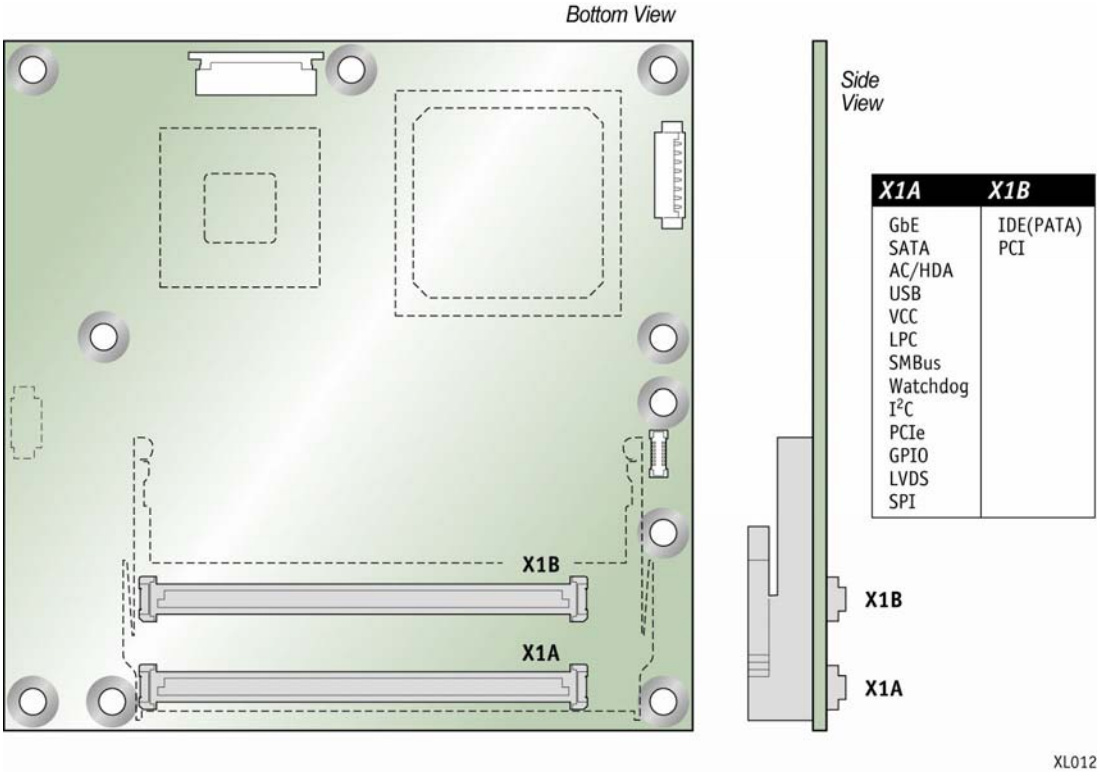


Table 4: General Signal Description

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1,8V Output
O-3,3	3,3V Output
O-5	5V Output

Type	Description
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection
nc	Not connected, Signal not available

NOTE: To protect external power lines of peripheral devices, make sure that the wires have the right diameter to withstand the maximum available current and the enclosure of the peripheral device fulfils the fire-protection requirements in IEC/EN60950

4.1 Pin-Outs

4.1.1Connectors X1A and X1B: microETXexpress® Interface

Table 5: Connector X1A - Row A

Pin	Signal	Description	Type	Termination	Comment
A1	GND(Fixed)	Power Ground	PWR	-	-
A2	GBE0_MDI3-	Ethernet I/O Data-	DP-I/O	-	-
A3	GBE0_MDI3+	Ethernet I/O Data+		-	-
A4	GBE0_LINK100#	Ethernet Speed LED 100Mbps	OD-3.3/3.3 SUS	-	On at 100 Mbps
A5	GBE0_LINK1000#	Ethernet Speed LED 1000Mbps	OD-3.3/3.3 SUS	-	On at 1000 Mbps
A6	GBE0_MDI2-	Ethernet I/O Data-	DP-I/O	-	-
A7	GBE0_MDI2+	Ethernet I/O Data-		-	-
A8	GBE0_LINK#	LAN Link LED	OD – 3.3/3.3 SUS	-	-
A9	GBE0_MDI1-	Ethernet I/O Data-	DP-I/O	-	-
A10	GBE0_MDI1+	Ethernet I/O Data-		-	-
A11	GND (Fixed)	Power Ground	PWR	-	-
A12	GBE0_MDI0-	Ethernet I/O Data-	DP-I/O	-	-
A13	GBE0_MDI0+	Ethernet I/O Data-		-	-
A14	GBE0_CTREF	LAN Reference Voltage	O-1.9/1.9 SUS	-	-

Pin	Signal	Description	Type	Termination	Comment
A15	SUS_S3#	Indicates Suspend to RAM state	O-3.3 SUS	-	-
A16	SATA0_TX+	SATA 0 Transmit Data+	DP-O	-	-
A17	SATA0_TX-	SATA 0 Transmit Data-		-	-
A18	SUS_S4#	Indicates Suspend to Disk state	O-3.3 SUS	-	-
A19	SATA0_RX+	SATA 0 Receive Data+	DP-I	-	-
A20	SATA0_RX-	SATA 0 Receive Data-			-
A21	GND (Fixed)	Power Ground	PWR		-
A22	SATA2_TX+	SATA 2 Transmit Data+	DP-O	-	-
A23	SATA2_TX-	SATA 2 Transmit Data-		-	-
A24	SUS_S5#	Indicates Soft Off state	O-3.3 SUS	-	-
A25	SATA2_RX+	SATA 2 Receive Data+	DP-I	-	-
A26	SATA2_RX-	SATA 2 Receive Data-		-	-
A27	BATLOW#	Indicates low external battery	I-3.3/3.3 SUS	PU 3.3V SUS in CPLD (5K to 25K ohms	-
A28	(S)ATA_ACT#	SATA Activity Indicator	O-3.3	-	-
A29	AC/HDA_SYNC	HD Audio Sync	O-3.3	-	-
A30	AC/HDA_RST#	HD Audio Reset	O-3.3	-	-
A31	GND(Fixed)	Power Ground	PWR	-	-
A32	AC/HDA_BITCLK	HD Audio Clock	O-3.3	-	-
A33	AC/HDA_SDOUT	HD Audio Data	O-3.3	-	-
A34	BIOS_DIS0#	Disable Module BIOS. Enables boot from a BIOS on Baseboard	I-3.3/3.3 SUS	PU 3.3V SUS of 51.1K ohms	-
A35	THRMTRIP#	CPU thermal shutdown indicator	O-3.3	-	Pin state is not valid in Suspend Power
A36	USB6-	USB Data- Port #6	DP-I/O	-	Connected to USB port #8 on the ICH8M.
A37	USB6+	USB Data+ Port #6		-	
A38	USB_6_7_OC#	USB Over current Pair 6/7	I-3.3/ 3.3 SUS	PU 3.3V SUS of 10K ohms	Connected to over current pin 8/9 of ICH8M.

Pin	Signal	Description	Type	Termination	Comment
A39	USB4-	USB Data- Port #4	DP-I/O	-	Connected to USB port #6 on the ICH8M.
A40	USB4+	USB Data+ Port #4		-	
A41	GND (Fixed)	Power Ground	PWR	-	-
A42	USB2-	USB Data- Port #2-	DP-I/O	-	Connected to USB port #2 on the ICH8M.
A43	USB2+	USB Data+ Port #2+		-	
A44	USB_2_3_OC#	USB Overcurrent Pair 2/3	I-3.3/ 3.3 SUS	PU 3.3 SUS of 10K ohms	Connected to over current pin 2/3 of ICH8M.
A45	USB0-	USB Data- Port #0-	DP-I/O	-	Connected to USB port #6 on the ICH8M.
A46	USB0+	USB Data+ Port #0+		-	
A47	VCC_RTC	RTC Power Supply +3V	PWR	-	-
A48	EXCD0_PERST#	PCIe Express Card 0 Reset	O-3.3	-	Connected to GPIO1 on the ICH8M.
A49	EXCD0_CPPE#	PCIe Express Card 0 Request	I-3.3	PU 3.3 of 10K ohms	Connected to GPIO8 on the ICH8M.
A50	LPC_SERIRQ	LPC Serial Interrupt Request	IO-3.3	PU 3.3 of 8.2K ohms	-
A51	GND (Fixed)	Power Ground	PWR	-	-
A52	PCIE_TX5+	PCIe 5 Transmit Data+	Not connected	nc	nc
A53	PCIE_TX5-	PCIe 5 Transmit Data-	Not connected	nc	nc
A54	GPI0	General Purpose Input0	I-3.3	PU 3.3 of 10K ohms	Connected to CPLD
A55	PCIE_TX4+	PCIe 4 Transmit Data+	DP-O	-	-
A56	PCIE_TX4-	PCIe 4 Transmit Data-		-	-
A57	GND(Fixed)	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCIe 3 Transmit Data+	DP-O	-	-
A59	PCIE_TX3-	PCIe 3 Transmit Data-		-	-
A60	GND (Fixed)	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCIe 2 Transmit Data+	DP-O	-	-
A62	PCIE_TX2-	PCIe 2 Transmit		-	-

Pin	Signal	Description	Type	Termination	Comment
		Data-			
A63	GPI1	General Purpose Input 1	I-3.3	PU 3.3 of 10K ohms	Connected to CPLD
A64	PCIE_TX1+	PCIe 1 Transmit Data+	DP-O	-	-
A65	PCIE_TX1-	PCIe 1 Transmit Data-		-	-
A66	GND (Fixed)	Power Ground	PWR	-	-
A67	GPI2	General Purpose Input 2	I-3.3	PU 3.3 of 10K ohms	Connected to CPLD
A68	PCIE_TX0+	PCIe 0 Transmit Data+	DP-O	-	-
A69	PCIE_TX0-	PCIe 0 Transmit Data-		-	-
A70	GND (Fixed)	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS Display Channel A (positive)	DP-O	-	-
A72	LVDS_A0-	LVDS Display Channel A (negative)		-	-
A73	LVDS_A1+	LVDS Display Channel A (positive)	DP-O	-	-
A74	LVDS_A1-	LVDS Display Channel A (negative)		-	-
A75	LVDS_A2+	LVDS Display Channel A (positive)	DP-O	-	-
A76	LVDS_A2-	LVDS Display Channel A (negative)		-	-
A77	LVDS_VDD_EN	LVDS Display Panel Power Control	O-3.3	PD 4.75K	-
A78	LVDS_A3+	LVDS Display Channel A (positive)	Not connected	nc	nc
A79	LVDS_A3-	LVDS Display Channel A (negative)	Not connected	nc	nc
A80	GND (Fixed)	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS Display Channel A Clock+	DP-O	-	-
A82	LVDS_A_CK-	LVDS Display Channel A Clock-		-	-
A83	LVDS_I2C_CK	LVDS Display I^2C	I/OD-3.3	PU 3.3 of	

Pin	Signal	Description	Type	Termination	Comment
		Clock		10K ohms	
A84	LVDS_I2C_DAT	LVDS Display I^2C Data	I/OD-3.3	PU 3.3 of 10K ohms	
A85	GPI3	General Purpose Input 3	I-3.3	PU 3.3 of 10K ohms	Connected to CPLD
A86	KBD_RST#	Keyboard Reset	I-3.3	PU 3.3 of 10K ohms	5V tolerant input
A87	KBD_A20GATE	A20 gate	I-3.3	PU 3.3 of 10K ohms	
A88	PCIE0_CK_REF+	PCIe Clock (positive)	DP-O	-	-
A89	PCIE0_CK_REF-	PCIe Clock (negative)		-	-
A90	GND (Fixed)	Power Ground	PWR	-	-
A91	SPI_POWER	SPI Power	PWR; 3.3 SUS	-	-
A92	SPI_MISO	SPI Data In	I – 3.3 SUS	PU 3.3 of 15K to 35K ohms	-
A93	GPO0	General Purpose Output 0	O – 3.3		Connected to CPLD
A94	SPI_CLK	SPI Clock	O – 3.3 SUS		
A95	SPI_MOSI	SPI Data Out			
A96	GND (FIXED)	Power Ground	PWR	-	-
A97	TYPE10#	Not connected for Type 2 Rev 2.0 modules	nc	-	-
A98	RSVD	Reserved	nc	-	Rev C PCB is at +12V
A99	RSVD	Reserved	nc		Rev C PCB is at +12V
A100	GND (Fixed)	Power Ground	PWR	-	-
A101	RSVD	Reserved	nc	-	-
A102	RSVD	Reserved	nc	-	-
A103	RSVD	Reserved	nc	-	-
A104	VCC_12V	12V VCC	PWR	-	-
A105	VCC_12V	12V VCC	PWR	-	-
A106	VCC_12V	12V VCC	PWR	-	-
A107	VCC_12V	12V VCC	PWR	-	-
A108	VCC_12V	12V VCC	PWR	-	-

Pin	Signal	Description	Type	Termination	Comment
A109	VCC_12V	12V VCC	PWR	-	-
A110	GND (Fixed)	Power Ground	PWR	-	-

Table 6: Connector X1A - Row B

Pin	Signal	Description	Type	Termination	Comment
B1	GND (Fixed)	Power Ground	PWR	-	-
B2	GBE0_ACT#	Ethernet Activity LED	O-3.3/3.3SUS	-	-
B3	LPC_FRAME#	LPC Frame Indicator	O-3.3	-	-
B4	LPC_AD0	LPC Address / Data Bus	I/O-3.3	-	-
B5	LPC_AD1	LPC Address / Data Bus	I/O-3.3	-	-
B6	LPC_AD2	LPC Address / Data Bus	I/O-3.3	-	-
B7	LPC_AD3	LPC Address / Data Bus	I/O-3.3	-	-
B8	LPC_DRQ0#	LPC DMA request	I-3.3	PU 3.3 of -20K in the ICH8M	-
B9	LPC_DRQ1#	LPC DMA request	I-3.3	PU 3.3 of -20K in the ICH8M	-
B10	LPC_CLK	LPC Clock	O-3.3	-	-
B11	GND (Fixed)	Power Ground	PWR	-	-
B12	PWRBTN#	Power Button Input	I - 3.3 SUS	Weak pullup in the CPLD	-
B13	SMB_CLK	SMBus Clock	I/O-3.3 SUS	PU 3.3 SUS of 2.2K	-
B14	SMB_DAT	SMBus Data	I/O-3.3 SUS	PU 3.3 SUS of 2.2K	-
B15	SMB_ALERT#	SMBus Interrupt	I/O-3.3 SUS	PU 3.3 SUS of 10K	-
B16	SATA1_TX+	SATA 1 Transmit Data+	DP-O	-	-
B17	SATA1_TX-	SATA 1 Transmit Data-		-	-
B18	SUS_STAT#	Indicates imminent suspend	O-3.3 SUS	-	-

Pin	Signal	Description	Type	Termination	Comment
		operation; used to notify LPC devices.			
B19	SATA1_RX+	SATA 1 Receive Data+	DP-I	-	-
B20	SATA1_RX-	SATA 1 Receive Data-		-	-
B21	GND (Fixed)	Power Ground	PWR	-	-
B22	SATA3_TX+	SATA 3 Transmit Data+	Not connected	nc	nc
B23	SATA3_TX-	SATA 3 Transmit Data-	Not connected	nc	nc
B24	PWR_OK	Power OK from power supply	I - 3.3 SUS/5 SUS		Vih = 1.7V
B25	SATA3_RX+	SATA 3 Receive Data+	Not connected	nc	nc
B26	SATA3_RX-	SATA 3 Receive Data-	Not connected	nc	nc
B27	WDT	Indicator for Watchdog Timeout	O - 3.3	-	-
B28	AC/HDA_SDIN2	Audio CODEC Serial Data In 2	I - 3.3 SUS	PD of 20K in the ICH8M	-
B29	AC/HDA_SDIN1	Audio CODEC Serial Data In 1	I - 3.3 SUS	PD of 20K in the ICH8M	-
B30	AC/HDA_SDIN0	Audio CODEC Serial Data In 0	I - 3.3 SUS	PD of 20K in the ICH8M	-
B31	GND (Fixed)	Power Ground	PWR	-	-
B32	SPKR	Speaker Interface	O -3 .3	-	-
B33	I2C_CK	I^2C Clock	I/O - 3.3 SUS	PU 3.3 SUS of 2.2K	-
B34	I2C_DAT	I^2C Data	I/O - 3.3 SUS	PU 3.3 SUS of 2.2K	-
B35	THRM#	Over Temperature Indicator	I - 3.3	PU 3.3 of 10K	-
B36	USB7-	USB Data- Port #7	DP-I/O	-	Hooked to USB port #9 on the ICH8M.
B37	USB7+	USB Data+ Port #7		-	
B38	USB_4_5_OC#	USB Over current Pair 4/5	I-3.3 SUS	PU 3.3 SUS of 10K	Hooked to over current pin 6/7 of ICH8M.
B39	USB5-	USB Data- Port #5	DP-I/O	-	Hooked to USB port #7 on the ICH8M.
B40	USB5+	USB Data+ Port #5		-	

Pin	Signal	Description	Type	Termination	Comment
B41	GND (Fixed)	Power Ground	PWR	-	-
B42	USB3-	USB Data- Port #3	DP-I/O	-	Hooked to USB port #3 on the ICH8M.
B43	USB3+	USB Data+ Port #3		-	
B44	USB_0_1_OC#	USB Over current Pair 0/1	I-3.3 SUS	PU 3.3 SUS of 10K	Hooked to over current pin 0/1 of ICH8M.
B45	USB1-	USB Data- Port #1	DP-I/O	-	Hooked to USB port #1 on the ICH8M.
B46	USB1+	USB Data+ Port #1		-	
B47	EXCD1_PERST#	PCIe Express Card 1 Reset	O-3.3	-	Connected to ICH8M pin GPIO6.
B48	EXCD1_CPPE#	PCIe Express Card 1 Request	I-3.3	PU 3.3 of 10K	Connected to ICH8M pin GPIO12.
B49	SYS_RESET#	Reset button input	I-3.3	PU 3.3 SUS of 10K	-
B50	CB_RESET#	Carrier Board Reset	O-3.3 SUS	-	-
B51	GND (Fixed)	Power Ground	PWR	-	-
B52	PCIE_RX5+	PCIe 5 Receive Data+	Not connected	nc	nc
B53	PCIE_RX5-	PCIe 5 Receive Data-	Not connected	nc	nc
B54	GPO1	General Purpose Output 1	O-3.3	-	Connected to CPLD
B55	PCIE_RX4+	PCIe 4 Receive Data+	DP-I	-	-
B56	PCIE_RX4-	PCIe 4 Receive Data-		-	-
B57	GPO2	General Purpose Output 2	O-3.3	-	Connected to CPLD
B58	PCIE_RX3+	PCIe 3 Receive Data+	DP-I	-	-
B59	PCIE_RX3-	PCIe 3 Receive Data-		-	-
B60	GND (Fixed)	Power Ground	PWR	-	-
B61	PCIE_RX2+	PCIe 2 Receive Data+	DP-I	-	
B62	PCIE_RX2-	PCIe 2 Receive Data-		-	
B63	GPO3	General Purpose Output 3	O-3.3		Connected to CPLD
B64	PCIE_RX1+	PCIe 1 Receive	DP-I	-	-

Pin	Signal	Description	Type	Termination	Comment
		Data+			
B65	PCIE_RX1-	PCIe 1 Receive Data-		-	-
B66	WAKE0#	PCI Express Wake Event	I-3.3 SUS	PU 3.3 SUS of 10K	Connected to ICH8M pin WAKE
B67	WAKE1#	General Purpose Wake Event	I-3.3 SUS	PU 3.3 SUS of 10K	Connected to ICH8M pin RI#
B68	PCIE_RX0+	PCIe 0 Receive Data+	DP-I	-	-
B69	PCIE_RX0-	PCIe 0 Receive Data-		-	-
B70	GND (Fixed)	Power Ground	PWR	-	-
B71	LVDS_B0+	LVDS Display Channel B0 (Positive)	Not connected	nc	nc
B72	LVDS_B0-	LVDS Display Channel B0 (Negative)	Not connected	nc	nc
B73	LVDS_B1+	LVDS Display Channel B1 (Positive)	Not connected	nc	nc
B74	LVDS_B1-	LVDS Display Channel B1 (Negative)	Not connected	nc	nc
B75	LVDS_B2+	LVDS Display Channel B 2(Positive)	Not connected	nc	nc
B76	LVDS_B2-	LVDS Display Channel B2 (Negative)	Not connected	nc	nc
B77	LVDS_B3+	LVDS Display Channel B3 (Positive)	Not connected	nc	nc
B78	LVDS_B3-	LVDS Display Channel B 3(Negative)	Not connected	nc	nc
B79	LVDS_BKLT_EN	LVDS Display Backlight Enable	O-3.3	PD 4.75K.	-
B80	GND (Fixed)	Power Ground	PWR	-	-
B81	LVDS_B_CK+	LVDS Display Channel B Clock+	Not connected	nc	nc
B82	LVDS_B_CK-	LVDS Display Channel B Clock-	Not connected	nc	nc
B83	LVDS_BKLT_CTRL	LVDS Display Backlight Brightness	O-3.3	-	-

Pin	Signal	Description	Type	Termination	Comment
B84	VCC_5V_SBY	+5V Standby	PWR	-	-
B85	VCC_5V_SBY	+5V Standby	PWR	-	-
B86	VCC_5V_SBY	+5V Standby	PWR	-	-
B87	VCC_5V_SBY	+5V Standby	PWR	-	-
B88	BIOS_DIS1#	BIOS Disable	I - 3.3 SUS	PU 3.3V SUS of 51.1K ohms	-
B89	VGA_RED	Analog video	O - Analog	-	-
B90	GND (Fixed)	Power Ground	PWR	-	-
B91	VGA_GRN	Analog video	O - Analog	-	-
B92	VGA_BLU	Analog video	O - Analog	-	-
B93	VGA_HSYNC	Horizontal Sync	O - 3.3	-	-
B94	VGA_VSYNC	Vertical Sync	O - 3.3	-	-
B95	VGA_I2C_CK	DDC Clock	I/O - 3.3	PU 3.3V of 4.75K	-
B96	VGA_I2C_DAT	DDC Data	I/O - 3.3	PU 3.3V of 4.75K	-
B97	SPI_CS#	Carrier board SPI chip select	O - 3.3 SUS	-	
B98	RSVD	Reserved	-	-	-
B99	RSVD	Reserved	-	-	-
B100	GND (Fixed)	Power Ground	PWR	-	-
B101	RSVD	Reserved	-	-	-
B102	RSVD	Reserved	-	-	-
B103	RSVD	Reserved	-	-	-
B104	VCC_12V	12V VCC	PWR	-	-
B105	VCC_12V	12V VCC	PWR	-	-
B106	VCC_12V	12V VCC	PWR	-	-
B107	VCC_12V	12V VCC	PWR	-	-
B108	VCC_12V	12V VCC	PWR	-	-
B109	VCC_12V	12V VCC	PWR	-	-
B110	GND (Fixed)	Power Ground	PWR		

NOTE: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the PICMG COM Express® Design Guide for information about additional termination resistors.

Table 7: Connector X1B - Row C

Pin	Signal	Description	Type	Termination	Comment
C1	GND (Fixed)	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus 7	I/O - 3.3	-	5V tolerant input
C3	IDE_D6	IDE Data Bus 6	I/O - 3.3	-	5V tolerant input
C4	IDE_D3	IDE Data Bus 3	I/O - 3.3	-	5V tolerant

Pin	Signal	Description	Type	Termination	Comment
					input
C5	IDE_D15	IDE Data Bus 15	I/O – 3.3	-	5V tolerant input
C6	IDE_D8	IDE Data Bus 8	I/O – 3.3	-	5V tolerant input
C7	IDE_D9	IDE Data Bus 9	I/O – 3.3	-	5V tolerant input
C8	IDE_D2	IDE Data Bus 2	I/O – 3.3	-	5V tolerant input
C9	IDE_D13	IDE Data Bus 13	I/O – 3.3	-	5V tolerant input
C10	IDE_D1	IDE Data Bus1	I/O – 3.3	-	5V tolerant input
C11	GND (Fixed)	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus 14	I/O – 3.3	-	5V tolerant input
C13	IDE_IORDY	IDE I/O Ready	I – 3.3V	PU 3.3 of 4.75K	5V tolerant input
C14	IDE_IOR#	IDE I/O Ready	O – 3.3V		
C15	PCI_PME#	PCI Power Management Event	I – 3.3 SUS		5V tolerant input
C16	PCI_GNT2#	PCI Bus Grant 2	O-3.3	-	-
C17	PCI_REQ2#	PCI Bus Request 2	I – 3.3	PU 3.3 of 8.2K	5V tolerant input
C18	PCI_GNT1#	PCI Bus Grant 1	O-3.3	-	-
C19	PCI_REQ1#	PCI Bus Request 1	I – 3.3	PU 3.3 of 8.2K	5V tolerant input
C20	PCI_GNT0#	PCI Bus Grant 0	O-3.3	-	-
C21	GND (Fixed)	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Request 0	I – 3.3	PU 3.3 of 8.2K	5V tolerant input
C23	PCI_RST#	PCI Bus Reset	O – 3.3 SUS		5V tolerant input
C24	PCI_AD0	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C25	PCI_AD2	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input -
C26	PCI_AD4	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input -
C27	PCI_AD6	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C28	PCI_AD8	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C29	PCI_AD10	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C30	PCI_AD12	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input

Pin	Signal	Description	Type	Termination	Comment
C31	GND (Fixed)	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Address and Data Bus line	I/O – 3.3		5V tolerant input
C33	PCI_C/BE1#	PCI Bus Command and Byte Enable1	I/O – 3.3		5V tolerant input
C34	PCI_PERR#	PCI Bus Parity Error	I/O – 3.3	PU 3.3 of 8.2K	5V tolerant input
C35	PCI_LOCK#	PCI Bus Lock	I/O – 3.3	PU 3.3 of 8.2K	5V tolerant input
C36	PCI_DEVSEL#	PCI Bus Device Select	I/O – 3.3	PU 3.3 of 8.2K	5V tolerant input
C37	PCI_IRDY#	PCI Bus Initiator Ready	I/O – 3.3	PU 3.3 of 8.2K	5V tolerant input
C38	PCI_C/BE2#	PCI Bus Command and Byte enable 2	I/O – 3.3	-	5V tolerant input
C39	PCI_AD17	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C40	PCI_AD19	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C41	GND (Fixed)	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C43	PCI_AD23	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C44	PCI_C/BE3#	PCI Bus Command and Byte enables 3	I/O – 3.3	-	5V tolerant input
C45	PCI_AD25	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C46	PCI_AD27	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C47	PCI_AD29	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C48	PCI_AD31	PCI Address and Data Bus line	I/O – 3.3	-	5V tolerant input
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I – 3.3	PU 3.3 of 8.2K	5V tolerant input
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I – 3.3	PU 3.3 of 8.2K	5V tolerant input
C51	GND (Fixed)	Power Ground	PWR	-	-
C52	PEG_RX0+	PCIe Graphics	Not	nc	nc

Pin	Signal	Description	Type	Termination	Comment
		Receive+ (0)	connected		
C53	PEG_RX0-	PCIe Graphics Receive- (0)	Not connected	nc	nc
C54	TYPE0#	Not connected for Type 2 module	Not connected	nc	nc
C55	PEG_RX1+	PCIe Graphics Receive+ (1)	Not connected	nc	nc
C56	PEG_RX1-	PCIe Graphics Receive- (1)	Not connected	nc	nc
C57	TYPE1#	Not connected for Type 2 module	Not connected	nc	nc
C58	PEG_RX2+	PCIe Graphics Receive+ (2)	Not connected	nc	nc
C59	PEG_RX2-	PCIe Graphics Receive- (2)	Not connected	nc	nc
C60	GND (Fixed)	Power Ground	PWR	-	-
C61	PEG_RX3+	PCIe Graphics Receive+ (3)	Not connected	nc	nc
C62	PEG_RX3-	PCIe Graphics Receive- (3)	Not connected	nc	nc
C63	RSVD	Reserved	Not connected	nc	nc
C64	RSVD	Reserved	Not connected	nc	nc
C65	PEG_RX4+	PCIe Graphics Receive+ (4)	Not connected	nc	nc
C66	PEG_RX4-	PCIe Graphics Receive- (4)	Not connected	nc	nc
C67	RSVD	Reserved	Not connected	nc	nc
C68	PEG_RX5+	PCIe Graphics Receive+ (5)	Not connected	nc	nc
C69	PEG_RX5-	PCIe Graphics Receive- (5)	Not connected	nc	nc
C70	GND (Fixed)	Power Ground	PWR	-	-
C71	PEG_RX6+	PCIe Graphics Receive+ (6)	Not connected	nc	nc
C72	PEG_RX6-	PCIe Graphics Receive- (6)	Not connected	nc	nc
C73	SDVO_DATA	SDVO Controller Data	Not connected	nc	nc
C74	PEG_RX7+	PCIe Graphics Receive+ (7)	Not connected	nc	nc
C75	PEG_RX7-	PCIe Graphics Receive- (7)	Not connected	nc	nc
C76	GND (Fixed)	Power Ground	PWR	-	-

Pin	Signal	Description	Type	Termination	Comment
C77	RSVD	Reserved	Not connected	nc	nc
C78	PEG_RX8+	PCIe Graphics Receive+ (8)	Not connected	nc	nc
C79	PEG_RX8-	PCIe Graphics Receive- (8)	Not connected	nc	nc
C80	GND (Fixed)	Power Ground	PWR	-	-
C81	PEG_RX9+	PCIe Graphics Receive+ (9)	Not connected	nc	nc
C82	PEG_RX9-	PCIe Graphics Receive- (9)	Not connected	nc	nc
C83	RSVD	Reserved	Not connected	nc	nc
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	PCIe Graphics Receive+ (10)	Not connected	nc	nc
C86	PEG_RX10-	PCIe Graphics Receive- (10)	Not connected	nc	nc
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	PCIe Graphics Receive+ (11)	Not connected	nc	nc
C89	PEG_RX11-	PCIe Graphics Receive- (11)	Not connected	nc	nc
C90	GND (Fixed)	Power Ground	PWR	-	-
C91	PEG_RX12+	PCIe Graphics Receive+ (12)	Not connected	nc	nc
C92	PEG_RX12-	PCIe Graphics Receive- (12)	Not connected	nc	nc
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	PCIe Graphics Receive+ (13)	Not connected	nc	nc
C95	PEG_RX13-	PCIe Graphics Receive- (13)	Not connected	nc	nc
C96	GND	Power Ground	PWR	-	-
C97	RSVD	Reserved	Not connected	nc	nc
C98	PEG_RX14+	PCIe Graphics Receive+ (14)	Not connected	nc	nc
C99	PEG_RX14-	PCIe Graphics Receive- (14)	Not connected	nc	nc
C100	GND (Fixed)	Power Ground	PWR	-	-
C101	PEG_RX15+	PCIe Graphics	Not	nc	nc

Pin	Signal	Description	Type	Termination	Comment
		Receive+ (15)	connected		
C102	PEG_RX15-	PCIe Graphics Receive- (15)	Not connected	nc	nc
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	-
C105	VCC_12V	12V VCC	PWR	-	-
C106	VCC_12V	12V VCC	PWR	-	-
C107	VCC_12V	12V VCC	PWR	-	-
C108	VCC_12V	12V VCC	PWR	-	-
C109	VCC_12V	12V VCC	PWR	-	-
C110	GND (Fixed)	Power Ground	PWR	-	-

NOTE: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the PICMG COM Express® Design Guide for information about additional termination resistors.

Table 8: Connector X1B - Row D

Pin	Signal	Description	Type	Termination	Comment
D1	GND (Fixed)	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus 5	I/O	-	5V tolerant input
D3	IDE_D10	IDE Data Bus 10	I/O	-	5V tolerant input
D4	IDE_D11	IDE Data Bus 11	I/O	-	5V tolerant input
D5	IDE_D12	IDE Data Bus 12	I/O	-	5V tolerant input
D6	IDE_D4	IDE Data Bus 4	I/O	-	5V tolerant input
D7	IDE_D0	IDE Data Bus 0	I/O	-	5V tolerant input
D8	IDE_REQ	IDE Data Bus	I/O	-	5V tolerant input
D9	IDE_IOW#	IDE I/O Write	O - 3.3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O - 3.3	-	-
D11	GND (Fixed)	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I - 3.3	PU 3.3 of 8.2K	5V tolerant input
D13	IDE_A0	IDE Address Bus 0	O - 3.3	-	-
D14	IDE_A1	IDE Address Bus 1	O - 3.3	-	-

Pin	Signal	Description	Type	Termination	Comment
D15	IDE_A2	IDE Address Bus 2	O - 3.3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 1	O - 3.3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 3	O - 3.3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O - 3.3	-	-
D19	PCI_GNT3#	PCI Bus Grant 3	O - 3.3		-
D20	PCI_REQ3#	PCI Bus Request 3	I -3 .3	PU 3.3 of 8.2K	5V tolerant input
D21	GND (Fixed)	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D23	PCI_AD3	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D24	PCI_AD5	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D25	PCI_AD7	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D26	PCI_C/BE0#	PCI Command and Byte Enable 0	I/O - 3.3	-	5V tolerant input
D27	PCI_AD9	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D28	PCI_AD11	PCI Address and Data Bus line	I/O-3.3	-	5V tolerant input
D29	PCI_AD13	PCI Address and Data Bus line	I/O-3.3	-	5V tolerant input
D30	PCI_AD15	PCI Address and Data Bus line	I/O-3.3	-	5V tolerant input
D31	GND (Fixed)	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	I/O - 3.3	-	5V tolerant input
D33	PCI_SERR#	PCI Bus System Error	I/OD - 3.3	PU 3.3 of 8.2K	5V tolerant input
D34	PCI_STOP#	PCI Bus Stop	I/O - 3.3	PU 3.3 of 8.2K	5V tolerant input
D35	PCI_TRDY#	PCI Bus Target Ready	I/O - 3.3	PU 3.3 of 8.2K	5V tolerant input
D36	PCI_FRAME#	PCI Bus Cycle Frame	I/O - 3.3	PU 3.3 of 8.2K	5V tolerant input
D37	PCI_AD16	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D38	PCI_AD18	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input

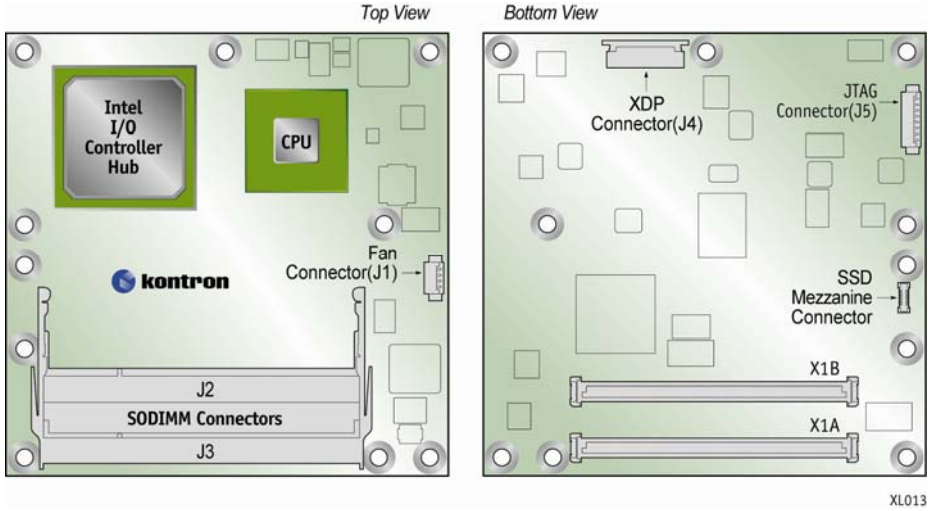
Pin	Signal	Description	Type	Termination	Comment
D39	PCI_AD20	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D40	PCI_AD22	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D41	GND (Fixed)	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D43	PCI_AD26	PCI Address and Data Bus line	I/O -3 .3	-	5V tolerant input
D44	PCI_AD28	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D45	PCI_AD30	PCI Address and Data Bus line	I/O - 3.3	-	5V tolerant input
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I - 3.3	PU 3.3 of 8.2K	5V tolerant input
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I - 3.3	PU 3.3 of 8.2K	5V tolerant input
D48	PCI_CLKRUN#	PCI Clock Run	I - 3.3	PU 3.3 of 8.2K	Not 5V tolerant per the COM.0 spec
D49	PCI_M66EN	PCI_M66EN	Not connected	nc	nc
D50	PCI_CLK	PCI Clock	O-3.3	-	-
D51	GND (Fixed)	Power Ground	PWR	-	-
D52	PEG_TX0+	PCIe Graphics Transmit+ (0)	Not connected	nc	nc
D53	PEG_TX0-	PCIe Graphics Transmit- (0)	Not connected	nc	nc
D54	PEG_LANE_RV#	PCIe Graphics Lane Reversal	Not connected	nc	nc
D55	PEG_TX1+	PCIe Graphics Transmit+ (1)	Not connected	nc	nc
D56	PEG_TX1-	PCIe Graphics Transmit- (1)	Not connected	nc	nc
D57	TYPE2#	Note connected for Type 2 modules	Not connected	nc	nc
D58	PEG_TX2+	PCIe Graphics Transmit+ (2)	Not connected	nc	nc
D59	PEG_TX2-	PCIe Graphics Transmit- (2)	Not connected	nc	nc
D60	GND (fixed)	Power Ground	PWR	-	-
D61	PEG_TX3+	PCIe Graphics Transmit+ (3)	Not connected	nc	nc

Pin	Signal	Description	Type	Termination	Comment
D62	PEG_TX3-	PCIe Graphics Transmit- (3)	Not connected	nc	nc
D63	RSVD	Reserved	Not connected	nc	nc
D64	RSVD	Reserved	Not connected	nc	nc
D65	PEG_TX4+	PCIe Graphics Transmit+ (4)	Not connected	nc	nc
D66	PEG_TX4-	PCIe Graphics Transmit- (4)	Not connected	nc	nc
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	PCIe Graphics Transmit+ (5)	Not connected	nc	nc
D69	PEG_TX5-	PCIe Graphics Transmit- (5)	Not connected	nc	nc
D70	GND (Fixed)	Power Ground	PWR	-	-
D71	PEG_TX6+	PCIe Graphics Transmit+ (6)	Not connected	nc	nc
D72	PEG_TX6-	PCIe Graphics Transmit- (6)	Not connected	nc	nc
D73	SDVO_CLK	SDVO Clock	Not connected	nc	nc
D74	PEG_TX7+	PCIe Graphics Transmit+ (7)	Not connected	nc	nc
D75	PEG_TX7-	PCIe Graphics Transmit- (7)	Not connected	nc	nc
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE Cable Type Identification	I - 3.3	PD of 10K	Not 5V tolerant per the COM.0 spec. Connected to ICH8M pin GPIO38.
D78	PEG_TX8+	PCIe Graphics Transmit+ (8)	Not connected	nc	nc
D79	PEG_TX8-	PCIe Graphics Transmit- (8)	Not connected	nc	nc
D80	GND (Fixed)	Power Ground	PWR	-	-
D81	PEG_TX9+	PCIe Graphics Transmit+ (9)	Not connected	nc	nc
D82	PEG_TX9-	PCIe Graphics Transmit- (9)	Not connected	nc	nc
D83	RSVD	Reserved	Not connected	nc	nc
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	PCIe Graphics Transmit+ (10)	Not connected	nc	nc
D86	PEG_TX10-	PCIe Graphics Transmit- (10)	Not connected	nc	nc
D87	GND	Power Ground	PWR	-	-

Pin	Signal	Description	Type	Termination	Comment
D88	PEG_TX11+	PCIe Graphics Transmit+ (11)	Not connected	nc	nc
D89	PEG_TX11-	PCIe Graphics Transmit- (11)	Not connected	nc	nc
D90	GND (Fixed)	Power Ground	PWR	-	-
D91	PEG_TX12+	PCIe Graphics Transmit+ (12)	Not connected	nc	nc
D92	PEG_TX12-	PCIe Graphics Transmit- (12)	Not connected	nc	nc
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	PCIe Graphics Transmit+ (13)	Not connected	nc	nc
D95	PEG_TX13-	PCIe Graphics Transmit- (13)	Not connected	nc	nc
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE#	PEG Enable	Not connected	nc	nc
D98	PEG_TX14+	PCIe Graphics Transmit+ (14)	Not connected	nc	nc
D99	PEG_TX14-	PCIe Graphics Transmit- (14)	Not connected	nc	nc
D100	GND (Fixed)	Power Ground	PWR	-	-
D101	PEG_TX15+	PCIe Graphics Transmit+ (15)	Not connected	nc	nc
D102	PEG_TX15-	PCIe Graphics Transmit- (15)	Not connected	nc	nc
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	-
D105	VCC_12V	12V VCC	PWR	-	-
D106	VCC_12V	12V VCC	PWR	-	-
D107	VCC_12V	12V VCC	PWR	-	-
D108	VCC_12V	12V VCC	PWR	-	-
D109	VCC_12V	12V VCC	PWR	-	-
D110	GND (Fixed)	Power Ground	PWR	-	-

NOTE: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the PICMG COM Express® Design Guide for information about additional termination resistors.

Figure 4: Onboard Connectors



4.1.2Connector J1 – Fan

J1 is the 4-pin connector for a fan. J1 can be configured in the BIOS setup. See Section 6.3, "Onboard Fan Connector" for more detailed information.

Although the module is functional without active cooling, it is advised that a minimal airflow be maintained within the system to ensure components do not overheat.

Table 9: J1 Fan Connector Pin-Out

Pin	Name
1	FAN_TACH
2	FAN_V_IN
3	FAN_GND
4	V_5V

4.1.3Connectors J2 and J3 – SODIMM DDR2 Memory Sockets

This design supports up to 2 GBytes (single channel) of DDR2 memory with two 200-pin sockets.

4.1.4Connector J4 - XDP

The eXtended Debug Port (XDP) connector is a 24-pin connector used for debugging the board.

NOTE: This connector is for development debug purposes only. The XDP connector pin-out is under NDA.

4.1.5Connector J5 –JTAG

This is the Intel® ICH8M debug connector.

WARNING: The debug port is for internal use only. Do not connect any devices.

Table 10: J5 JTAG Connector Pin-Out

Pin	Name	Termination
1	V_3V3_S5	-
2	CPLD_TDI	PU to 3.3V SUS of 1K.
3	CPLD_TCK	PD to 1K.
4	CPLD_TMS	PU to 3.3V SUS of 1K.
5	CPLD_TDO	PU to 3.3V SUS of 1K.
6	GND	-
7	KILL_POWER_UP#	PU 5K to 25K in the CPLD.
8	GND	-

4.1.6SSD Mezzanine Connector

The optional onboard SSD module interface uses SATA to connect to port 2 the Intel® ICH8M.

Table 11: J6 SSD Connector Pin-Out

Pin	Name
1	GND
2	GND
3	GND
4	SATA_RX+
5	V_3V3
6	SATA_RX-
7	V_3V3
8	GND
9	V_3V3
10	SATA_TX+
11	NC
12	SATA_TX-
13	RESET
14	GND

4.1.7PCI Express Interface

The PCI Express* x1 lane is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the ETXexpress® COM Express Specification. Refer to the PICMG COM Express® Design Guide for additional implementation information.

The microETXexpress®-PV COM supports up to 5 PCI Express x1 lanes. See Table 12 for detailed configuration information.

Table 12: PCI Express Configurations

PCIExpress Ports	Config. 1	Config. 2	Config. 3	Config. 4
Port 0	x4 Port	x2 Port	x2 Port	x1 Port
Port 1				x1 Port
Port 2		x2 Port	x1 Port	x1 Port
Port 3			x1 Port	x1 Port
Port 4	x1 Port	x1 Port	x1 Port	x1 Port

4.1.8USB Interface

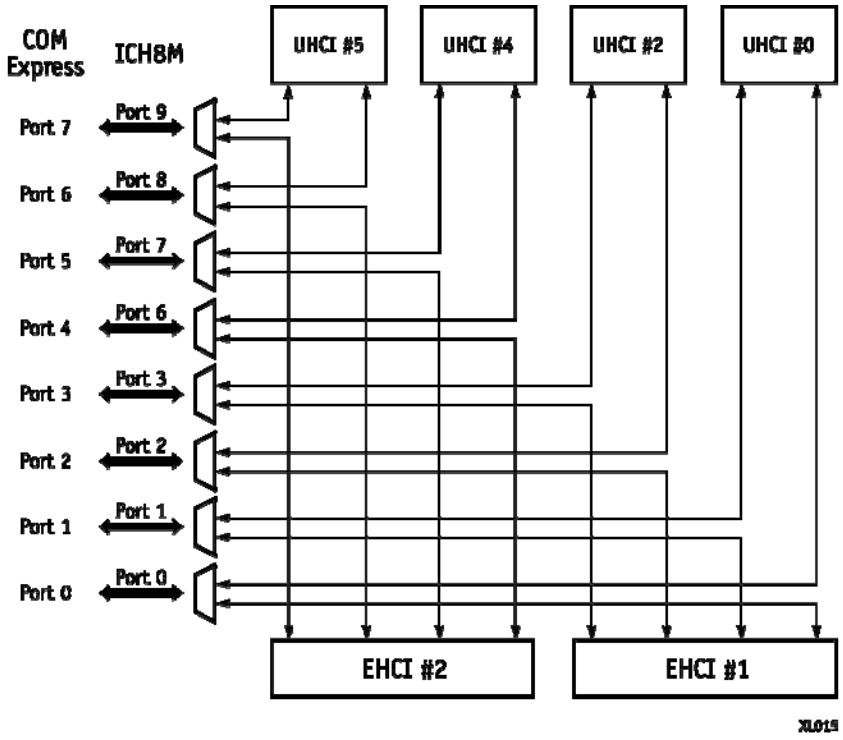
The USB interface has five UHCI (USB 1.1) controllers and two EHCI (USB 2.0) controllers. Not all of the UHCI controllers are used. Table 13 shows how eight USB ports are used for USB configuration in the microETXexpress®-PV module.

Table 13: USB Configuration

COMexpress™ Port	ICH8M Port	Description
USB0	USB0	Either USB 1.1 (UHCI1) or USB 2.0 (EHC1)
USB1	USB1	Either USB 1.1 (UHCI1) or USB 2.0 (EHC1)
USB2	USB2	Either USB 1.1 (UHCI2) or USB 2.0 (EHC1)
USB3	USB3	Either USB 1.1 (UHCI2) or USB 2.0 (EHC1)
USB4	USB6	Either USB 1.1 (UHCI4) or USB 2.0 (EHC2)
USB5	USB7	Either USB 1.1 (UHCI4) or USB 2.0 (EHC2)
USB6	USB8	Either USB 1.1 (UHCI5) or USB 2.0 (EHC2)
USB7	USB9	Either USB 1.1 (UHCI5) or USB 2.0 (EHC2)

Figure 5 shows the internal USB mapping from the Intel® ICH8M.

Figure 5: USB Mapping



NOTE: Additional USB connections can be added using external USB hubs.

Configuration

The USB controllers are PCI bus devices. The BIOS allocates the required system resources during configuration of the PCI bus.

4.1.9SATA Interface

NOTE: If you are installing your operating system on a SATA hard drive in AHCI mode, you might need to install the driver when prompted. To obtain this driver, go to the Kontron microETXexpress®-PV COM download page at http://emdcustomersection.kontron.com/.

Configuration

The SATA controller is part of the ICH8M.

4.1.10 Audio Interface

The Intel® ICH8M supports Intel® High Definition Audio (HDA). This HD audio configuration supports up to four audio streams (with up to 16 channels each), 32-bit sample depth, and sample rates up to 192 KHz.

With this configuration you can implement hardware CODECs on your baseboard for 7.1/5.1 audio systems and SDIF output. The pins for the HD audio are defined in Section 4.1, Pin-Outs.

WARNING: This feature is only supported with baseboards that have an HD audio CODEC.

Configuration

The audio controller is in the Intel® ICH8M. The BIOS allocates the required system resources during configuration.

4.1.11 Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in "Continuous Mode".

4.1.12 Graphics Interface

The microETXexpress®-PV uses the Intel® Graphics Media Accelerator 3150 (Intel® GMA 3150) with a 400 MHz GPU clock for the D410/D510 Atom processors and 200MHz for the N450 Atom processor. This controller, which is integrated in the Intel® Atom processor, delivers advanced 3D video capabilities. The graphics engine supports multiple display types (LVDS, VGA, DVI-I, HDTV, and CRT), and resolutions up to 2048x1536 VGA mode for the modules with the D510 and D410 processors. Module with the N450 CPU support resolution of 1400x1050.

The GMA uses the processor RAM for graphics memory. The pre-allocated memory is defined through BIOS settings.

VGA

The analog VGA graphics core, with a maximum resolution of 1400x1050 (Modules with the N450 CPU), is integrated in the processor. Modules with the D410 and D510 CPU support 2048x1536 resolution.

LVDS Flat Panel Interface (JILI)

The Intel® Atom processor has integrated 18-bit single channel LVDS for WXGA. The user interface for flat panels is the JUMPtec* Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the COM Express® specification. For additional implementation information, refer to the ***PICMG COM Express® Design Guide*** on the PIGMG website.

4.1.13 Ethernet Interface

The Ethernet interface on the microETXexpress®-PV COM is the Intel® 82567LM 10/100/1000 Mbit Gigabit Ethernet PHY. The GbE PHY is connected to the GLCI/LCI of the ICH8M. The controller supports a 10/100/1000 Base-T interface and it auto-negotiates the use of 10 Mbit/sec, 100 Mbit/sec or 1Gbit/sec connections.

The interface supports functions such as WOL (WakeOnLAN) and PXE (Preboot eXecution Environment) boot.

For cable lengths and terminations on your baseboard, refer to the PICMG ***COM Express® Design G***uide on the PICMG website.

Configuration

The Ethernet controller is a PCI Express bus device. The BIOS allocates the required system resources during the configuration of the PCIe device.

4.1.14 SPI Bus Interface

The Serial Peripheral Interface (SPI) signals are connected to the Intel® ICH8M hub with pins that were previously reserved on the COM Express® connector. The SPI interface can be used to connect one carrier board devices, including external BIOS flash memory. The implementation of this subsystem complies with the COM Express® specification. For additional implementation information, refer to the ***PICMG COM Express® Design Guide*** on the PICMG website

4.1.15 LPC Bus Interface

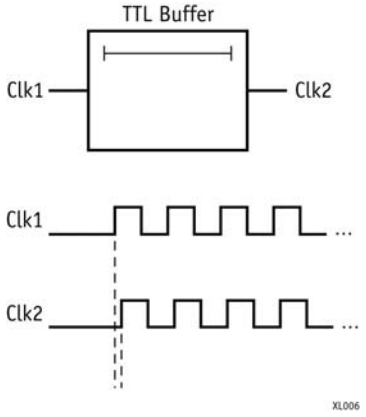
The Low Pin Count (LPC) interface signals are connected to the Intel® ICH8M. The LPC low-speed interface can be used for peripheral circuits. For example,

it can be used as an external super I/O controller to combine legacy-device support into a single IC. The implementation of this subsystem complies with the COM Express® specification. For additional implementation information, refer to the ***PICMG COM Express® Design Guide*** on the PICMG website.

The LPC bus does not support DMA (Direct Memory Access) and therefore imposes limitations for ISA bus and standard I/Os (SIOs) like floppy or LPT interface implementations.

WARNING: Connecting more than one device to the LPC bus requires using a clock buffer. Because of the power management of the LPC bus, you must use great care with clock buffers that require synchronization as they could prevent the board from booting up.

Figure 6: Standard Clock Buffer



NOTE: When using a standard clock buffer on the baseboard, be aware that the generated delay must be considered for the length matching of the layout.

Clock Buffer Reference Schematic

The schematic in Figure 7 shows an implementation example for the clock buffer.

Figure 7: LPC Clock Buffer

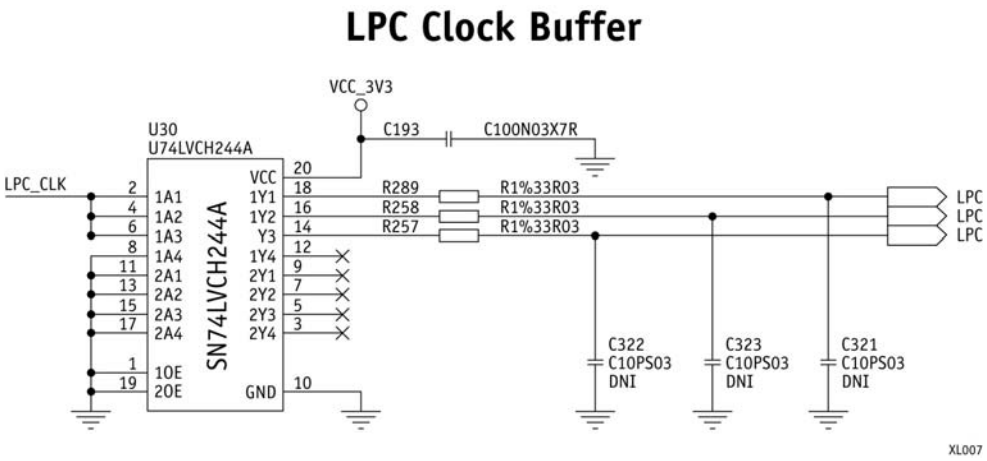


Table 14: LPC Addresses

Address (HEX)	Device
0000 – 00FF	IBM PC compatible devices (IRQ-Controller, Keyboard, RTC, etc.)
002E-002F	Optional: Super I/O W83627
01F0 – 01F7	Fixed Disk
03C0 – 03CF	VGA/EGA compatible registers
03F6	Fixed Disk
0400 – 041F	SMBus
0500 – 053F	GPIO ICH
04D0 – 04D1	IRQ Configuration
0800 – 087F	Power Management
0A00 – 0A2F	CPLD I/O
0A20 – 0A2F	SIO HWM (if present)
0CF8 – 0CFF	PCI Configuration
C400 – C41F	PCI USB Controller *
C480 – C49F	PCI USB Controller *
C000 – C007	PCI VGA Controller *
EF00 – EF1F	PCI USB Controller*
FFA0 – FFAF	PCI IDE Controller *

* = not fixed, configured by the BIOS automatically and may be different in other system configurations.

Table 15: Device Addresses

Address (HEX)	Device
00000000 – 0009FFFF	DOS- (Real mode-) memory
000A0000 – 000BFFFF	Display memory

000C0000 - 000CBFFF	VGA BIOS
000CC000 - 000DFFFF	Other Option ROM
000E0000 - 000EFFFF	System BIOS extended space
000F0000 - 000FFFFF	System BIOS base segment
00100000 - 7FFFFFFF	System Memory
80000000 - FFF00000	PCI Memory, other extensions
CFDDC000 - CFFFFFFF	PCI LAN Controller
D0000000 - DFFFFFFF	PCI VGA Controller / Audio Controller / USB Controller
FEC00000 - FEC00040	APIC Configuration
FED00000 - FED003FF	Event Timer
FED10000 - dynamic	Audio Controller
FED40000 - FED4BFFF	LPC Configuration
F0000000 - F0003FFF	RCRB (Root Complex)
FFC00000 - FFF00000	Reserved
FFF00000 - FFFFFFFF	Firmware Hub
FFF80000 - FFFFFFFF	Mapping space for BIOS ROM

For further details, please refer to the processor and I/O controller hub information on the Intel website at http://www.intel.com.

4.1.16 Power Control Interface

Power Good (PWR_OK)

The microETXexpress®-PV COM provides an external input for a power-good signal (pin B24). The implementation of this subsystem complies with the COM Express® Specification. PWR_OK must be high-level (> 1.7V) to power on the module in normal ATX mode.

Power Button (PWRBTN#)

The power button (pin B12) is available through the module connector as defined in the pin-out list. To start the module using the power button the PWRBTN# signal must be at least 50ms (50ms ≤ t < 4sec) at low-level power.

To force a power-off the module, press and hold the power button for at least four seconds. Depending on the OS in use, only one press of the Power button initiate the clean power down of the module.

Reset Button (SYS_RESET#)

The reset button (pin B49) is available through the module connector as defined in the pin-out list. The module stays in reset as long as SYS_RESET# is grounded.

WARNING: Please note that in order to fulfill the COM Express requirements, pressing the reset button will cause a complete power cycle.

Power Supply

The microETXexpress®-PV COM has a wide range of power input, from 4.75V to 18V DC. The supply voltage is applied through 24 pins (VCC) on the module connectors. In ATX mode with 5V standby voltage, the VCC input must be higher than the standby voltage.

In general, single supply mode means that the module is able to function with a single supply (no standby voltage is necessary). All other functions attributed to the ATX mode remain functional.

ATX Mode / Single Supply Mode

ATX Mode:

When an ATX power supply is connected, PWR_OK is set to low-level and VCC is off. Pressing the power button enables the ATX PSU setting PWR_OK to high-level and powers on VCC. The ATX PSU is controlled by the PS_ON# signal, which is generated by SUS_S3# via inversion.

Table 16: ATX Mode

State	PWRBTN#	PWR_OK	V5_StdBy	PS_ON#	VCC
S3	x	x	5V	x	0V
S5	high	low	5V	high	0V
S5 -> S0	PWRBTN Event	low -> high	5V	high -> low	0 V-> VCC
S0	high	high	5V	low	VCC

Single Supply (Battery) Mode:

To enable the single supply mode the BIOS setup must be changed. The "Battery Mode" must be enabled from the Boot menu. Setting "Power Scheme" option to "Battery Mode" in the BIOS will enable the following features:

» The PWR_OK# state is ignored and the input voltage monitoring will be enabled

An internal voltage monitor will let the board start (after a power button event or self-power up) when the input voltage is above 4.75V. The voltage monitor accomplishes this by controlling, via the CPLD, the BATLOW# signal of the ICH8M. When BATLOW# is asserted the ICH8M will defer the platform to leave the power states S3 – Suspend to RAM, S4 – Suspend to disk or S5 – Soft off. Once BATLOW# goes inactive the ICH8M will let the platform transition to S0.

» Onboard debug LED will be disabled

The onboard debug LED will be turned off to reduce the power consumption, especially when not in S0.

Table 17: Single Supply Mode

State	PWRBTN#	PWR_OK	V5_StdBy	VCC (4.75-18V)	Note
S3	x	x	5V	VCC	3
S3 -> S0	PWRBTN Event	x	x	VCC	
S5	x	x	5V	VCC	3
S5 -> S0	PWRBTN Event	x	x	VCC	

NOTES: 1) Columns marked "x" are not relevant for the specified power state.
2) All ground pins have to be tied to the ground plane of the carrier board.
3) In suspend either V5_StdBy **AND/OR** VCC can be powered.

4.1.17 Miscellaneous Circuits

Speaker

The implementation of this subsystem complies with the COM Express® Specification. For additional implementation information, refer to the PICMG COM Express® Design Guide.

Battery

The implementation of this subsystem complies with the COM Express® specification. For additional implementation information, refer to the ***PICMG COM Express® Design Guide*** on the PICMG website.

In compliance with the EN60950 standard, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

NOTE: A diode and resistor protection is already present on the module.

I^2C Bus

The I^2C bus is implemented using bit banging. The speed for this bus is always 100kHz. No multi-master support is available.

See the Chapter 8, "BIOS Operation" for supported I^2C features.

SMBus

System Management Bus (SMB) signals are connected to the SMBus controller, which is located on the Intel® ICH8M. The SMBus is a 2-wire bi-directional bus (clock and serial data) used for system management tasks such as reading parameters from a memory card or reading temperatures and voltages of system components.

The SMBus uses the same signaling scheme as the I^2C bus.

PCI Bus

The processor provides a standard PCI 3.0 32-bit/33 MHz interface. The implementation of this subsystem complies with the COM Express® Specification. For additional implementation information, refer to the PICMG COM Express® Design Guide.

WARNING: The following signal is not 5V tolerant as required by the COM Express 2.0 specification:
- Pin D48 - PCI_CLKRUN#

IDE Port

The IDE host adapter on the Intel® ICH8M supports PATA/UDMA-33/66/100 operation. The implementation of this subsystem complies with the COM Express® Specification. For additional implementation information, refer to the ***PICMG COM Express® Design Guide*** on the PICMG website.

WARNING: The following signal is not 5V tolerant as required by the COM Express 2.0 specification:
- Pin D77 - IDE_CBLID

5 Special Features

5.1 Hyper-Threading

Hyper-threading (officially termed Hyper-Threading Technology or HTT) is an Intel-proprietary technology used to improve parallelization of computations performed on PCs. Hyper-threading works by duplicating certain sections of the processor—those that store the architectural state -- but not duplicating the main execution resources. A hyper-threading equipped processor can appear to be two "logical" processors to the host operating system, thus allowing the operating system to schedule two threads or processes simultaneously. Hyper Threading Technology support always depends on the operating system.

5.2 Enhanced SpeedStep™ Technology

The Intel® N450 Atom processor supports the Intel® Enhanced SpeedStep™ technology, which automatically switches the processor between maximum performance mode and battery-optimized mode, depending on the needs of the application being run. Modules with either the D510 or D410 CPU do not support Enhanced Intel SpeedStep Technology. SpeedStep technology lets you optimize the system performance to match application requirements. When powered by a battery or running in idle mode, the processor drops to lower frequencies (by changing the CPU ratios) and voltage to conserving battery life while maintaining a high level of performance. The frequency is set back to high automatically, allowing you to customize performance.

NOTE: To use Enhanced SpeedStep™ technology, you need an operating system that supports it.

Disabling SpeedStep in the BIOS enables manual control of CPU performance. You can set the CPU performance state in the BIOS setup or use third-party software to control CPU performance states.

5.3 Onboard Hardware Monitor

The microETXexpress®-PV COM has an onboard hardware monitor. The following table lists the different sensors implemented.

Table 18: Sensors

Sensor name	Measurements	Notes
CPU Temp 1	CPU 1 junction temperature.	-
CPU Temp 2	CPU 2 junction temperature.	Only available on the modules with D510 CPU.

System Temp	Internal HWM IC temperature.	Provides the module's PCB temperature
FAN 0	Onboard fan connector tach input.	-
Voltage 0	CPU core voltage	-
Voltage 1	Module main (12V) input voltage	A voltage divider is present on this pin in order to be able to read the full range of input voltage. The reading must be multiplied by 2 to have the real value when using third party software.
Voltage 2	Module 5V standby input voltage	-
Voltage 3	RTC battery voltage	To read this sensor properly when using third party software, the HWM GPIO 1 must be enabled. This feature prevents unnecessary drainage of the RTC battery.

5.4 Watchdog

This feature is implemented through the LPC on the CPLD and offers a dual-stage watchdog. It first generates an NMI and, after 1mS, a reset is generated. The application software should strobe the WDTimer to prevent a timeout. The WDTrigger resets and restarts the system after a timeout to provide a way to recover from program crashes or lockups.

The Watchdog can be triggered through

» K-Station

» Direct programming (i.e., writing data into one register of the CPLD)

For information about programming this feature, see the JIDA32/K-Station driver packet in the Kontron Customer section or contact your local sales support representative to get an application note about low level programming.

5.5 JIDA Non-Volatile and CMOS Settings

The microETXexpress® -PV module allows saving the CMOS settings externally. If the RTC battery fails to keep CMOS voltage at a certain level, the external EEPROM restores the previous settings. If the CMOS is lost, all previous settings are restored and an error message is displayed on the POST screen: "CMOS Date/Time Not Set".

From there, users have two choices: "Press F1 to Run SETUP" or "Press F2 to load default values and continue". If the choice is to keep all previous settings, then Press "F1" and enter the new date and new hour. Press F10 to save and exit. Your previous settings are set correctly and the time and

date are set accordingly. Pressing F2 sets the date to the BIOS build date and the hour is set to 00:00:00. The default values are reloaded and the system will boot on the default bootable device.

5.6 General Purpose Input and Output (GPIO)

The microETXexpress®-PV COM provides eight GPIOs (always enabled)that can be accessed through the module connector described in the pin-out lists, in Section 4.1. The GPIO viewer can be enabled in the BIOS setup.

NOTE: GPIO cannot drive applications faster than 2 msec. Data transfer rates up to 1 kHz maximum are recommended.

Table 19: GPIO COM Express Pin-Outs

Bit of GPIO Port0	Function	COM Express Pin
0	GPI0	A54
1	GPI1	A63
2	GPI2	A67
3	GPI3	A85
4	GPO0	A93
5	GPO1	B54
6	GPO2	B57
7	GPO3	B63

5.7 I^2C

The microETXexpress®-PV COM integrates uses an I^2C bus provided via the Intel® ICH8M chipset. For the External I^2C Speed it will always be 100kHz. No multi-master support is available.

5.8 ACPI Suspend Modes and Resume Events

The microETXexpress®-PV COM supports the following suspend modes:

- S0 (Full on)
- S3 (Suspend to RAM)
- S4 (Suspend to Disk)
- S5 /WOL(power off, WOL enabled)
- S5 (power off, WOL disabled)

Events that Resume the System from S3

- USB keyboard (1)
- USB mouse (1)
- Power button
- WakeOnLan (2)

Events that Resume the System from S4/S5

- Power button
- WakeOnLan

NOTES: 1) The OS must support wake-up via USB devices and the baseboard must power the USB port with Standby-Voltage
2) WakeOnLan must be enabled in the driver options

6 Design Considerations

6.1 Thermal Management

A heat spreader plate assembly is available from Kontron Embedded Modules for the microETXexpress®-PV COM. The heat spreader plate on top of this assembly is NOT a heat sink. It works as a COM Express®-standard thermal interface to be used with a heat sink or other cooling device.

External cooling must be provided to maintain the heat spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat spreader plate temperature of 60° C or less.

The aluminum slugs and thermal pads on the underside of the heat spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the microETXexpress®-PV. About 80 percent of the power dissipated within the module is conducted to the heat spreader plate and can be removed by the cooling solution.

Kontron also has defined a passive heat sink that can be used in place of the heat spreader plate to provide additional cooling. You can use many thermal-management solutions with the heat spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COM Express® application and environmental conditions. Drawings for both the heat spreader plate and the passive heat sink are available on request. Also, see the ***PICMG COM Express® Design Guide*** on the PICMG website for further information about thermal management.

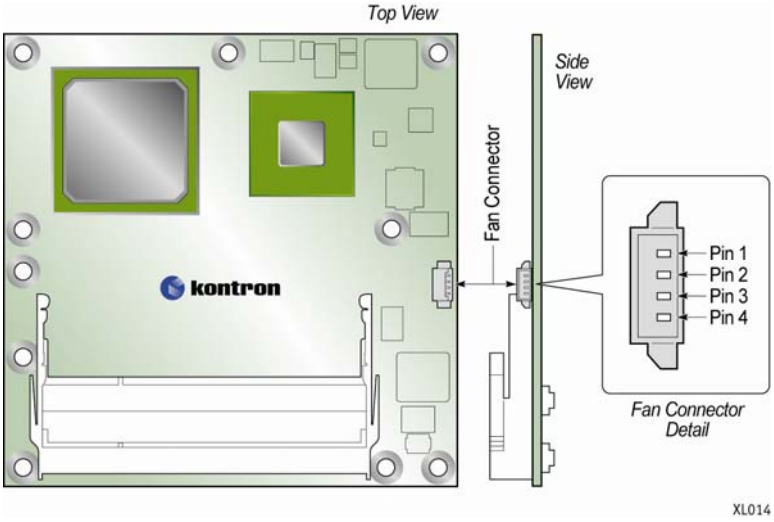
6.2 Heat Spreader Dimensions

Documentation for the microETXexpress®-PV COM heat spreader and cooling solutions is provided at http://emdcustomersection.kontron.com.

6.3 Onboard Fan Connector

This section describes how to connect an optional fan to the connector located directly on the microETXexpress®-PV COM. With certain BIOS-settings it is possible to control the fan depending on the active trip point temperature. The fan switches on/off depending on the adjusted Active Trip Point temperature. This feature requires an ACPI-compliant OS to function properly. The fan PWM control is done on the GND pin rather than the positive side. Please do not use pin 3 as a ground connection. See schematic below for more details.

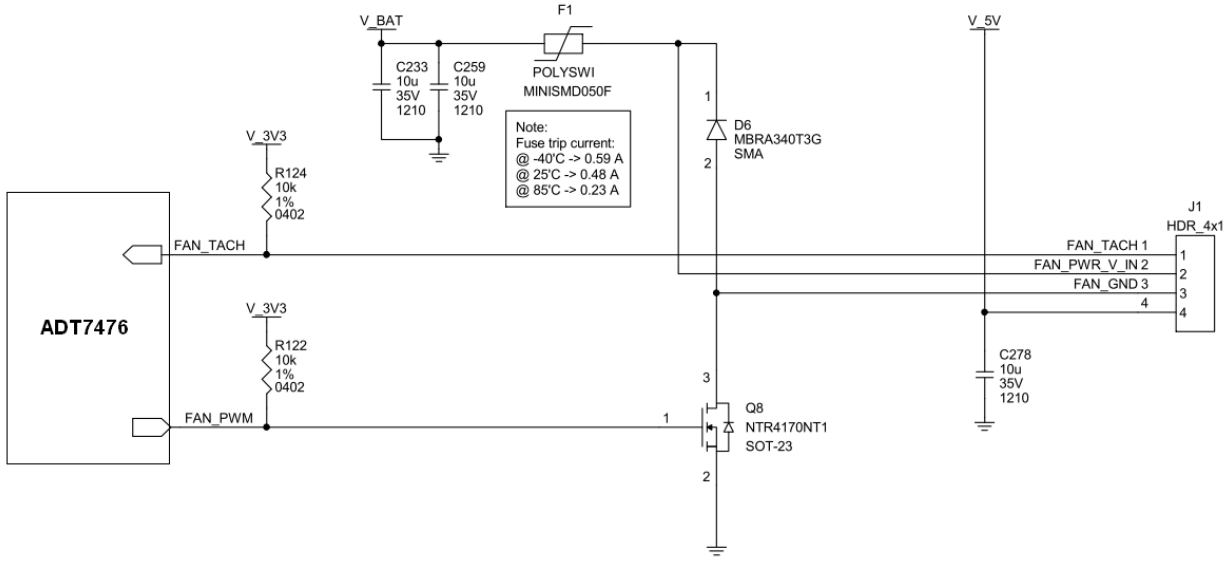
Figure 8: Fan Connector (J1) Location and Pin-Out



The onboard fan connector (J1) is on the right top side of the PCB.

Table 20: Fan Connector (J1) Pin-Out

Pin	Description
1	Fan Tachometer
2	Power (12V)
3	Fan GND (PWM controlled)
4	Power (5V)



Connector J1 specifications and Kontron part numbers for the components are:

» Part number: (Molex) 53261-0471

- Mates with: (Molex) 51021-0400
- Crimp terminals: (Molex) 50079-80000 (26-28 AWG)

6.3.1Fan Connector Electrical Characteristics

The fan connector has two supply pins. One of the supply pins outputs a regulated +5V with a maximum current of 350mA. The second supply pin is connected directly from the VCC_12V supply from the COM Express connector .The maximum current supported on that output is 125mA @ 60°C ambient because it is current limited by a resettable fuse. The voltage is not limited to +12V on this pin.

WARNING: Be aware of the wide range input voltage and acceptable fan voltage when connecting a fan to ht VCC_12V (Pin 2) output.

7 System Resources

7.1 Interrupt Request (IRQ) Lines

Table 21: 8259 PIC Mode

IRQ #	Used For	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Cascade	No	
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	External SIO	Yes (No)	Note (1)
7	External SIO - LPT1	Yes (No)	Note (1)
8	RTC	No	
9	ACPI	No	Note (2)
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	
14	Primary IDE	No	
15	Secondary IDE	No	

NOTES: 1) If the "Used For" device is disabled in setup, the interrupt is available for other devices.
2) Not available if ACPI is used

Table 22: APIC Mode

IRQ #	Used For	Available	Comment
0	Timer0	No	-
1	Keyboard	No	-
2	Cascade	No	-
3	External SIO - COM2	Yes (No)	Note (1)
4	External SIO - COM1	Yes (No)	Note (1)
5	PCI	for PCI	Dynamic (BIOS default)
6	External SIO	Yes (No)	Note (1)
7	External SIO - LPT1	Yes (No)	Note (1)
8	RTC	No	-
9	ACPI	No	Note (2)
10	PCI	for PCI	Dynamic (BIOS default)
11	PCI	for PCI	Dynamic (BIOS default)
12	PS/2 Mouse	Yes (No)	Note (1)
13	FPU	No	-
14	Primary IDE	No	Note (1)
15	PCI	for PCI	Dynamic (BIOS default)
16	PIRQ [A]	No	PCI IRQ line 1 + PCIe- Switch + + SATA Bridge + USB client (if enabled) (3)
17	PIRQ [B]	No	PCI IRQ line 2 +
18	PIRQ [C]	No	PCI IRQ line 3 + USB UHCI 2832
19	PIRQ [D]	No	PCI IRQ line 4 + PCIe- Switch + USB UHCI 2831
20	PIRQ [E]	No	-
21	PIRQ [F]	No	HD Audio
22	PIRQ [G]	No	-
23	PIRQ [H]	No	USB EHCI 2836, USB UHCI 2830

NOTES: 1) If the "Used For" device is disabled in setup, the interrupt is available for other devices.
2) Not available if ACPI is used
3) ACPI OS decides on the particular IRQ usage

7.2 Memory Area

The first 640 KBytes of DRAM are used as main memory. With DOS, you can address 1 MByte of memory directly. Memory area above 1 MByte (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. See the operating system documentation or special textbooks for information about HIMEM.SYS and EMM386.EXE.

Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Used for	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic controller
C0000h – CFFFFh	VGA BIOS	No	Used by onboard VGA ROM
D0000h – DFFFFh		Yes	Free for shadow RAM in standard configurations.
E0000h – FFFFFh	System BIOS	No	Fixed

7.3 I/O Address Map

The I/O-port addresses of the microETXexpress®-PV COM are functionally identical to those of a standard PC/AT system. All addresses not mentioned in Table 1 should be available. We recommend that you do not use I/O addresses below 0100h for additional hardware for compatibility reasons, even if available.

Table 23: I/O Address Assignments

I/O Address	Used for	Available	Comment
0000 – 000F	Direct memory access controller	No	Fixed
0010 – 001F	System Resources	No	Fixed
0020 – 0021	Interrupt Controller 1	No	Fixed
0022 – 003F	System Resources	No	Fixed
002E – 002F	WB83627	No	Fixed if WB83627HG is in system
0040 – 0043	Timer, Counter	No	Fixed
0044-005F	System Resources	No	Fixed
0060-0060	System Resources	No	Fixed
0061 – 0061	System Speaker	No	Fixed
0062 – 006F	System Resources	No	Fixed
0070 – 007F	RTC and CMOS Registers	No	Fixed
0080	BIOS Postcode	No	Fixed
0081 – 008F	DMA Page Register	No	Fixed

I/O Address	Used for	Available	Comment
0090 – 009F	System Resources	No	Fixed
00A0 – 00BF	Interrupt Controller 2	No	Fixed
00C0 – 00DF	DMA Controller 2	No	Fixed
00E0 – 00EF	System Resources	No	Fixed
00F0 – 00FF	Math Coprocessor	No	Fixed
0170 – 0177 0376	Fixed Disk	No	Available if IDE port 1 is disabled
01F0 – 01F7 03F6	Fixed Disk	No	Available if IDE port 1 is disabled
0290–0295	ADT7476 HWM	No	SMBus driven
03B0 – 03DF	VGA	No	Fixed
03F8 – 03FF	Serial port 1	No	Available if WB83627HG is disabled.
0400 – 041F	SMBus	No	Fixed
04D0 – 04D1	PIC Extension	No	Fixed
0500 – 053F	GPIO	No	Fixed
0A20 – 0A2F	SIO Hardware Monitor	No	Fixed if SIO is in system
0A05 – 0A06	ADT7476 Hardware Monitor	No	The HW monitor uses the SMBus to access registers (address is 0x5C)
0A80 – 0A81	CPLD	No	CPLD use 0A00h to 0A1Fh
0D00 – FFFF	PCI Bus	No	Fixed
C000 – C007	VGA	No	Fixed
C400 – C41F	Standard PCI to USB	No	Dynamic
C480 – C49F	USB Host Controller 2832	No	Dynamic
C800 – C81F	USB Host Controller 2831	No	Dynamic
C880 – C89F	USB Host Controller 2830	No	Dynamic
D000 – DFFF	PCIe Root Port 1	No	Dynamic (BIOS default value)
E000 – EFFF	PCIe Root Port 2	No	Dynamic (BIOS default value)
0CF8 – 0CFF	PCI Configuration	No	Fixed
FF90 – FFAF	SATA Controller	No	Dynamic (BIOS default address)

7.4 Peripheral Component Interconnect (PCI) Devices

All devices follow the Peripheral Component Interconnect 2.3 (PCI 2.3) and the PCI Express Base 1.0a specifications. The BIOS and OS control memory and I/O resources. Please see the PCI 2.3 specification for details.

Table 24: PCI Device IRQs

PCI Device	PCI IRQ	Interface	Comment
Host Bridge / Memory Controller	None		Integrated in processor
Graphics / Video Controller	INTA		Integrated in processor
UHCI controller	INTA		Integrated in chipset
HD Audio Controller	INTA		Integrated in chipset
PCI Express Port 0	INTA		Integrated in chipset
PCI Express Port 2	INTB		Integrated in chipset
PCI Express Port 3	INTC		Integrated in chipset
PCI Express Port 4	INTD		Integrated in chipset
PCI Express Port 5	INTA		Integrated in chipset
UHCI USB Controller 1	B		Integrated in chipset
UHCI USB Controller 2	C		Integrated in chipset
UHCI USB Controller 3	D		Integrated in chipset
EHCI USB Controller 0	INTA		UHCI controller 0 INTA
ISA Bridge / LPC Controller	None		Integrated in chipset
IDE Controller	None		Integrated in chipset
Network Controller	INTA	PCI Express	Integrated in chipset.
SATA	INTA	PCI Express	Integrated in chipset.

Table 25: External I²C Bus #1

I²C Address	Used For	Available	Comment	JIDA Bus Nr.
A0h	JIDA-EEPROM	No	EEPROM for CMOS Data	1
A2h	JIDA-EEPROM	No	EEPROM for CMOS Data	1

Table 26: JILI I²C Bus

I²C Address	Used For	Available	Comment	JIDA Bus Nr.

A0h	JILI-EEPROM	No	EEPROM for JILI Data	4

7.5 System Management Bus (SMBus)

Table 27: SMBus Address Assignments

Address	Device	Notes	JIDA Bus Nr.
12h	SMART_CHARGER	Not to be used with any SMBus device except a charger	1
14h	SMART_SELECTOR	Not to be used with any SMBus device except a selector	1
16h	SMART_BATTERY	Not to be used with any SMBus device except a battery	1
5Ch	ON Semiconductor ADT7476 HWM	Do not use under any circumstances	1
A0h	SPD EEPROM on DDR2	Do not use under any circumstances	1
A2h	SPD EEPROM on DDR2	Do not use under any circumstances	1
D2h	Clock Gen CK610/ICS9DB403	Do not use under any circumstances	1

7.6 K-Station / JIDA32 Resources

Table 28: I^2C

Bus	Function
I2C 0	Internal / JIDA I2C #1
I2C 1	SMBus
I2C 2	Internal / JIDA I2C #2 (for slow devices)
I2C 3	JILI I2C

Table 29: Storage

Device	Function
EEPROM 0	JIDA EEPROM Area 1 with 32 Bytes (free to use)

Table 30: GPIO

Port	Function
IO-Port 0	GPIO Port, Bit 0-3: Input, Bit 4-7:

	Output

Table 31: Hardware Monitor

Sensor	Function
Temp 0	CPU Core 1 Temperature. TEMP 0 Internal temperature TEMP2 CPU Core 2 Temperature TEMP1
Temp 1	Module temperature (internal IC temperature of onboard ADT7476 HWM)
FAN 0	Module CPU fan sensor (measured with ADT7476 HWM)
Voltage 0	ON Semiconductor ADT7476 Voltage Sensor 0: VCC RTC
Voltage 1	ON Semiconductor ADT7476 Voltage Sensor 1: VCore
Voltage 2	ON Semiconductor ADT7476 Voltage Sensor 2: Vcc +5Vin (Voltage 3) +VBat (Voltage 4)

8 BIOS Operation

8.1 Determining the BIOS Version

The microETXexpress®-PV COM has AMIBIOS®8 installed on the onboard 16Mbit SPI. To determine the AMI® BIOS version, press the Pause key on your keyboard immediately, as soon as you see the following text display in the upper left corner of your screen

- AMIBIOS © 1985-2009, American Megatrends, Inc.
- BIOS Date: 06/16/08 10:52:49 Ver: 08.00.16
- Kontron® BIOS Version < UPV1R016 > (This revision number "R016" will change as the BIOS is improved)
- © Copyright 2002-201008 Kontron

8.2 Setup Guide

The AMIBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

NOTE: Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>.

8.2.1Start AMIBIOS®8 Setup Utility

To start the AMIBIOS® setup utility, press <DEL> when the following string appears during boot-up:

Press <DEL> to enter Setup

The Info menu then appears.

The Setup screen has several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side bottom	Lists setup navigation keys.
Item Specific Help Window	Right side top	Help for selected item.
Menu Window	Left center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the ← arrow key or the → arrow key to make a selection.

Legend Bar

Use the keys listed on the bottom of the legend bar to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and - keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← arrow key or the → arrow key to move the cursor to the submenu you want and then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor through each field.

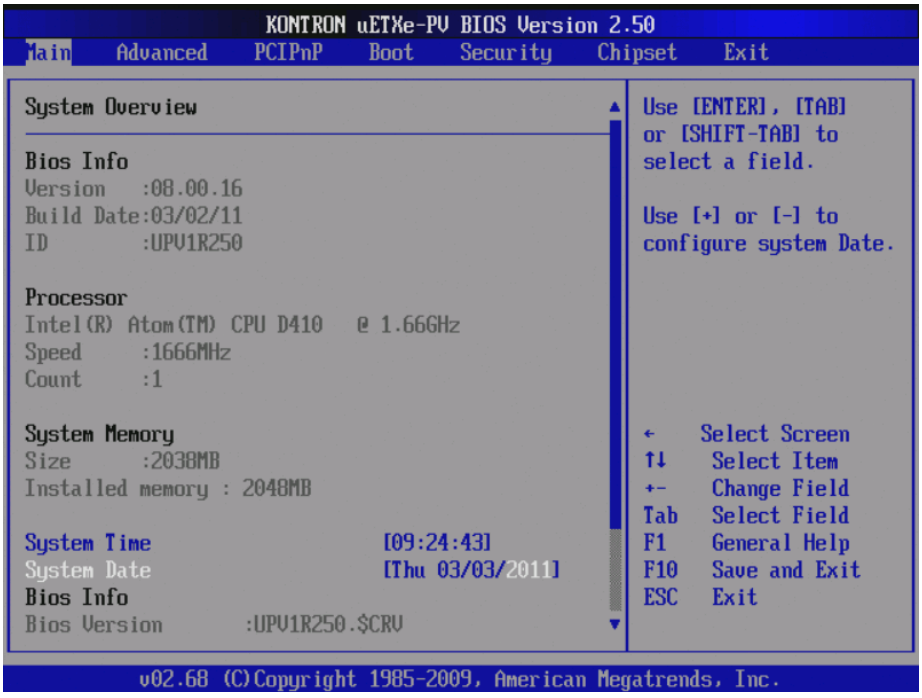
General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

8.3 BIOS Setup

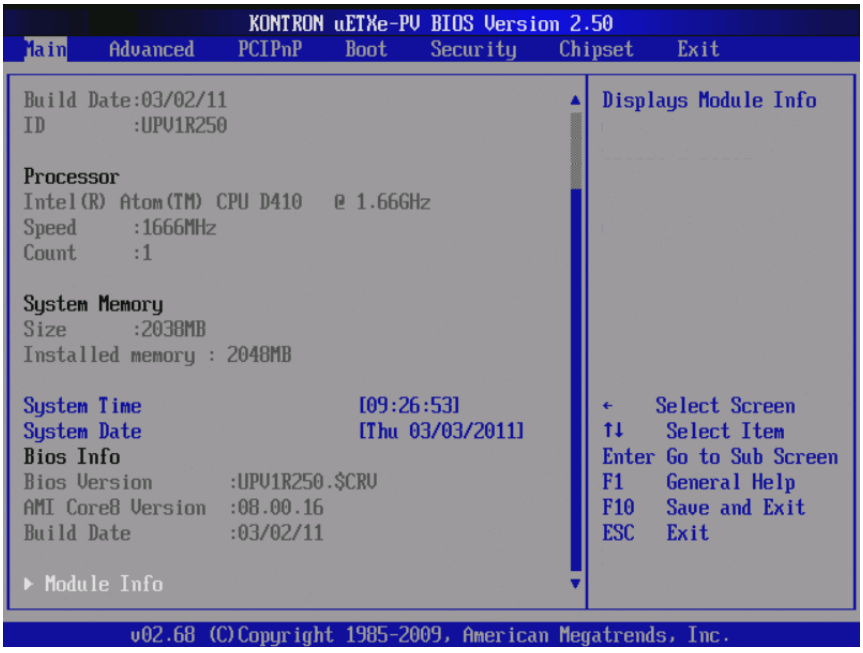
NOTE:	Default settings are in bold

8.3.1Main Menu



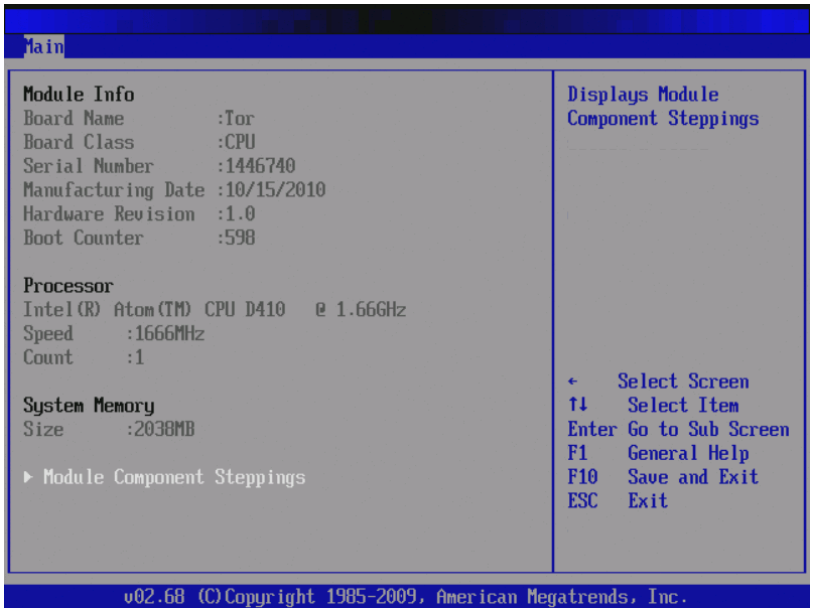
Feature	Option	Description
System Time	[hh:mm:ss]	<Tab>, <Shift-Tab>, or <Enter> selects field
System Date	[mm-dd-yyyy]	<Tab>, <Shift-Tab>, or <Enter> selects field

System Overview



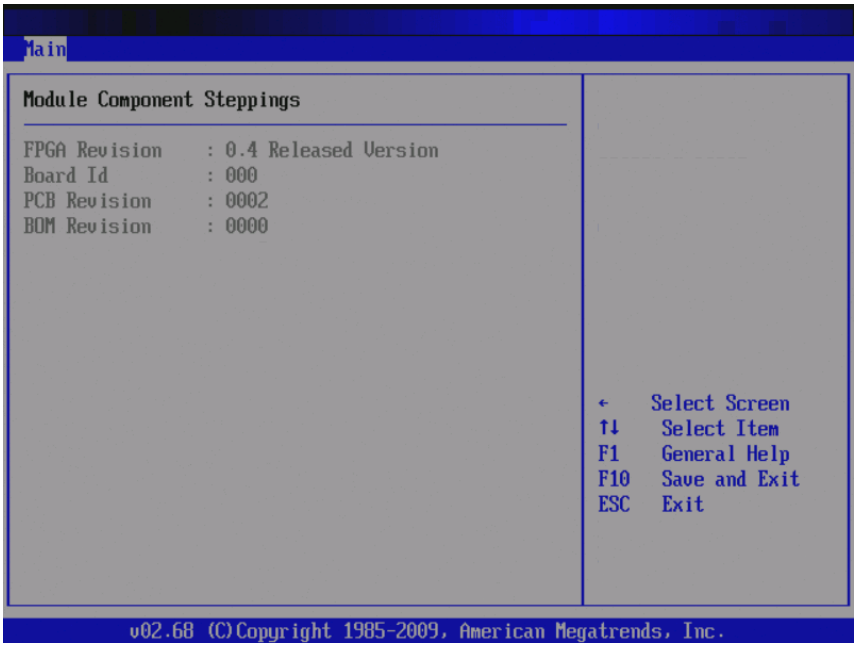
Feature	Option	Description
Module Info	N/A	Select sub-menu.

8.3.2Module Info



Feature	Option	Description
Module Info	N/A	Select sub-menu
Board Name	N/A	Displays the board name programmed
Board Class	N/A	Displays the class of the board
Serial Number	N/A	Displays serial number of the board
Manufacturing Date	N/A	Date of production of the board
Hardware Revision	N/A	Displays revision programmed of the board
Boot Counter	N/A	Displays complete boot count of the board
Processor type	N/A	Displays information about the CPU (Brand name, Speed and count
Size	N/A	Displays amount of memory available to the OS
Module Component Steppings	N/A	Select sub-menu

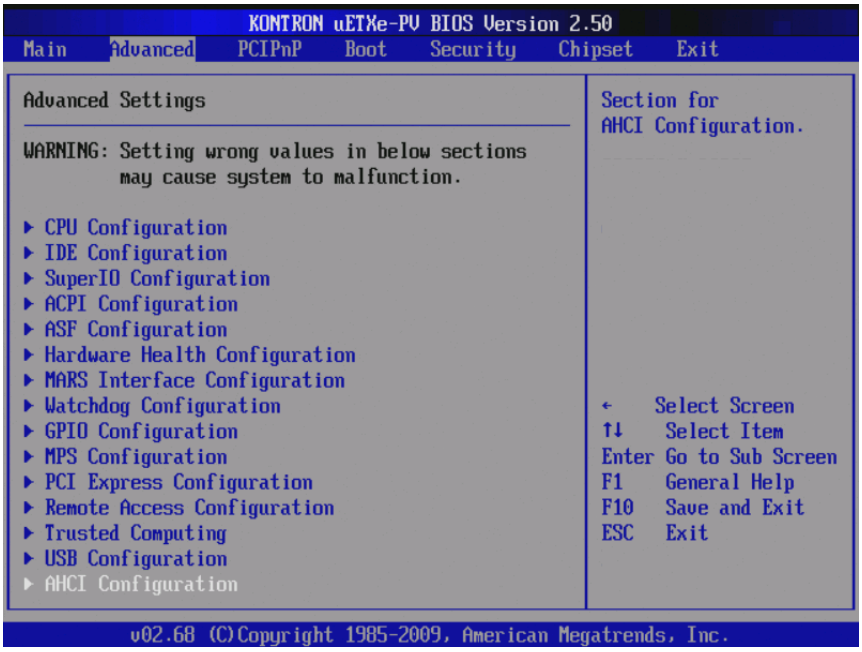
Module Component Stepping



Feature	Option	Description
FPGA Revision	N/A	Displays the FPGA version programmed on the board
Board Id	N/A	Displays id of the board (HW strap)
PCB	N/A	Displays PCB version of the board

Revision		(HW strap)
BOM Revision	N/A	Displays BOM version of the board (HW strap)

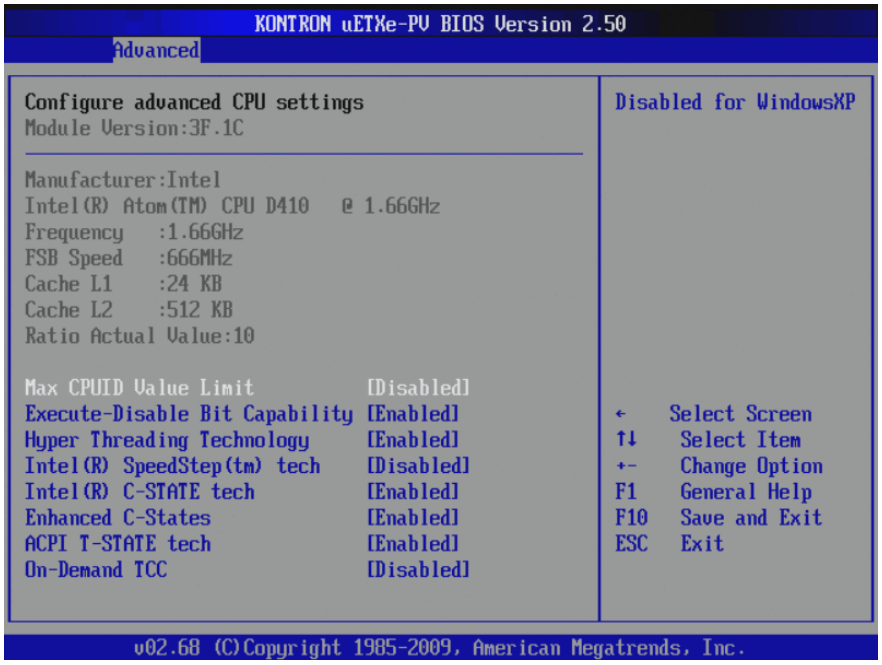
8.3.3Advanced Settings Menu



Feature	Option	Description
CPU Configuration	**N/A**	Select sub-menu
IDE Configuration	N/A	Select sub-menu
SuperIO Configuration	N/A	Select sub-menu (only if SIO is present or enabled on carrier board).
ACPI Configuration	N/A	Select sub-menu
ASF Configuration	N/A	Select sub-menu
Hardware Health Configuration	N/A	Select sub-menu
MARS Interface Configuration	N/A	Select sub-menu
Watchdog Configuration	N/A	Select sub-menu
GPIO Configuration	N/A	Select sub-menu
MPS Configuration	N/A	Select sub-menu
PCI Express Configuration	N/A	Select sub-menu
Remote Access	N/A	Select sub-menu

Configuration		
Trusted Computing	N/A	Select sub-menu
USB Configuration	N/A	Select sub-menu
AHCI Configuration	N/A	Select sub-menu

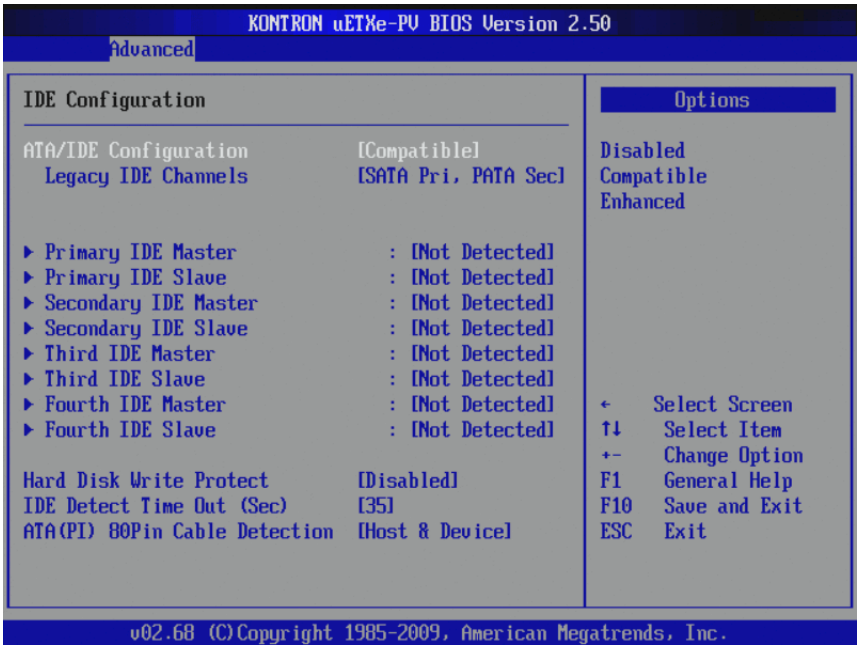
CPU Settings Configuration



Feature	Option	Description
Manufacturer	N/A	Displays information about the CPU manufacturer
Frequency	N/A	Displays CPU Speed
FSB Speed	N/A	Displays Front Side Bus speed information
Cache L1	N/A	Displays level 1 amount of cache memory
Cache L2	N/A	Displays level 2 amount of cache memory
Ratio Actual Value	N/A	Displays CPU ratio for the CPU Speed
Max CPUID Value Limit	**Disabled** Enabled	Enable this for legacy operating systems that do not support CPUID function >
Execute-Disable Bit Capability	Enabled **Disabled**	When enabled, allows the processor to prevent application code access to certain memory areas (requires OS that supports this) When disabled, there are no restrictions to application code

Feature	Option	Description
		memory area access by the processor
Hyper Threading Technology	**Enabled** Disabled	Enables or disables Intel® Hyper Threading Technology, which allows one additional logical CPU for each physical CPU
Intel® SpeedStep™tech	**Enabled** Disabled	When enabled, cpu speed can be controlled by OS (only supported on the N450 CPU)
Intel® C-State tech	**Enabled** Disabled	Intel CPU state for power saving (Dx10 CPUs support C0-C1 only; the N450 CPU supports C0-C4)
Enhanced C-States	**Enabled** Disabled	Deeper C-state for CPU (only enabled when option "Intel® C-State tech" is enabled)
ACPI T State	Enabled Disabled	Enables or disables the ACPI T State power management features (Not used with the microETXexpress-PV)
On-Demand TCC	Enabled Disabled	Enables throttling at all time. This is for testing purpose only. WARNING: Never leave this option enabled. The board lifetime will be seriously impacted.
Duty Cycle in %	12.5 25 37.5 **50** 62.5 75 87.5	Percentage of the throttling forced for the CPU.

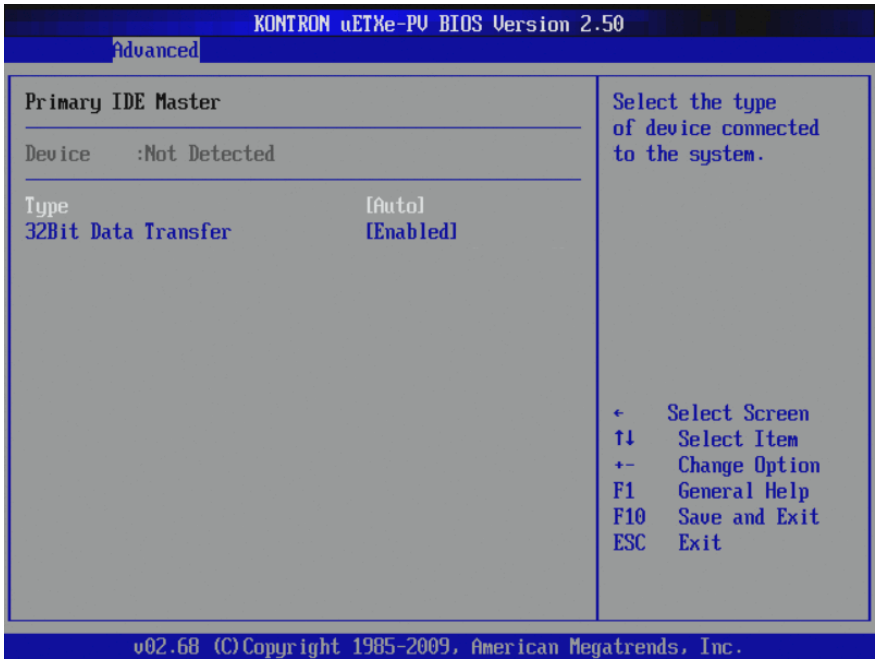
IDE Configuration



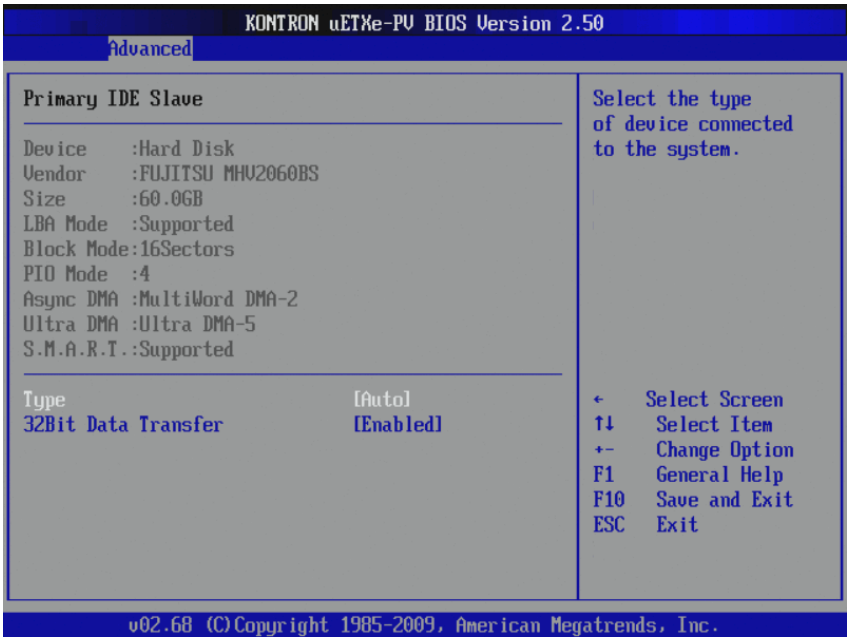
Feature	Option	Description
ATA/IDE Configuration	Disabled **Compatible** Enhanced	With AHCI, advanced SATA features such as Native Command Queuing and hot plug are supported **Compatible** enables legacy disk usage (Windows XP with no AHCI drivers)
Legacy IDE Channels	SATA only **SATA primary/PATA secondary** PATA only	Configures IDE channel use
Configure SATA as	**IDE** AHCI	Menu appears only if ATA/IDE configuration is set to "Enhanced".
▸ Primary IDE Master	Submenu **Not Detected**	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto-detection of IDE devices
▸ Primary IDE Slave	Submenu **Not Detected**	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto-detection of IDE devices
▸ Secondary IDE Master	Submenu **Not Detected**	While entering setup, BIOS auto detects the presence of IDE devices. This displays

Feature	Option	Description
		the status of auto-detection of IDE devices
▸ Secondary IDE Slave	Submenu **Not Detected**	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto-detection of IDE devices
▸ Third IDE Master	Submenu **Not Detected**	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto-detection of IDE devices
▸ Third IDE Slave	Submenu **Not Detected**	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto-detection of IDE devices
▸ Fourth IDE Master	Submenu **Not Detected**	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto-detection of IDE devices
▸ Fourth IDE Slave	Submenu **Not Detected**	While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto-detection of IDE devices
Hard Disk Write Protect	**Disabled** Enabled	Disable/Enable device write protection. (This is effective only when the device is accessed through the BIOS)
IDE Detect Time Out (Sec)	0 5 10 15 20 25 30 **35**	Selects the maximum time- out value for detecting ATA/ATAPI device(s)
ATA(PI) 80Pin Cable Detection	**Host & Device** Host Device	Mechanism selection of the 80-pin ATA cable detection

Primary IDE Master



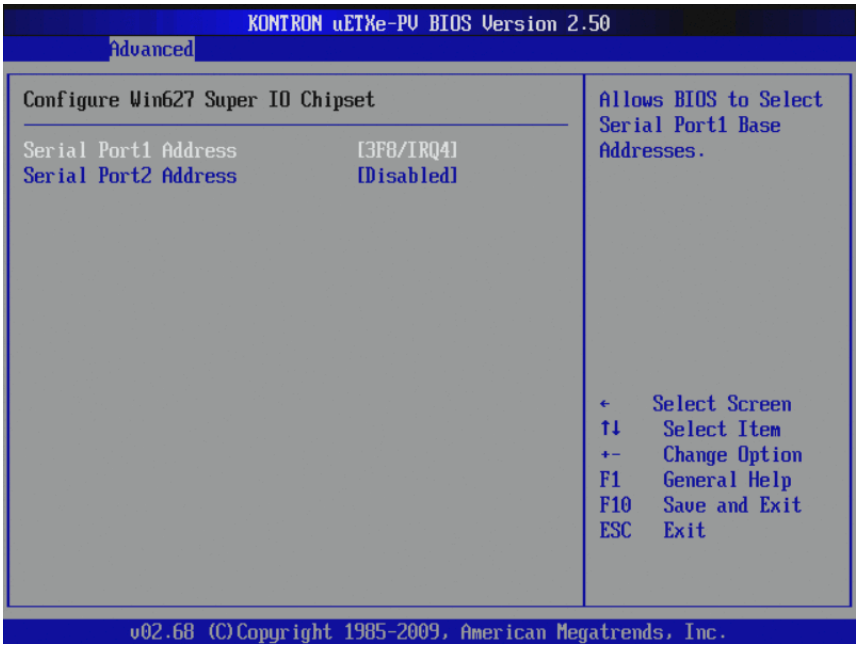
Primary IDE Slave



Feature	Option	Description
Device	Depends on disk presence	Displays the device type (hard disk).

Feature	Option	Description
Vendor	N/A	Displays the vendor string of the disk.
Size	N/A	Displays the size of the disk.
LBA Mode	N/A	Displays if LBA mode is supported by the disk.
Block Mode	N/A	Displays block mode size
PIO Mode	N/A	Displays PIO mode speed
Async DMA	N/A	Displays Async mode speed
Ultra DMA	N/A	Displays Ultra DMA mode
S.M.A.R.T.	N/A	Displays if SMART is supported
Type	Not Installed **Auto** CD/DVD ARMD	Selects the type of IDE devices connected to the system
32Bit Data Transfer	**Enabled** Disabled	Enables or disables the 32-bit Data Transfer features

Super I/O Configuration



Feature	Option	Description
Serial Port1 Address	Disabled **3F8/IRQ4** 3E8/IRQ4 2E8/IRQ3	Selects the serial port 1 base address and interrupt
Serial Port2 Address	Disabled **2F8/IRQ3**	Selects the serial port 2 base address and interrupt

Feature	Option	Description
	3E8/IRQ4 2E8/IRQ3	
Serial Port2 Mode	**SPP** IrDA ASK IR	Serial Port2 mode selection (depends on the carrier board support. Normally only SPP is present on the carrier)
IR I/O Pin Select	**SINB/SOUTB** IRRX/IRTX	Allows BIOS to select receive or transmit pin for Serial Port2 (IR Mode). This only shows if "Serial Port2 Mode" is set to "IrDA" or "ASK IR".
IR Duplex Mode	Full Duplex **Half Duplex**	Allows BIOS to select full or half duplex for Serial Port2 (IR Mode) This only shows if "Serial Port2 Mode" is set to "IrDA" or "ASK IR".

ACPI Configuration

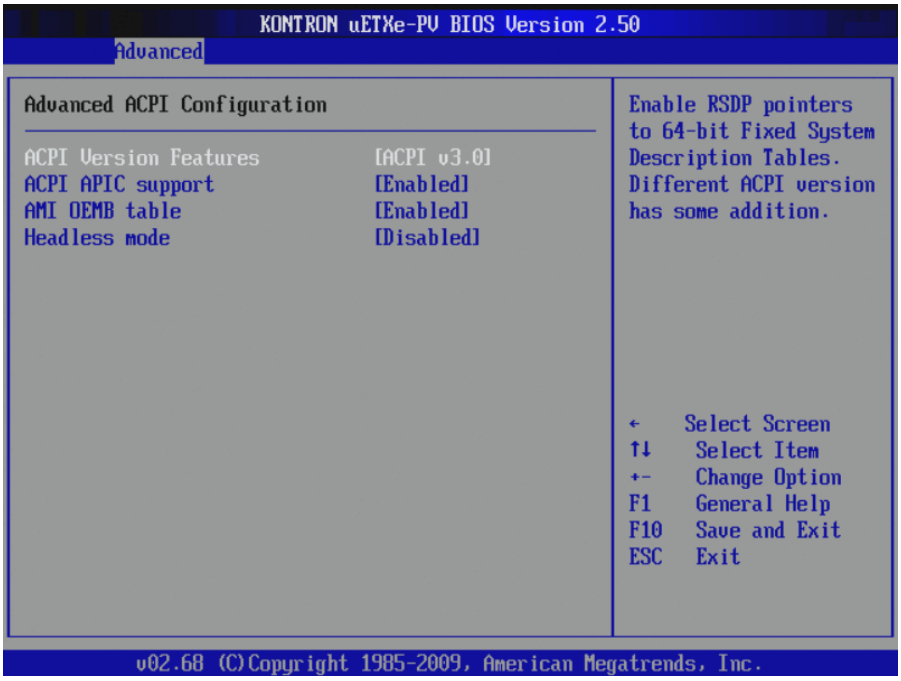
Feature	Option	Description
▸ General ACPI Configuration	Submenu	Allows configuration of the general ACPI features
▸ Advanced ACPI	Submenu	Allows configuration of the advanced ACPI features

Configuration		
▸Chipset ACPI Configuration	Submenu	Allows configuration of the ACPI features supported by the chipset

General ACPI Configuration

Feature	Option	Description
Suspend Mode	S1 (POS) S3 (STR) **Auto**	Allows for adjustment of the suspend mode settings managed under ACPI power management features
Repost Video on S3 Resume	**No** Yes	Determines whether to invoke VGA BIOS post on S3/STR resume

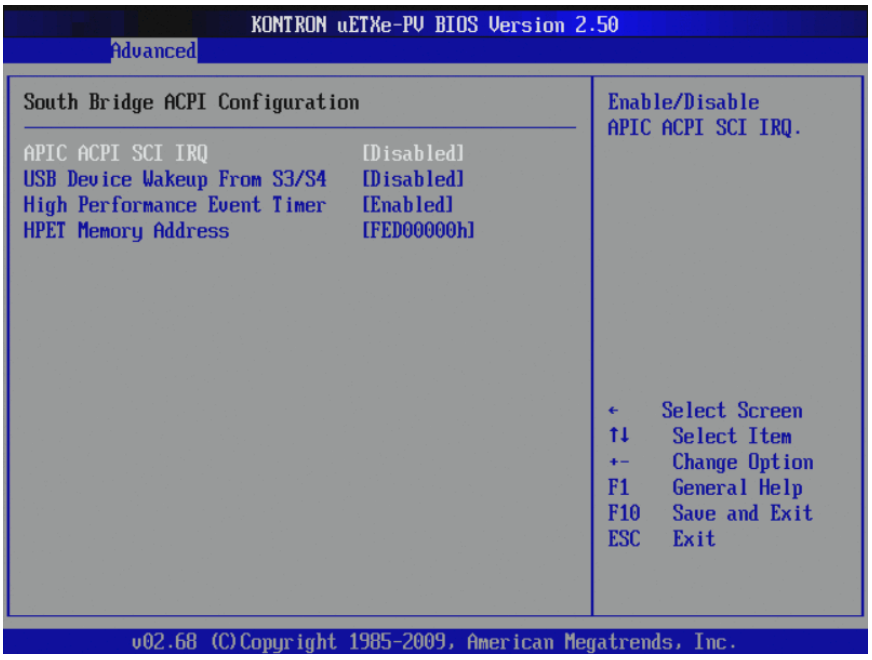
Advanced ACPI Configuration



Feature	Option	Description
ACPI Version Features	ACPI 1.0 ACPI 2.0 **ACPI 3.0**	Version 1.0 only supports RSDP pointers to 32-bit Fixed System Description Tables Version 2.0 enables RSDP pointers to 64-bit Fixed System Description Tables Version 3.0 improves processor, PCI Express, and SATA support
ACPI APIC Support	Disabled **Enabled**	Include ACPI APIC table pointer to RSDT pointer list. APIC supports more IRQs and faster interrupt handling
AMI OEMB Table	Disabled **Enabled**	Includes the AMI OEMB table pointer. The OEMB table is used to fill in POST data in AML code during ACPI OS operations. This option should only be disabled if ACPI 1.0 is used
Headless Mode	**Disabled** Enabled	Indicates support for headless operation, which means without keyboard, mouse and/or monitor. The

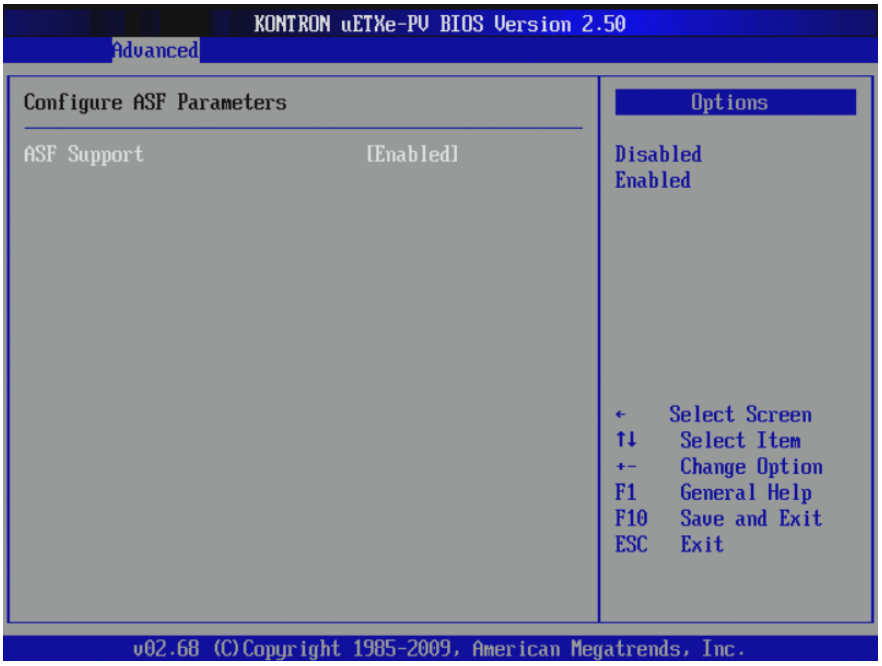
		OS must support the headless mode

Chipset ACPI Configuration



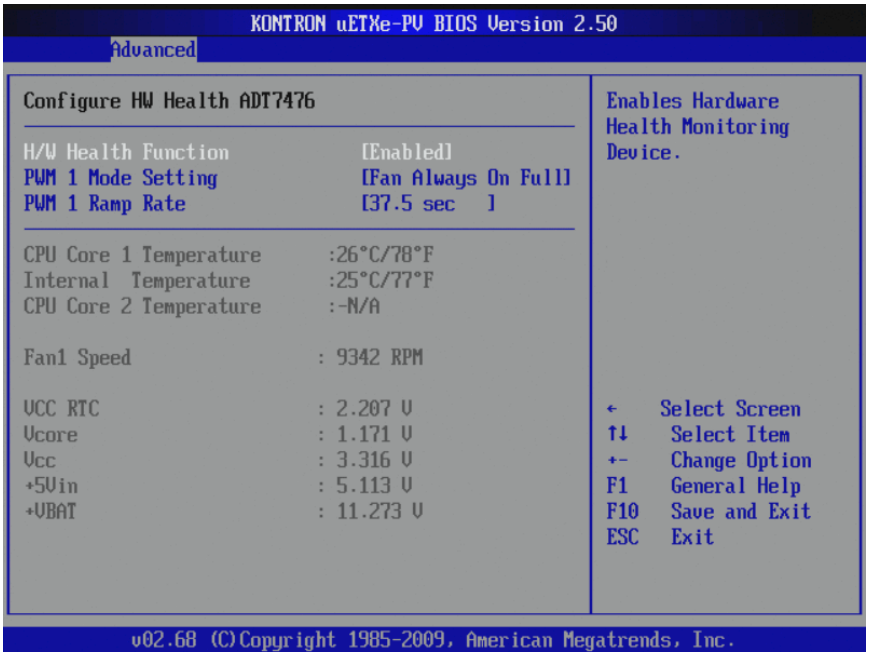
Feature	Option	Description
APIC ACPI SCI IRQ	Enabled **Disabled**	IRQ9 if APIC is not used for SCI IRQ20 is only available for SCI if APIC is enabled
USB Device Wakeup From S3/S4	Enabled **Disabled**	Enable/Disable USB Device Wakeup From S3/S4
High Performance Event Timer	**Enabled** Disabled	Enables or Disables the High Performance Event Timer feature
HPET Memory Address	**FED00000h** FED01000h FED02000h FED03000h	Allows for adjustment of the HPET memory address

ASF Configuration



Feature	Option	Description
ASF Support	**Enabled** Disabled	Enable or disable support for Alert Standard Format

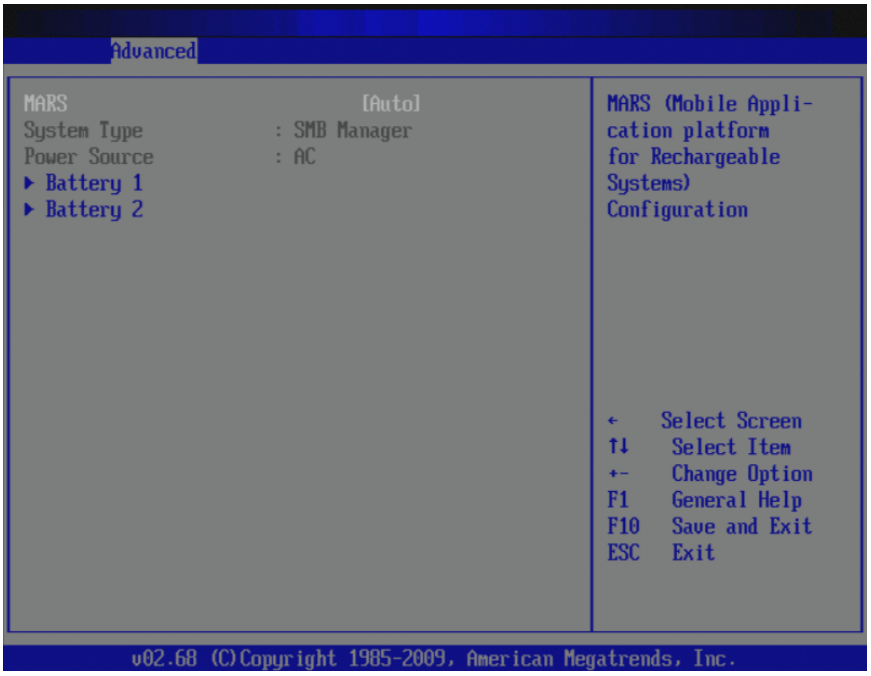
Hardware Health Configuration



Feature	Option	Description
H/W Health Function	**Enabled** Disabled	Enables Hardware Health Monitoring Device on module
PWM 1 Mode Setting	Auto Fan Mode **Fan Always On Full** Fan Disabled Mode Fan Manually Mode	Allows for adjusting fan controls
PWM 1 Ramp Rate	**37.5 secs** **18.8 secs** **12.5 secs** **7.5 secs** **4.7 secs** **3.1 secs** **1.6 secs** **0.8 secs**	Allows for adjusting the PWM Ramp Rate feature (Does not appear if "PWM1 mode Setting" is set to "Fan Disable Mode")
Min PWM 1 Duty Cycle	Range = 0 - 255 **Default = 130**	Allows for adjusting the Minimum PWM Duty Cycle Available only if "PWM1 Mode Setting" is set to "Auto Fan Mode". (See http://www.onsemi.com/pub_link/Collateral/ADT7476-D.PDF for more details)

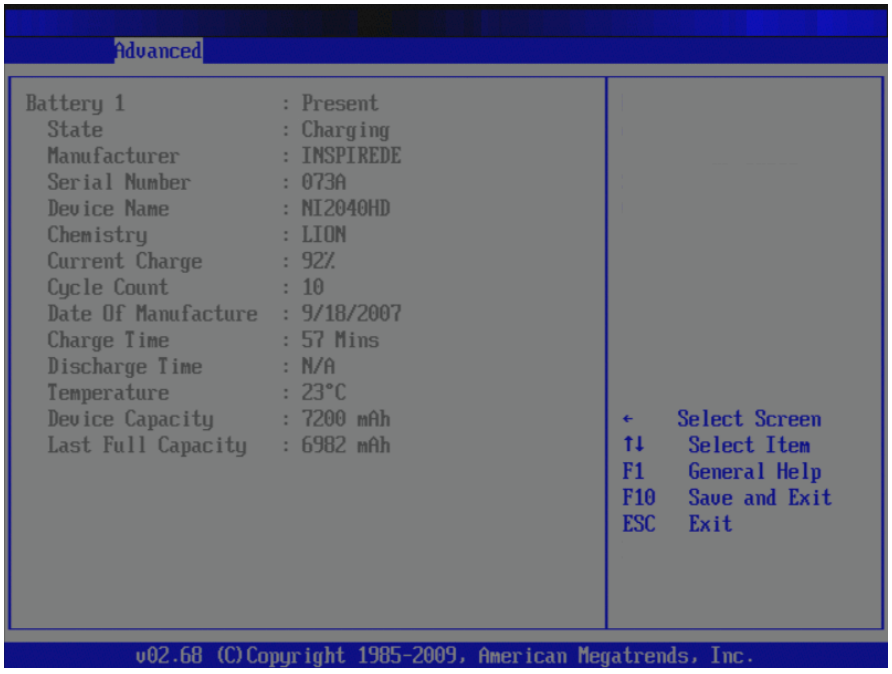
Feature	Option	Description
Absolute Temperature 1 Set	Range = 0 – 127 **Default = 075**	Allows the absolute temperature to be set
Low Temperature 1 Limit	Range = 0 – 127 **Default = 065**	Allows the low temperature limit to be set
Temperature 1 Range	2 °C 2.5 °C 3.33 °C 4 °C 5 °C 6.67 °C 8°C **10 °C** 13.33 °C 16 °C 20 °C 26.67 °C 32 °C 40 °C 53.33 °C 80 °	Allows the temperature range of the slope to be set
PWM 1 Control Duty Cycle	Range = 0 – 255 **Default = 200**	Manually set the PWM of the fan to the selected value

MARS Configuration



Feature	Option	Description
MARS	**Disabled** Auto SMB Charger SMB Manager	If carrier board support and the MARS system are present, set this option to "Auto". This option detects and enables the Mobile Application platform for Rechargeable Systems
System Type	N/A	
Power Source	N/A	
Battery 1	Submenu	
Battery 2	Submenu	

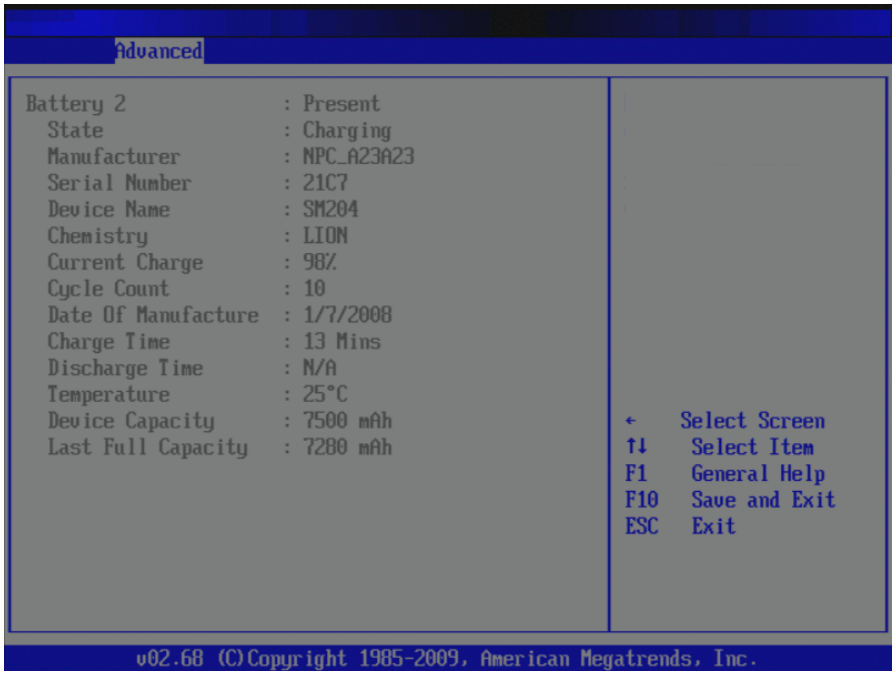
Battery 1 (if present)



Feature	Option	Description
Battery 1	N/A	Indicates battery present
State	N/A	Displays the state of the battery (charging, discharged)
Manufacturer	N/A	Displays manufacturer name
Serial Number	N/A	Displays the battery serial number
Device Name	N/A	Displays manufacturer's name for the battery
Chemistry	N/A	Displays chemistry information
Current Charge	N/A	Shows current charge capacity
Cycle Count	N/A	Shows current charge cycle of the battery
Date Of Manufacture	N/A	Displays build date of the battery
Charge time	N/A	Displays estimated time for charging to be complete
Discharge Time	N/A	Displays how much time before the battery becomes empty
Temperature	N/A	Displays the internal temperature of the battery
Device Capacity	N/A	Displays device initial capacity
Last Full	N/A	Displays last fully charged

Feature	Option	Description
Capacity		capacity

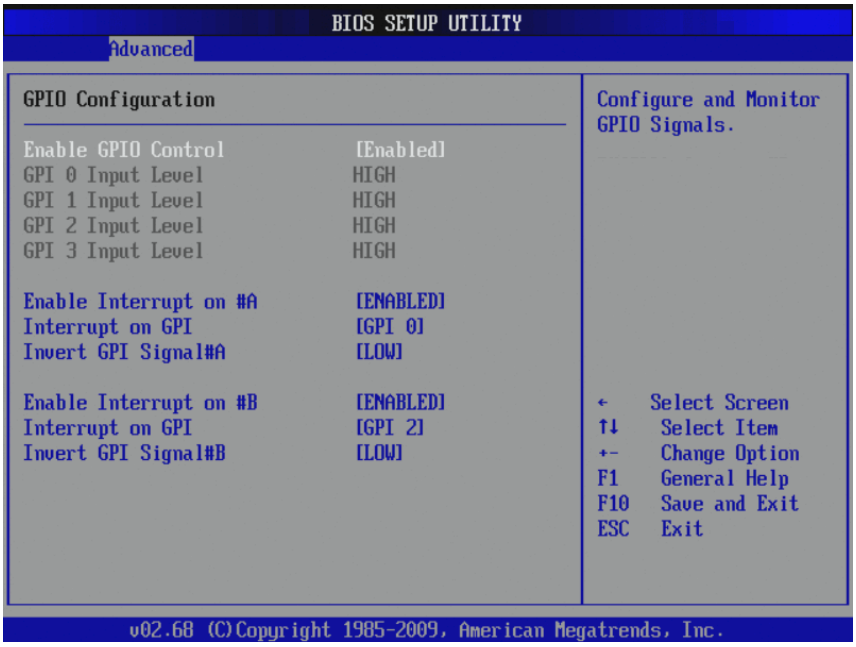
Battery 2 (if present)



Watchdog Configuration

Feature	Option	Description
FPGA Watchdog Timer	Enabled **Disabled**	When enabled, the watchdog is set with a value of 10 minutes during POST
FPGA Watchdog Timer after POST	Enabled **Disabled**	To enable this option, you must have a driver that disables or triggers the watchdog to prevent NMI generation and a reset to occur
Watchdog Duration in Sec	Range = 1 - 4194	Duration of the timeout prior to reset

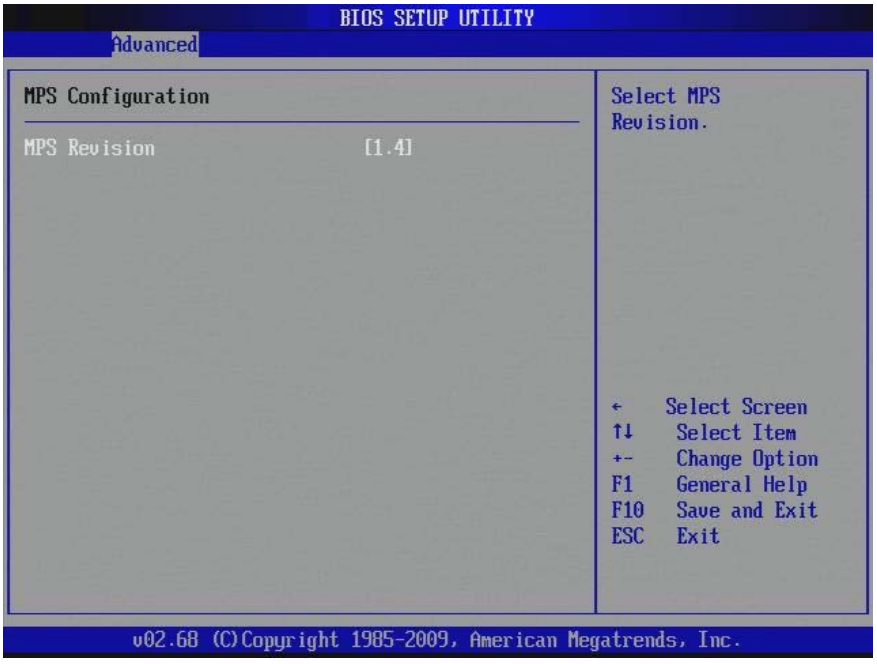
GPIO Configuration



Feature	Option	Description
Enable GPIO Control	Enabled **Disabled**	Enables or disables the GPIO monitor and settings (**NOTE:** this does not disable control of the GPIO in JIDA32)
GPI 0 Input Level	High Low	Displays the current status of GPI 0
GPI 1 Input Level	High Low	Displays the current status of GPI 1
GPI 2 Input Level	High Low	Displays the current status of GPI 2
GPI 3 Input Level	High Low	Displays the current status of GPI 3
Enable Interrupt on #A	Enabled **Disabled**	Enables or disables the interrupt on channel A
Interrupt on GPI	**GPI 0** GPI 1 GPI 2 GPI 3	Selects the GPI that will generate interrupt PIRQF or IRQ21 in APIC mode
Invert GPI Signal #A	**LOW** High	Allows selection of GPI state that will generate an interrupt.
Enable Interrupt on #B	Enabled **Disabled**	Enables or disables the interrupt on channel B
Interrupt on GPI	**GPI 0** GPI 1 GPI 2	Selects the GPI that will generate interrupt PIRQF or IRQ21 in APIC mode.

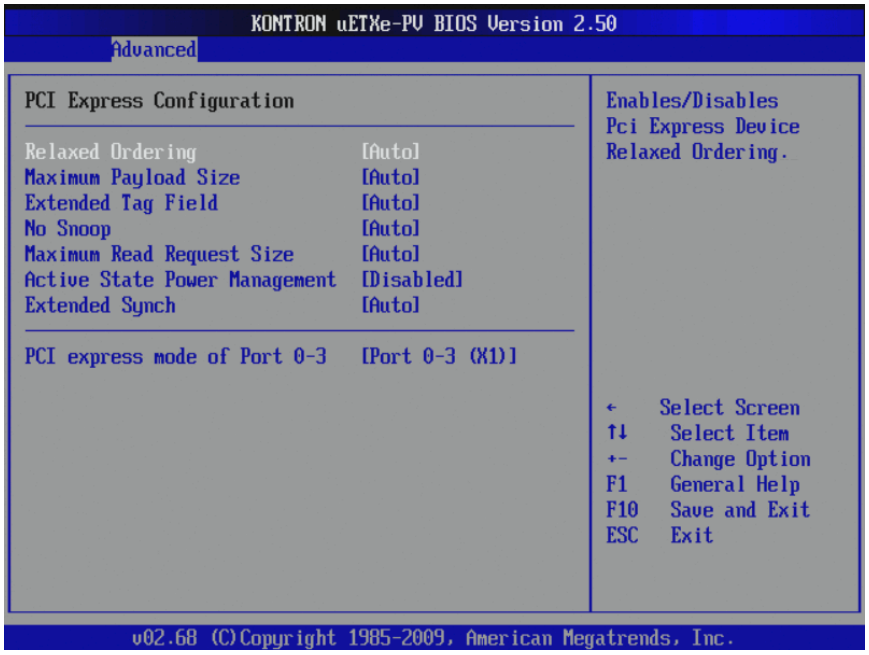
Feature	Option	Description
	GPI 3	
Invert GPI Signal #B	**LOW** High	Allows selection of GPI state that will generate an interrupt.

MPS Configuration



Feature	Option	Description
MPS revision	**1.4** 1.1	Configures the multiprocessor specification (MPS) revision level. (Some operating systems will require revision 1.1 for compatibility reasons.)

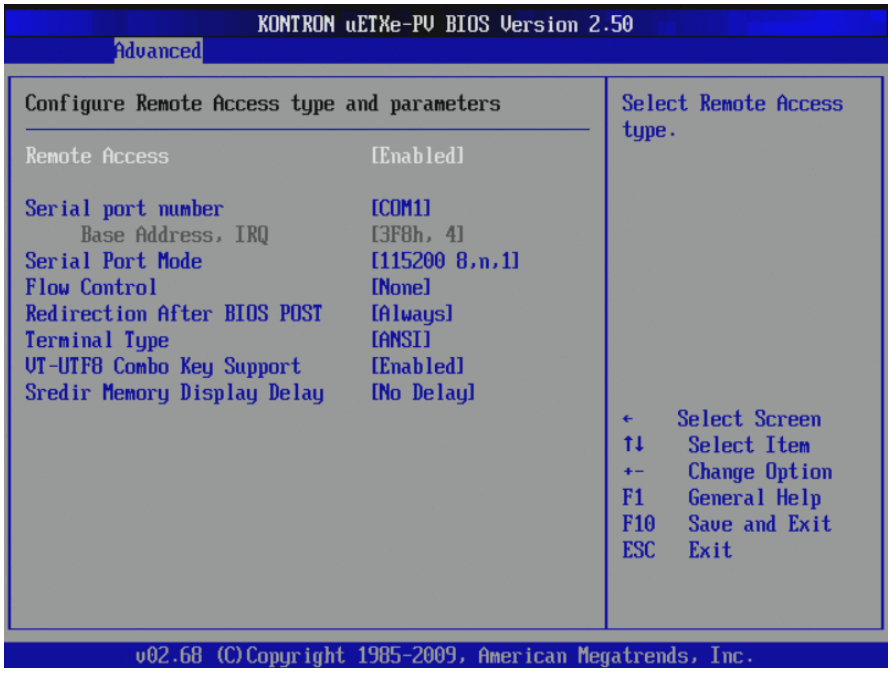
PCI Express Configuration



Feature	Option	Description
Relaxed Ordering	**Auto** Enabled **Disabled**	Applicable and set with AtomicOp Requests, where it affects the ordering of both the requests and their associated completions
Maximum Payload Size	**Auto** 128 bytes 256 bytes 512 bytes 1024 bytes 2048 bytes 4096 bytes	Sets maximum TLP payload size for the function As a receiver, the function must handle TLPs as large as the set value. As a transmitter, the function must not generate TLPs exceeding the set value.
Extended Tag Field	**Auto** Enabled Disabled	Enables function to use an 8-bit tag field as a requester If the bit is clear, the function is restricted to a 5-bit tag field.
No Snoop	**Auto** Enabled Disabled	Applicable and set with AtomicOp Requests, but atomicity must be guaranteed regardless of the No Snoop attribute value
Maximum Read Request Size	**Auto** 128 bytes	Sets the maximum Read Request size for the

Feature	Option	Description
	256 bytes 512 bytes 1024 bytes 2048 bytes 4096 bytes	function as a requester The function must not generate Read Requests with size exceeding the set value.
Active State Power Management	**Disabled** Enabled	Enables or disables PCI Express L0 and L1 link power states
Maximum Read Request Size	**Auto** Enabled Disabled	Configures Maximum Read Request Size
Active State Power-Management	Enabled **Disabled**	Enables or disables PCI Express L0 and L1 link power states
Extended Synch	**Auto** Disabled Enabled	If enabled, forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state This mode provides external devices (e.g., logic analyzers) monitoring the link time to achieve bit and symbol lock before the link enters the L0 state and resumes communication
PCI express mode of Port 0-3	**Port 0-3 (x1)** P0(X2), P2-3(X1) P0(X2), P2(X2) Port 0 (X4)	Allows configuration of PCIexpress ports 0 to 3 to different configurations. **WARNING:** Settings other than Port 0-3 (X1) cause an additional reset during the board power up sequence.

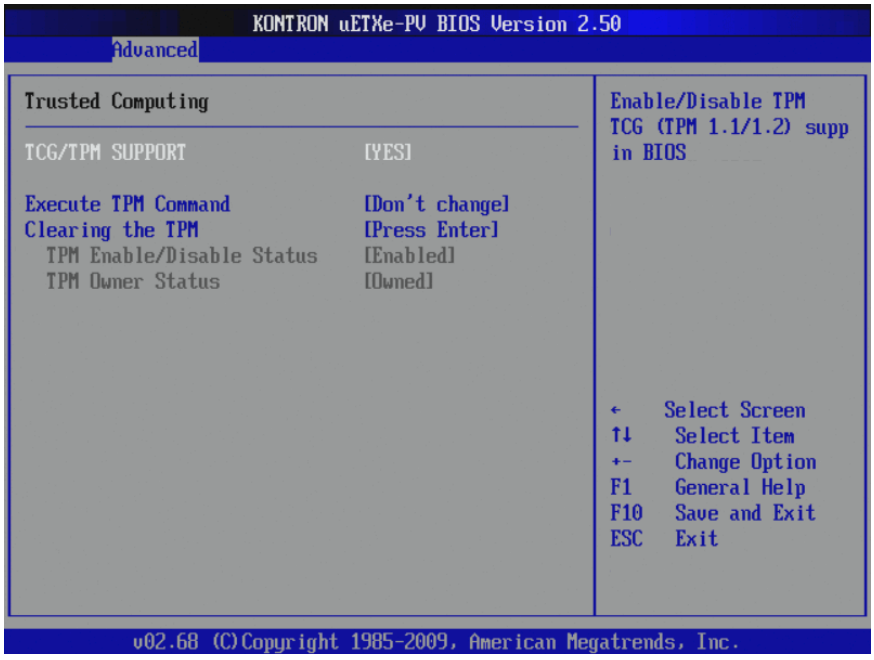
Remote Access Configuration



Feature	Option	Description
Remote Access	**Disabled** Enabled	Selects Remote Access type
Serial port number	**COM1** COM2	Allows the adjustment of serial port numbering
Base Address, IRQ	N/A	Displays the hardware address of the COM port.
Serial Port Mode	**115200 8,n, 1** 57600 8,n,1 38400 8,n,1 19200 8,n,1 09600 8,n,1	Configures serial port speed
Flow Control	**None** Hardware Software	Configures flow control for console redirection
Redirection After BIOS POST	Disabled Boot loader **Always**	Selects how the serial redirection done by the BIOS will operate after the POST
Terminal Type	**ANSI** VT100 VT-UTF8	Allows setting the terminal type
VT-UTF8 Combo Key Support	**Enabled**	Adds escape sequences for F1 to F12 and most other control keys on a keyboard
Sredir Memory	**No Delay**	Allows adding delay

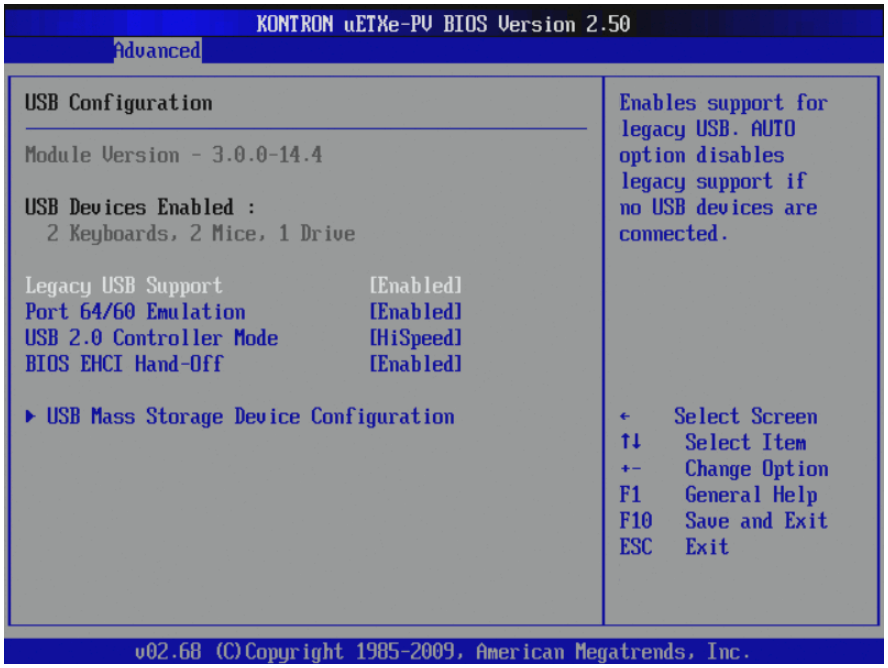
Feature	Option	Description
Display Delay	Delay 1 Sec Delay 2 Sec Delay 4 Sec	during POST for display of memory information

Trusted Computing



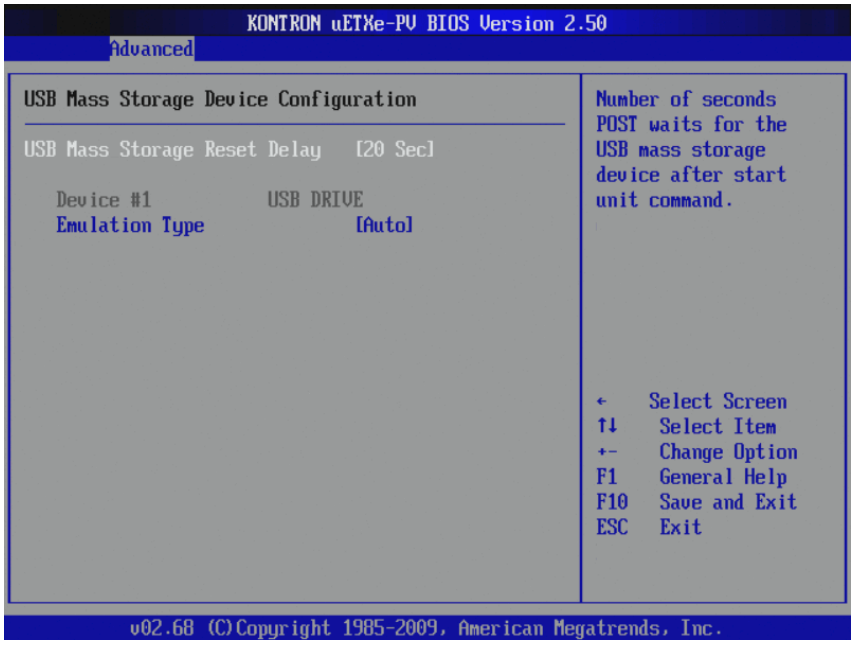
Feature	Option	Description
TCG/TPM Support	**YES**	Enables or disables TPS TCG (TPM 1.1/1.2) support in BIOS (Required for drivers or other programs to use the TPM chip)
Execute TPM Command	**Don't change**	Sets Execute TPM Command
Clearing the TPM	**Press Enter**	Sets Clearing the TPM
TPM Enable/Disable Status	**Enabled**	Enables or disables TPM Status
TPM Owner Status	**UnOwned**	Sets TPM Owner Status

USB Configuration



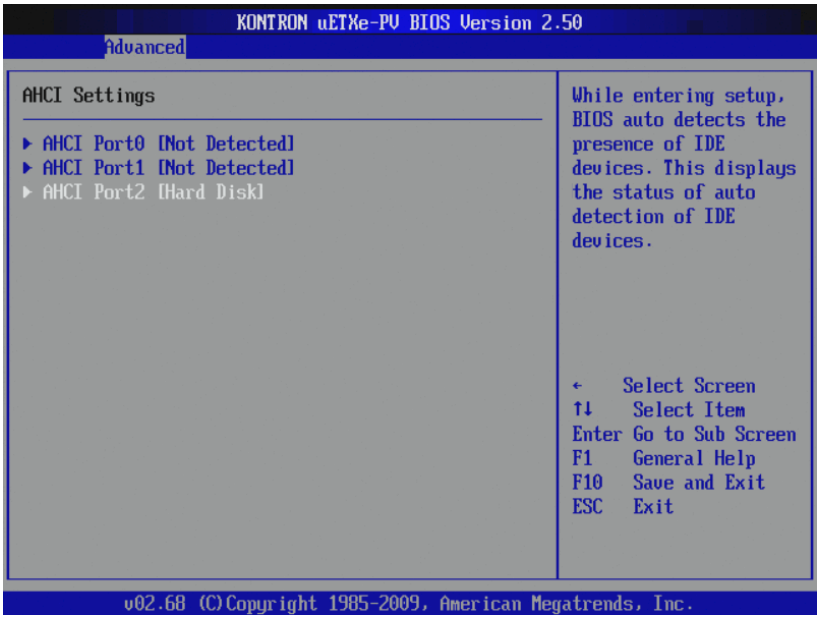
Feature	Option	Description
USB Devices Enabled: 2 Keyboards, 3 Mice	**N/A**	Display only Identifies what USB devices are enabled
Legacy USB Support	Disabled **Enabled** Auto	Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected
Port 64/60 Emulation	Disabled **Enabled**	Must be enabled for complete USB keyboard legacy support where OS is not USB-aware
USB 2.0 Controller Mode	FullSpeed **HiSpeed**	Configures the USB 2.0 controller in HiSpeed (480 Mbps) or FullSpeed (12 Mbps)
BIOS EHCI Hand-Off	Disabled **Enabled**	Workaround for an OS without EHCI hand-off support The EHCI ownership change should be claimed by the EHCI driver
USB Mass Storage Device Configuration	**N/A**	Submenu -- allows the USB Mass Storage device to be configured

USB Mass Storage Device Configuration



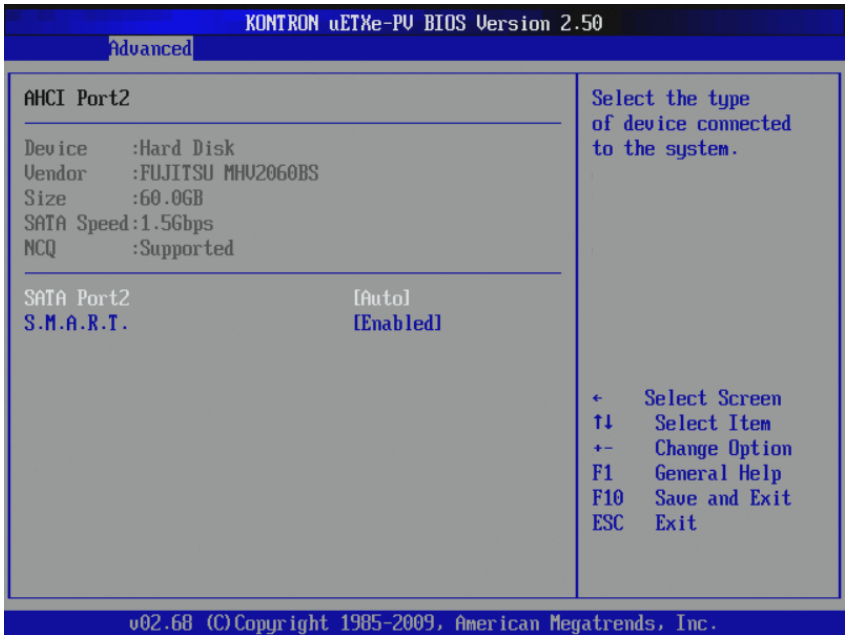
Feature	Option	Description
USB Mass Storage Reset Delay	**20 Sec**	Number of seconds POST waits for the USB mass storage device after the Start Unit command
Device #1	**N/A**	Display only Displays the 1st USB mass storage device description
Emulation Type	**Auto** Floppy Forced FDD Hard Disk CD-ROM	If Auto, USB devices less than 530MB are emulated as Floppy and remaining as hard drive Forced FDD option can be used to force an HDD formatted drive to boot as FDD (eg. ZIP drive)

AHCI Configuration



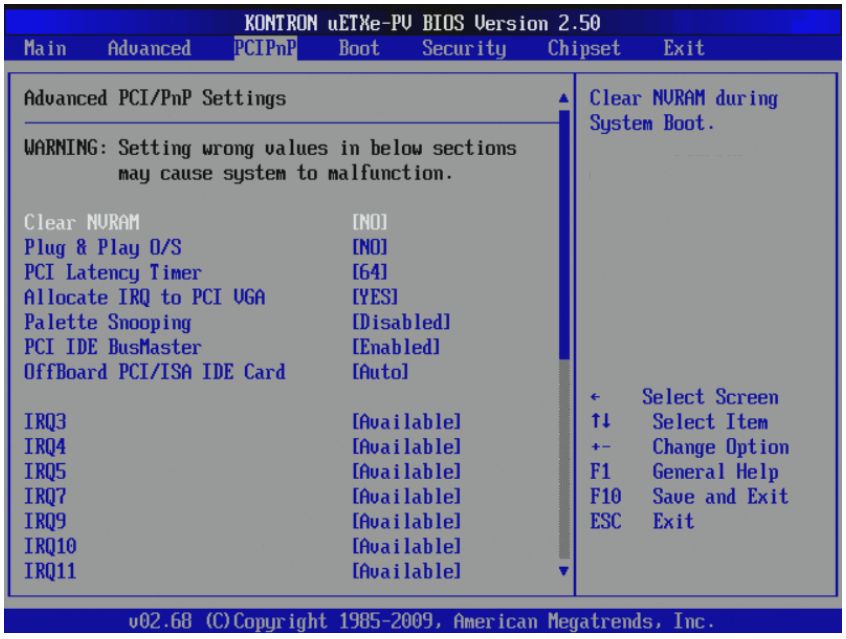
Feature	Option	Description
ACHI Port0	N/A	Selects sub-menu
ACHI Port1	N/A	Selects sub-menu
ACHI Port2	N/A	Selects sub-menu

AHCI Port2



Feature	Option	Description
Device	**N/A**	Shows device type.
Vendor	**N/A**	Shows HDD name and brand
Size	**N/A**	Shows HDD size
SATA Speed	**N/A**	Shows SATA Speed supported (1.5 or 3Gbps)
NCQ	**N/A**	Shows if device support NCQ
SATA Port2	**Auto** Not Installed	With "Not Installed" the controller disables the device.
S.M.A.R.T.	**Enabled** Disabled	Enables the BIOS to read the status of the disk prior to boot and display the information during POST

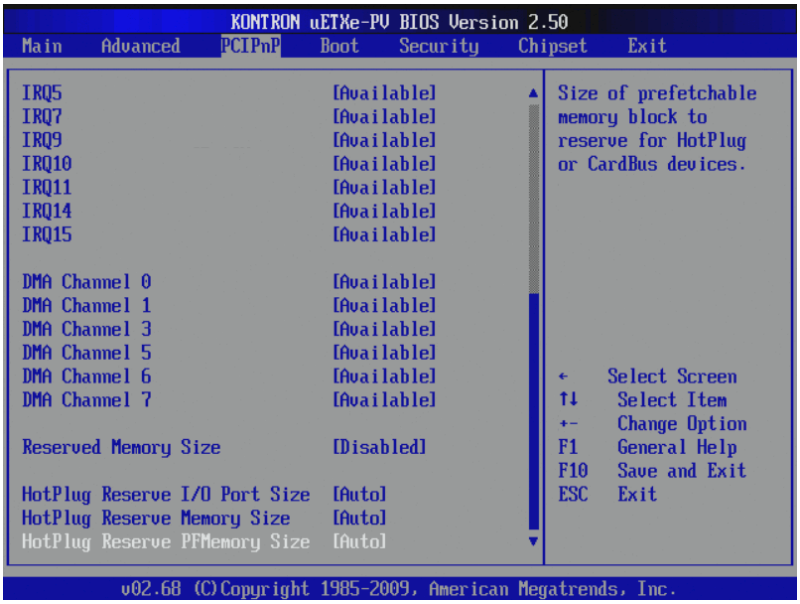
8.3.4PCIPnP Settings



Feature	Option	Description
Clear NVRAM	**No** Yes	BIOS stores information about PCI devices scanned and boot devices in NVRAM. Its content may no longer be valid and this may result in unexpected behaviors (this sometimes happens when there are many changes with devices connected to the system).

Feature	Option	Description
Plug & Play O/S	**No** Yes	No: the BIOS configures all the devices in the system Yes: the OS configures PnP devices not required for boot if your system has a Plug and Play OS
PCI Latency Timer	32 **64** 96 128 160 192 224 248	Sets this value to allow the Master Latency Timer to be adjusted. This option sets the latency for most PCI devices
Allocate IRQ to PCI VGA	**Yes** No	Allows the allocation of the IRQ to PCI VGA to be adjusted
Palette Snooping	**Disable** Enable	Enables or disables Palette Snooping
PCI IDE Bus master	Disable Enable	If enabled, improves the performance of the IDE interface for some operating systems (e.g. DOS)
OffBoard PCI/ISA IDE Card	**Auto** PCI Slot1 PCI Slot2 PCI Slot3 PCI Slot3 PCI Slot4 PCI Slot5	Allows the OffBoard PCI/ISA IDE card to be configured for plug & play
IRQ3 IRQ4 IRQ5 IRQ7 IRQ9 IRQ10 IRQ11 IRQ15	**Available** Available Available Available Available Available Available Available	Reserved means that this interrupt is a legacy IRQ (not shared). Available means this interrupt can be used as a PCI IRQ

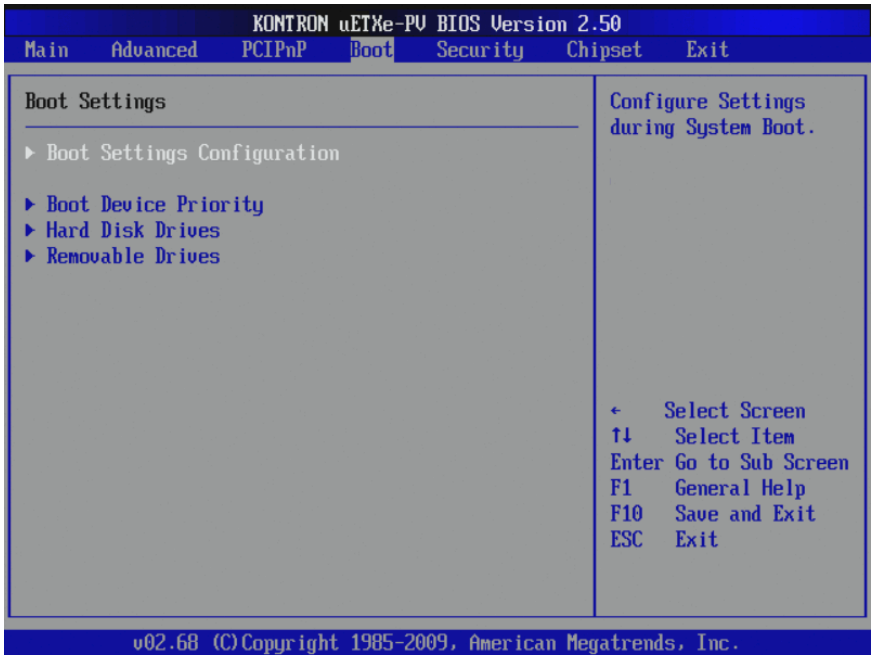
PCI Plug&Play Settings



Feature	Option	Description
DMA Channel 0 DMA Channel 1 DMA Channel 3 DMA Channel 5 DMA Channel 6 DMA Channel 7	**Available** Reserved	Available specifies that DMA is available for PCI/PnP
Reserved Memory Size	**Disabled** 16k 32k 64k	Size of memory block to reserve for legacy ISA devices
HotPlug Reserve I/O port Size	**Auto** 4k 8k 12k 16k 20k 24k 28k	Size of I/O port block to reserve for HotPlug or CardBus devices.
HotPlug Reserve Memory Size	**Auto** 8M 16M 32M 64M 128M 256M 512M	Size of memory block to reserve for HotPlug or CardBus devices

Feature	Option	Description
HotPlug Reserve PFMemory Size	**Auto** 32M 64M 128M 256M 512M 1024M 2048M	Size of pre-fetchable memory block to reserve for HotPlug or CardBus devices

8.3.5Boot Settings



Feature	Option	Description
Boot Settings Configuration	Submenu	Defines some special boot settings
Boot Device Priority		Allows the Boot Device Priority to be set
Removable Drives		

Boot Settings Configuration

Feature	Option	Description
Quick Boot	Disabled **Enabled**	Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system
Quiet Boot	**Disabled** Enabled	If disabled the BIOS generates the normal messages, otherwise an OEM logo can be displayed
AddOn ROM Display Mode	**Force BIOS** Keep Current	Keep Current keeps the current display mode. Force BIOS switches to BIOS mode before an AddOn ROM is called
Bootup Num-Lock	Off **On**	Selects power-on state for Numlock
PS/2 Mouse Support	Disabled Enabled **Auto**	If disabled or no PS/2 mouse is found (Auto) the BIOS frees up IRQ12
Wait For F1 If Error	Disabled **Enabled**	Enabled allows the BIOS to wait for any error. If an error is detected, pressing <F1> will enter the setup and the BIOS

Feature	Option	Description
		settings can be adjusting to fix the problem
Hit 'DEL' Message Display	**Disabled** Enabled	If enabled, boots new attached USB HDD first. If disabled, sets new attached USB HDD to last boot position
Interrupt 19h Capture	**Disabled** Enabled	If enabled AddOn ROMs can be trapped via Interrupt 19h (Boot IRQ). Use this option for network boot (PXE ROM)
Power Scheme	**ATX mode** Battery mode	With Battery mode selected, prevents southbridge to leave S3 or S5 if input voltage is low. (Refer to FPGA guide for more information)
Flash Write Protection	**Disabled** Enabled	Software flash write protection protects from unwanted software updates
Delay to add for Display	**Disabled** Delay 1 Sec Delay 2 Sec Delay 4 Sec	Adds delay to various POSTs to view all displayed messages

Boot Device Priority

Feature	Option	Description
1st Boot Device	Type: Boot device	Specifies the priority of the available boot sources The list includes USB CD ROM, USB Hard Drive, Hard Drive and PXE Other supported devices might be dynamically added to the list
Nth Boot Device	Type: Boot device	Specifies the priority of the available boot sources The list includes USB CD ROM, USB Hard Drive, Hard Drive and PXE Other supported devices might be dynamically added to the list.

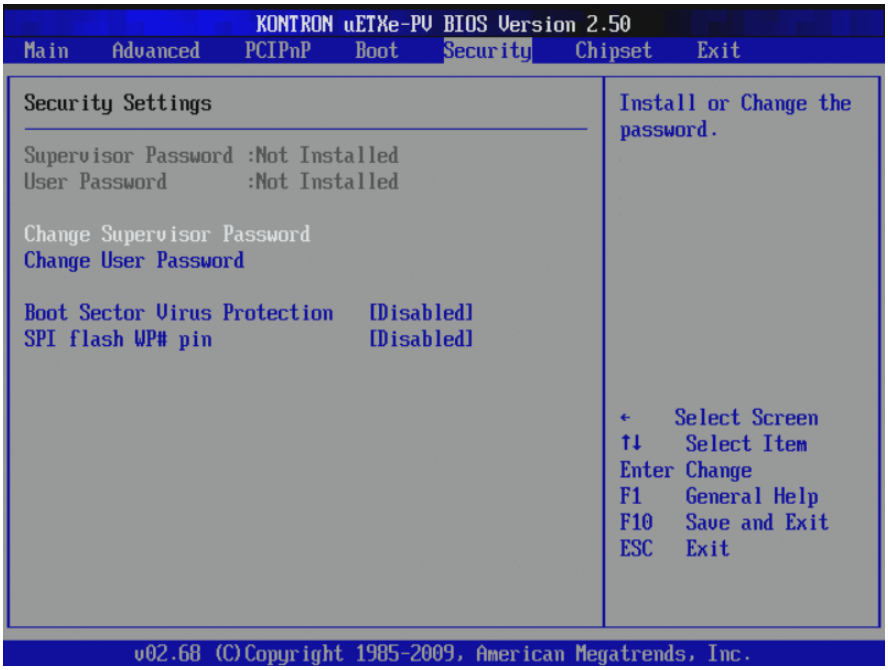
8.3.6Hard Disk Drives

Feature	Option	Description
1st Drive		Specifies the boot sequence from the available devices
Nth Drive		Specifies the boot sequence from the available devices

Removable Drives

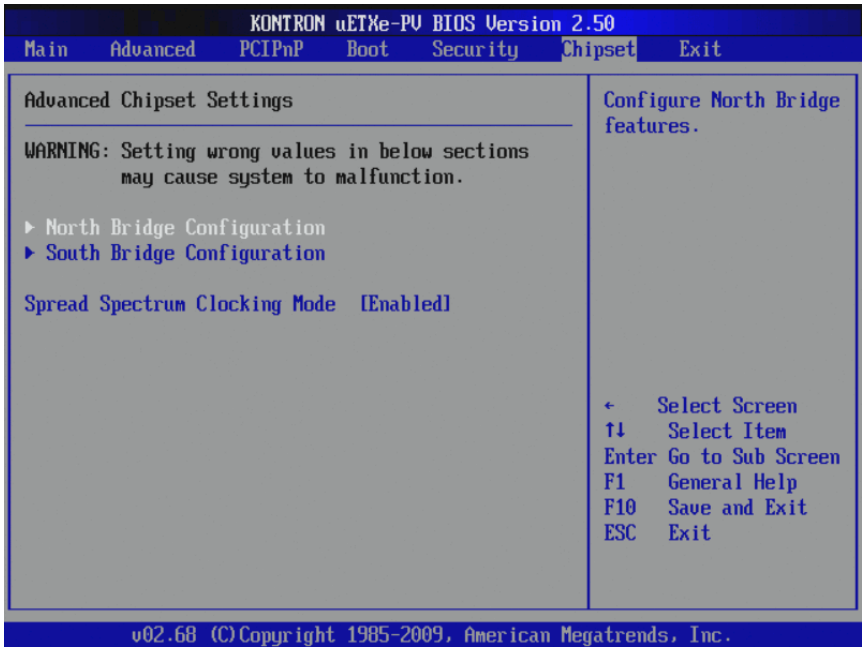
Feature	Option	Description
1st Drive		Specifies the boot sequence from the available devices
Nth Drive		Specifies the boot sequence from the available devices

8.3.7Security Settings



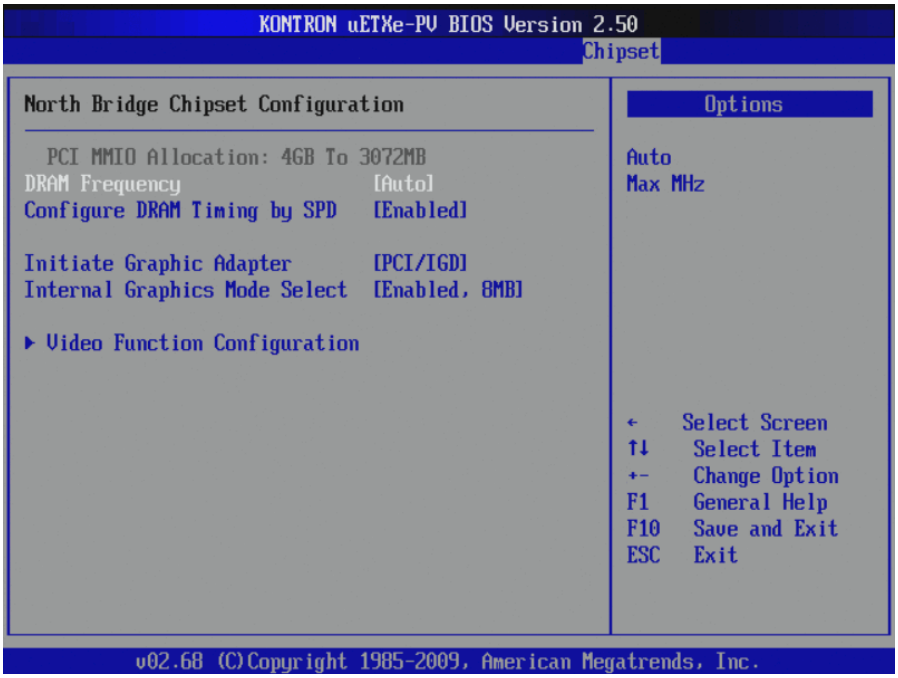
Feature	Option	Description
Supervisor Password	Installed Not Installed	Indicates the status of the Supervisor Password.
User Password	Installed Not Installed	Indicates the status of the User Password.
Change Supervisor Password		Select this option and press Enter to change the supervisor password
Change User Password		Select this option and press Enter to change the user password
Boot Sector Virus Protection	**Disable** Enable	If a program or a virus accesses the boot sector, a warning appears when the option is enabled
SPI flash WP# pin	**Disabled** Enabled	If HW supports it. this will assert the pin, WP#.

8.3.8Chipset Settings



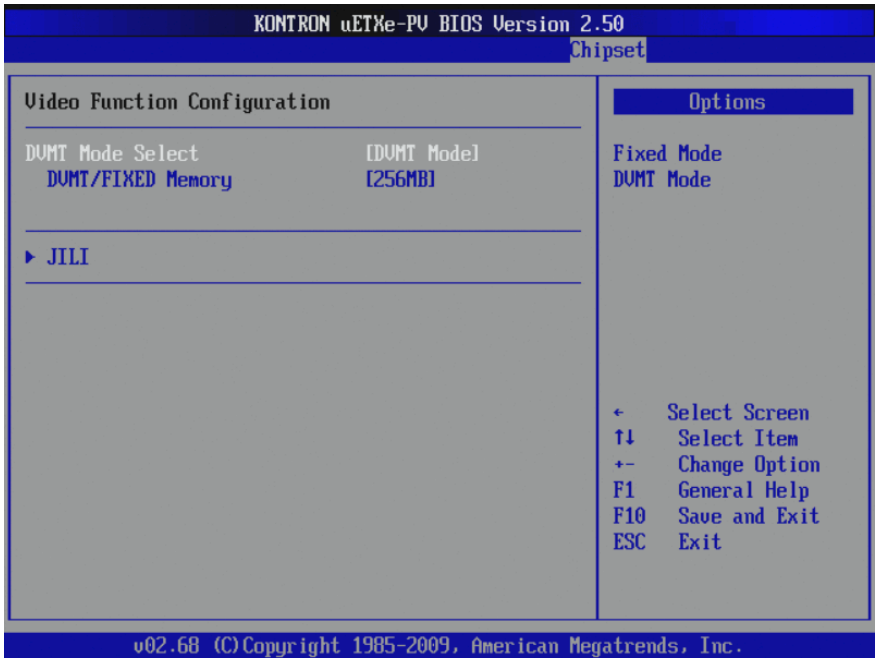
Feature	Option	Description
North Bridge Configuration		Configures North Bridge features
South Bridge Configuration		Configures South Bridge features
Spread Spectrum Clocking Mode	**Enabled** Disabled	Allows BIOS to set Clock Spread Spectrum for EMI (electromagnetic interference) control.

North Bridge Configuration



Feature	Option	Description
PCI MMIO Allocation: 4GB to 3072MB		
DRAM Frequency	**Auto** 667 MHz 800 MHz	Allows the DRAM frequency to be designated if it is not set to auto-detect
Initiate Graphic Adapter	IGD **PCI/IGD** PCI/PEG PEC/IGD PEC/PCI	Select which bus the BIOS will check first to find a graphic controller
Internal Graphics Mode Select	**Enabled, 8MB**	This is the only choice for this board
Video Function Configuration	N/A	Display sub-menu

Video Function Configuration



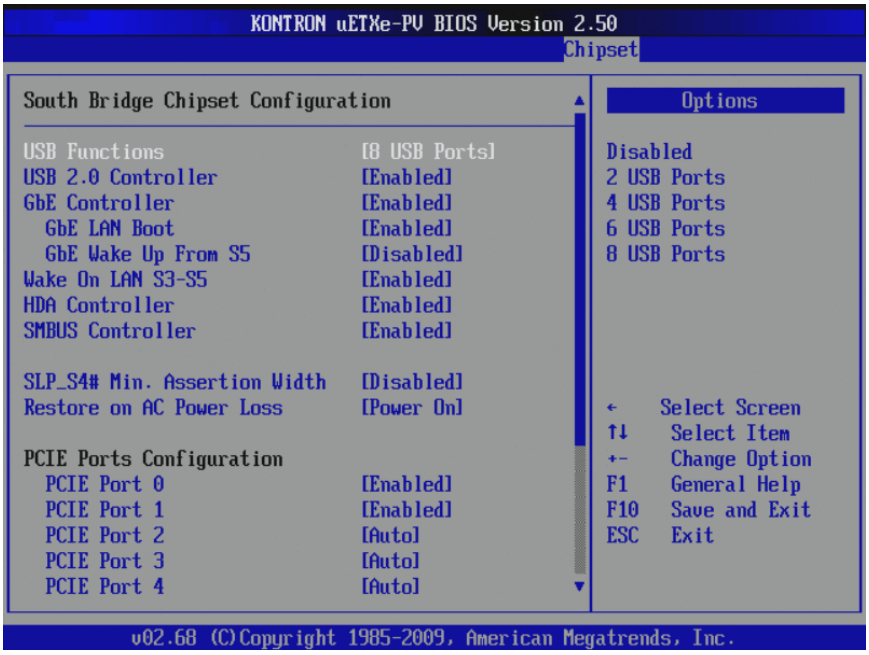
Feature	Option	Description
DVMT Mode Select	Fixed Mode DVMT mode	Displays the active system memory mode
DVMT/Fixed Memory	128MB **256MB** Maximum DVMT	Specifies the amount of DVMT/Fixed system memory to allocate for video memory
JILI	N/A	Jili sub-menu

JILI Display Configuration

Feature	Option	Description
JDA Revision	N/A	Displays the JDA revision
Boot Display Device	Auto CRT LVDS **CRT + LVDS**	Selects boot display device at POST stage of the BIOS
Flat Panel MODE	**Auto** Fixed PAID FPID	Selects the resolution of the panel connected to the board
Flat Panel Type	VGA 640x480 **SVGA 800x600** XGA 1024x768 WXGA 1280x768 WVGA 800x480 WXGA 1366x768 WXGA 1280x800	Allows selection of panel resolution (Depends on the panel type and the resolution of the chipset)
PAID/FPID	Various	Only displays when "Flat Panel MODE" = "FPID" or "PAID"
Local Flat Panel Scaling	Centered **Stretched** Disabled	Option applied before the drivers start
Color Depth	18bit	Only option and the maximum supported.

Backlight Startup Value	Varies from 1 to 254.	Boot values programmed in the Northbridge for the backlight

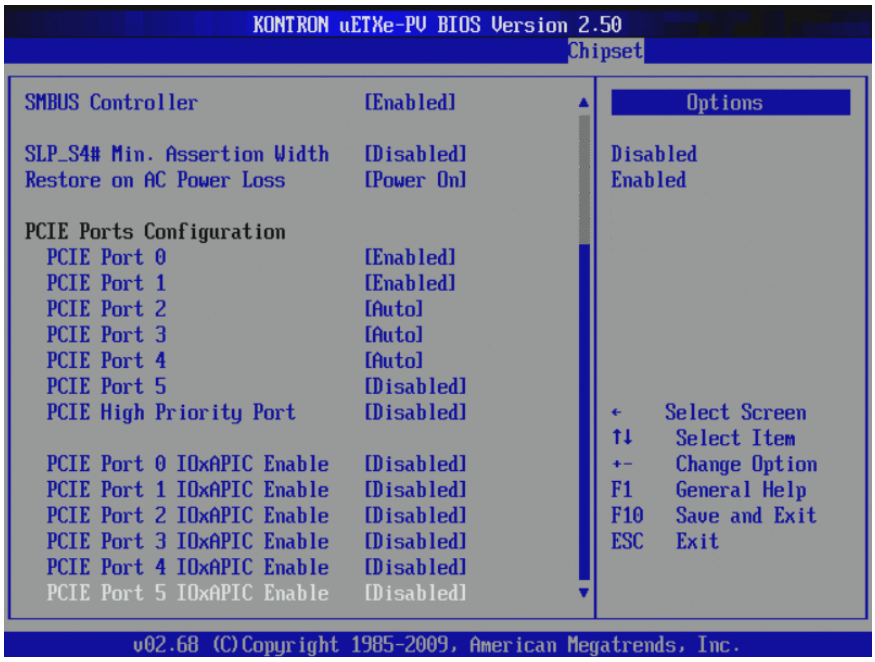
South Bridge Configuration



Feature	Option	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports 6 USB Ports **8 USB Ports**	Selects the number of USB ports for the board
USB 2.0 Controller	**Enabled** Disabled	Enables or disables the USB 2.0 controller
GbE Controller	**Enabled** Disabled	Enables or disables the integrated GbE controller
GbE LAN boot	**Enabled** Disabled	Allows the PXE boot option ROM to be executed during POST **NOTE:** only used when option "GbE Controller" is set to "Enabled"
GbE Wake up From S5	Enabled **Disabled**	Allows PME_B0_EN in chipset registers Used to enable GbE to wake system from S5
Wake On LAN S3-S5	**Enabled** Disabled	Allows WOL on the GbE chip

HDA Controller	**Enabled** Disabled	Enables or disables the High Definition Audio device

SMBus Controller Configuration



Feature	Option	Description
SMBUS Controller	**Enabled** Disabled	Enables or disables the SMBus controller. BDF(0,1F,3)
SLP_S4# Min. Assertion Width	**Disabled** 4 to 5 seconds 3 to 4 seconds 2 to 3 seconds 1 to 2 seconds	Enables or diables setting a delay of seconds before the SLP_S4# signal Used to guarantee that the DRAMs have been safely power-cycled
Restore On AC Power Loss	Power Off **Power On** Last State	Power Off = keep power off until reinsertion Last State = restore previous power state Power On = restore power to the board
PCIE Port 0	Auto **Enabled** Disabled	Enables or disables the PCIe port on the south bridge

Feature	Option	Description
		Auto only enables the device if device is present
PCIE Port 1	Auto **Enabled** Disabled	Enables or disables the PCIe port on the south bridge Auto only enables the device if device is present
PCIE Port 2	**Auto** Enabled Disabled	Enables or disables the PCIe port on the south bridge Auto only enables the device if device is present
PCIE Port 3	**Auto** Enabled Disabled	Enables or disables the PCIe port on the south bridge Auto only enables the device if device is present
PCIE Port 4	**Auto** Enabled Disabled	Enables or disables the PCIe port on the south bridge Auto only enables the device if device is present
PCIE Port 5	Auto Enabled **Disabled**	Enables or disables the PCIe port on the south bridge Auto only enables the device if device is present
PCIE High Priority Port	**Disabled** Port 0 Port 1 Port 2 Port 3 Port 4 Port 5	Enables High Priority Port on the selected port Selected port is arbitrated above all other VC0 devices
PCIE Port 0 IOxAPIC Enable	**Disabled** Enabled	Enables IOxAPIC for the PCIe port
PCIE Port 1 IOxAPIC Enable	**Disabled** Enabled	Enables IOxAPIC for the PCIe port
PCIE Port 2 IOxAPIC Enable	**Disabled** Enabled	Enables IOxAPIC for the PCIe port
PCIE Port 3 IOxAPIC Enable	**Disabled** Enabled	Enables IOxAPIC for the PCIe port
PCIE Port 4 IOxAPIC Enable	**Disabled** Enabled	Enables IOxAPIC for the PCIe port
PCIE Port 5	**Disabled**	Enables IOxAPIC for the

Feature	Option	Description
IOxAPIC Enable	Enabled	PCIe port

8.3.9Exit Options

Feature	Description
Save Changes and Exit	Exit system setup, save changes in CMOS and in JIDA eeprom F10 key can be used for this operation
Discard Changes and Exit	Exit system setup without saving any changes ESC key can be used for this operation
Discard Changes	Discards changes done so far to any of the setup questions F7 key can be used for this operation
Load Optimal Defaults	Loads the manufacture's designated optimal default settings F9 key can be used for this operation
Load Failsafe Defaults	Loads the designated fail-safe default settings F8 key can be used for this operation

8.4 Appendix A: JIDA Standard

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=Eah
- AL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

8.5 JIDA Information

To obtain information about boards that follow the JIDA standard, use the following procedure.

- Call Get BIOS ID with CL=1. The name of the first device installed will be returned. If you see the result Board exists (CL=0), increment CL, and call Get BIOS ID again.
- Repeat until you see Board not present (CL0). You now know the names of all boards within your system that follow the JIDA standard.
- You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

NOTE: Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai1xx.zip folder, which is available from the Kontron Web site, for further information on implementing and using JIDA calls with C sample code.

9 Appendix B: Architecture Information

The following sources of information can help you better understand PC architecture.

9.1 Buses

9.1.1ISA, Standard PS/2 – Connectors

» AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6

» AT IBM Technical Reference Vol. 1 and 2, 1985

» ISA and EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159

» ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel

» ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8

» Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc

» Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

9.1.2PCI/104

» Embedded PC 104 Consortium
The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.

» PCI SIG
The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.

» PCI and PCI-X Hardware and Software Architecture and Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.

» PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

9.2 General PC Architecture

» Embedded PCs, MarktandTechnik GmbH, ISBN 3-8272-5314-4 (German)

» Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8

» Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3

» The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9

» The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

9.3 Ports

9.3.1 RS-232 Serial

» EIA-232-E standard
The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.

» RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

» National Semiconductor: The Interface Data Book includes application notes. Type "232" as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor's Web site.

9.3.2 Serial ATA

» Serial AT Attachment (ATA) Working Group
This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web. We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

9.3.3 USB

» USB Specification
USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

9.4 Programming

» C Programmer's Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0

» Programmer's Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

» The Programmer's PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X

» Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

10 Appendix C: Document Revision History

Revision	Date	Changes
0.5	19-4-10	Initial review draft
0.8	04-6-10	Reviewed draft updated with comments and new figures and spec info
0.9	22-6-10	Preliminary draft
1.0	01-02-11	Final draft for product release
1.1	16-02-11	Update to I2C information
1.2	02-03-11	Updates throughout
1.3	03-24-11	New BIOS setup screens and tables, updates throughout
1.4	20 Oct 11	Update to max memory information and I2C speed support sections.

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